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Power Efficient Clock Pulsed D Flip Flop Using Transmission Gate

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ABSTRACT

The need for low-power sequential circuits is pushing towards the implementation of low power consuming basic memory elements like D Flip-Flop. To accomplish power efficient D Flip-Flop; we create a better-performance Current-Mode Pulse Triggered D Flip-Flop using 180nm CMOS technology. Here is a new idea for mode of clock distribution that uses current source, instead of voltage source, for the provision of a clock signal with reduced power consumption. In addition to Current-Mode signaling, Transmission Gate has been used to design the D Flip-Flop which also helps for power consumption in a great way. The Cadence-Virtuoso tool is to be used to simulate all the circuits with 180nm technology.

Index Terms: Current mode pulse triggered D-flip flop, clock distribution, current mode signaling,,180nm CMOS technology

1. INTRODUCTION

Portable electronic devices tend to require more lifetime on battery which can be achieved only by employing power efficient devices. The synchronous Application Specific Integrated Circuits (ASICs) are complex to design and consume more power because, in scaled technologies, the interconnect does consume a noticeably significant amount of power. Researcher scholars did demonstrate that the consumers which consume majority of this power, in general, are the Clock Distribution Networks (CDNs), and synchronous signals [1]. The previous result proves that clock distributed network in power four microprocessor absorbs 70% of total power of the chip. Design operating at high frequency ranges is effected by interconnection delay, besides power. Technology scaling decreases both the transistor and local interconnect delay while it increases the global interconnect delay [3], [4]. But, because of skew, jitter, and variability are mostly in proportion with large latencies [5], the conventional CDN structures are growing to become highly tough for multi-GHz Integrated Circuits Now we discuss about the following sections: Section II covers brief overview of conventional clocked D Flip-Flops. Section III shows a brief detail about existing CM signaling schemes. Section IV proposes our CM FF and CDN. Section V compares our new FF and CDN with existing scheme. Finally, Section VI concludes the paper.

2. CONVENTIONAL CLOCKED D FLIP-FLOPS

The voltage mode clock distribution networks are very widely used clock distribution networks in the real life applications. This is due to the fact that it is easy to analyze and operate with the voltage sources rather that with current sources. On the other hand almost all the transistors and gates used are being designed on specifications provided with the terms involving voltages.

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The Voltage Mode Clock Distribution Networks pulsed D flip-flop is most oldest versions of the D flip-flop. The power consumption in this type of flip-flops is noticeably high and the area is low. When implemented as an individual circuit the time analysis was also proven to be satisfied. But most of the applications of the D flip-flop were found in the sequential circuits like Registers, Counters etc... These types of circuits use a number of D flip-flops in series to satisfy the required design. When the D flip-flops are employed are in these circuits the power consumption is one of the major issues which is to be taken into account. For meeting that specification many changes are being made in the D flip-flop, till date. Irrespective of the changes made in the design, the working of the D flip-flop is always is always the same but the implementation alone changes.

These conventional schemes used an expensive trans-impedance amplifier receiver which may result in noticeable skew due to shift if applied to Clock Distribution Networks [10].

3. EXISTING CM SIGNALING SCHEME

In earlier current mode logic is considered mostly due to high speed signaling scheme. But VM signaling has become alternate for CM signaling as it dissipates static power due to its high speed.

3.1. VM vs CM

Issues due to interconnect power and variability can be solved by low swing and current mode signaling schemes. Earlier current-mode schemes have been implemented for mostly, off-chip signals. Standard logic signals need to have remained VM to gain advantage from the low static power of CMOS logic. Normally in current mode signaling circuits the static power consumption very high comparing with dynamic power dissipation. But in cmos circuits dynamic power dissipation is a major factor. In voltage mode the dynamic power dissipation is less when compared to the static power dissipation. The latency is mainly improved in global current mode interconnect than voltage mode circuits. Current mode signaling scheme provide more receptive and they are not much receptive to single event transient changes in the clock pulses because of no buffers in source and drain diffusion will be affected by high energy particles of electrons and hole in the semi conductor. In this ideology, there is no practical possibility for making each of the point-to-point segments of the Clock distribution node of current-mode, but the clock signal should

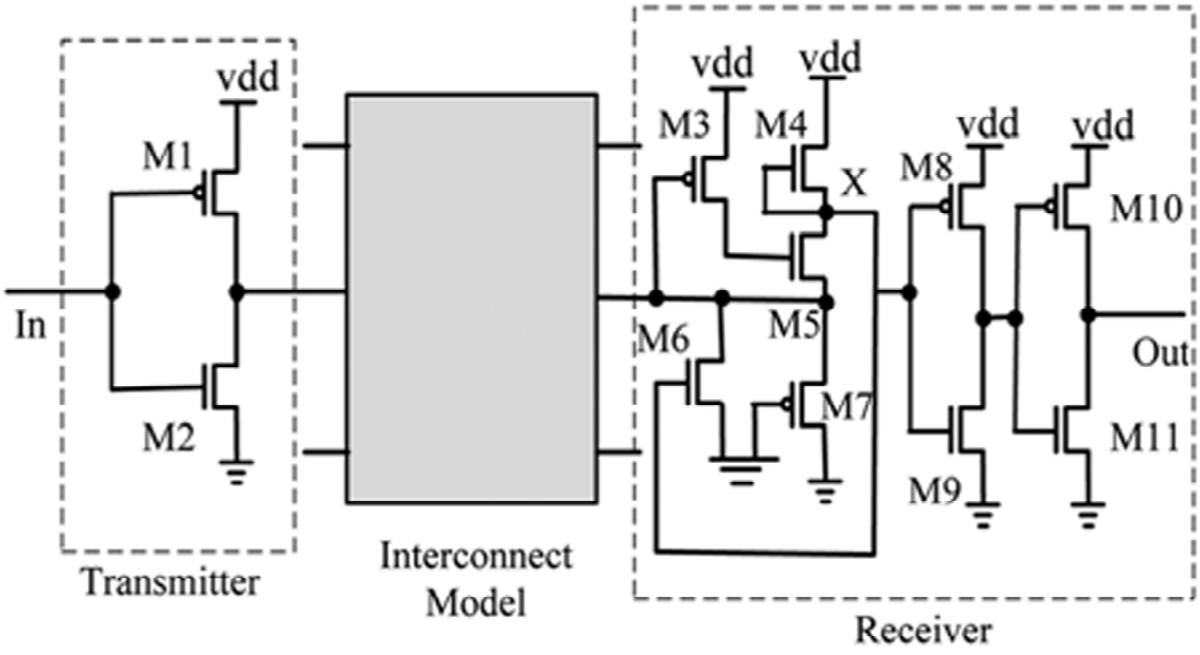

Figure 1: Conventional D Flip-Flop with VM Signaling.

have to be benefitted from the reliability and power of current-mode signaling. In recent days with the effort of low power consumption that increased the fan out of the circuit by connecting many current mode flip-flops at the receiver. At the flip-flop receiver it retains voltage mode signaling with low power in cmos ICs.

3.2. Overview

In current mode signaling scheme transmitter which uses a voltage mode input signal for transmission of a current by reducing voltage swing, less compared with normal voltage swing into an interconnect like conversion of current to voltage in the receiver of transmission line. The Current Mode scheme, which is represented here, uses a different transmitter and receiver. The CMOS inverter is used as the Transmitter and the type of Receiver used is based on a trans-impedance amplifier. This Current Mode scheme has a provision for improvement in delay over Voltage Mode schemes, but the swings of Receiver voltage is around a Common-Mode voltage and in the case of any shift in the swings might result in a large skew in Clock Distribution Network. Each one of the past Current Mode signaling schemes performs the conversion from current to voltage and then uses the Voltage Mode clock signaling scheme, which is buffered. Moreover, the lowest level of a Clock Distribution Network driven with a full-swing of voltage gives a large dynamic power besides significant area to buffer for driving the capacitances of clock pin. To reduce total power consumption and IC area, this CM scheme is totally unified in flip-flops that receives the current mode signals.

3.3. Current Mode Clock Distribution Network Pulsed D Flip Flop (Cmpffe)

This CMPFFE is more or less same as the CMPFF, which was published earlier. But, the difference is that this CMPFFE has enable signal as an active-low signal. The CMPFFE uses a current-comparator (CC) stage as an input stage, followed by a register stage, and finally a static storage cell as a memory stage. The principle of current comparator stage is to compare the push-pull current input with the current from reference input and also does conditional amplification for the clock to provide a full-swing voltage pulse which

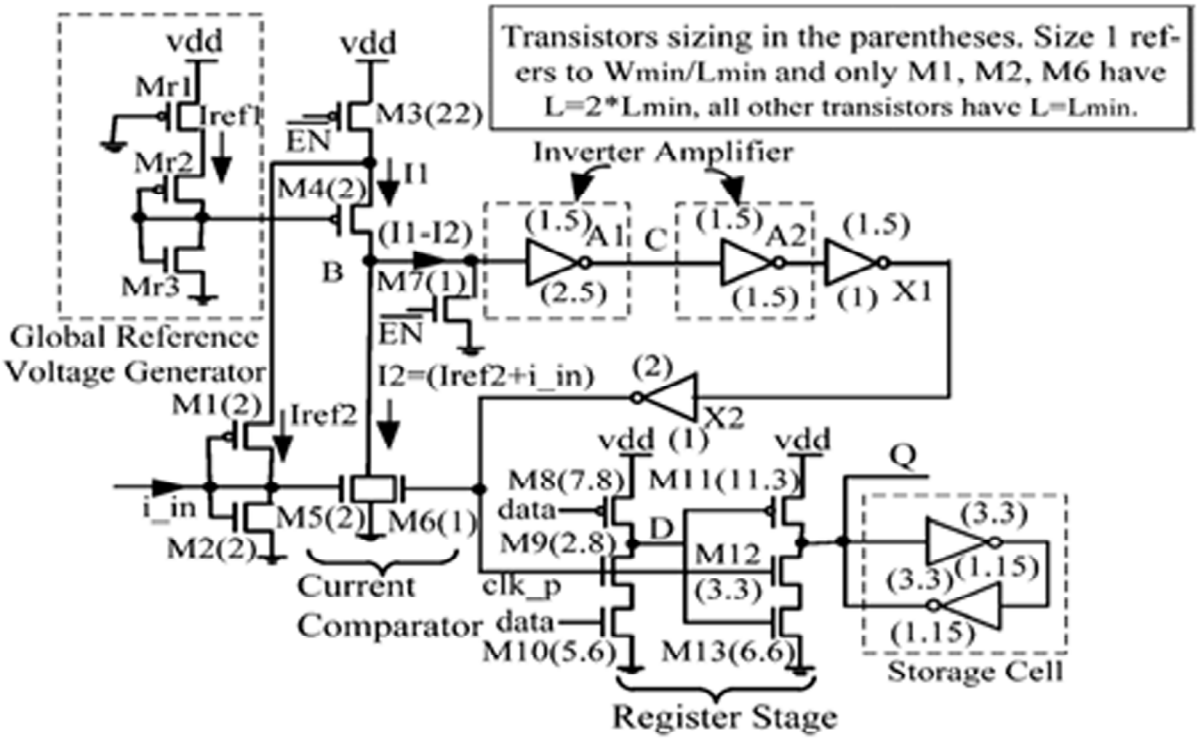

Figure 2: Existing D Flip-Flop with CM Signaling

activates the data to latch, which is in the register stage. The feedback pulsed Flip-Flop is a way different from the earlier CM schemes which happened to utilize costlier circuits for receiver and buffers for driving the final Flip-Flops.

The option of push-pull current provides enable for the simple transmitter circuit and also maintains a constant or low-swing bias voltage on the Clock Distribution Network interconnect. The CMPFFE circuit acts sensible only to the current that has unidirectional push that gives the Flip-Flop, an operation based on positive edge triggering.

Proposed CMPFFE employs the current-comparator and a connection for feedback which is for the generation of a voltage pulse which is used to trigger the register stage for storing the data in storage cell.

The simulation waveforms shown in the Fig. 3 confirm that the internal current-to-voltage pulse generation which triggers the capture of input data.

4. PROPOSED SYSTEM

The existing system completely aims on reducing the power only by reducing the power consumed by the Clock Distribution Networks. By concentrating on the Clock Distribution Networks, it is true that the power consumption can be reduced to greater extent. There are also other methods of reducing the consumption of power by implementing the D flip-flop by more power efficient logic. One of such methods is implementing D flip-flop using Transmission Gate Logic (TGL).

4.1. Proposed model

The D flip-flop is totally modified with transmission gates by applying concept called master slave.

This figure 4 describes the leading-edge triggered D flip-flop with only clock signal without any Set, Reset and Clear signals. The input signal is **d**, **pc** is the clock signal**, pcb** is the complement of the clock signal or it can be said as the inverted clock signal and **q** is the output of the D flip-flop. The input is given to the input line of D flip-flop. The Transmission Gates are provided with the mutually complement clock pulses. When the leading edge of clock pulse arrives, both the transistors, nmos and pmos of the TG-1 gets in to ON state and the input signal provided gets transmitted through the gate. Similarly the TG-2 which gets the clock pulses quite complement to the clock pulses received by the TG-1, and so the TG-2 remains in OFF state as neither of the transistors gets into active region. The TG-3 which receives the similar clock

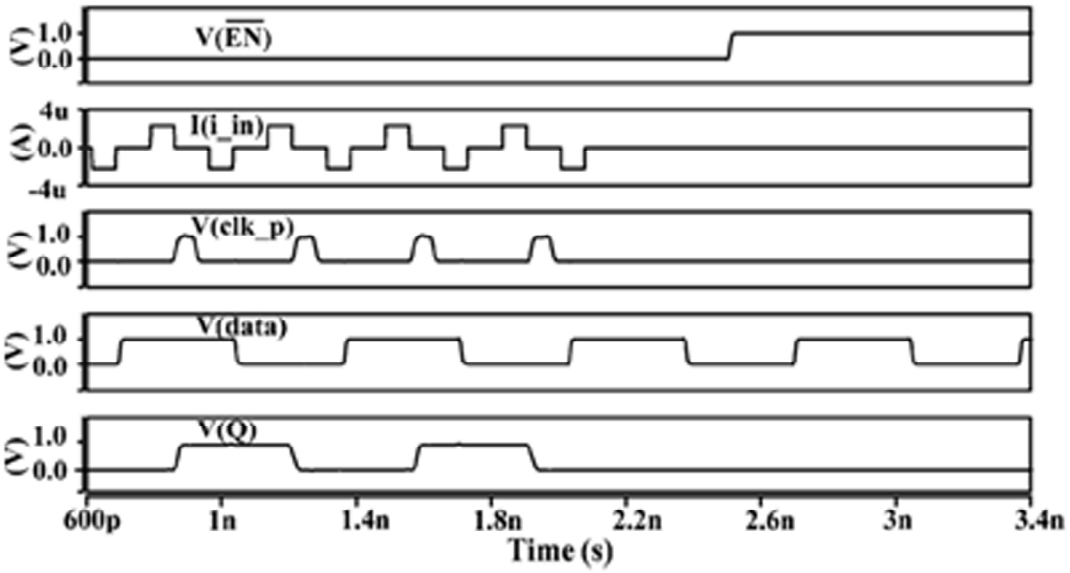

Figure 3: Output of Existing D Flip-Flop with CM Signaling

pulses like the TG-2 remains in OFF state for the same reason. Now the TG-4, which gets the clock pulses same as those of TG-1, gets into ON state and the data gets transmitted.

Now since the data provided at the input doesn't get propagated to the output, the memory stage comes into the act. When leading-edge of the clock does not arrive it is the feature of the D Flip-Flop that it has to maintain to the previous stage's output and it is done by the memory stage of the D Flip-Flop.

4.2. Proposed Final Structure

The main change in the proposed final structure and all the other structures sis the CDN. All the other structures use Voltage-Mode Clock Distribution Networks but here we are using Current Mode Clock Distribution Networks.

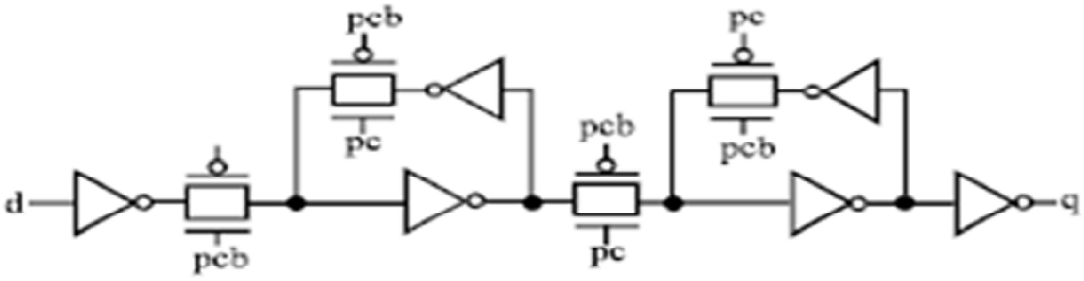

Figure 4: Model of Register stage of the Proposed D Flip-Flop

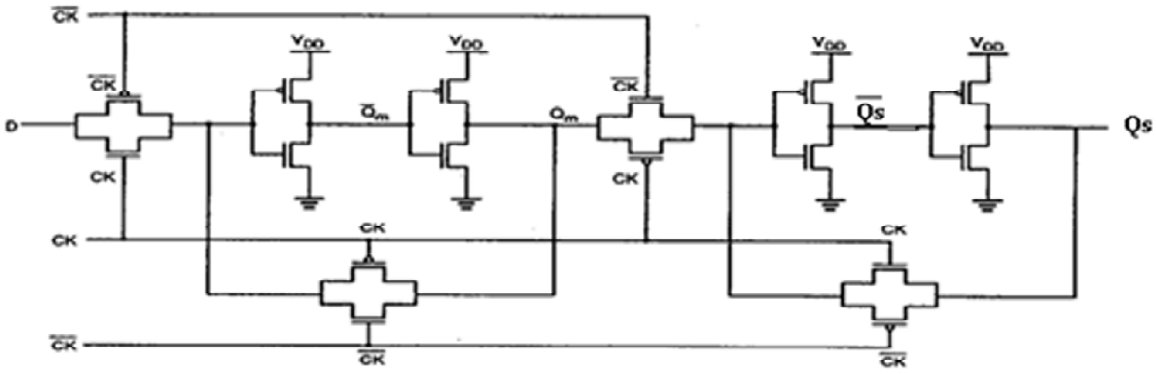

Figure 5: Final Structure of Register stage of Proposed D Flip-Flop

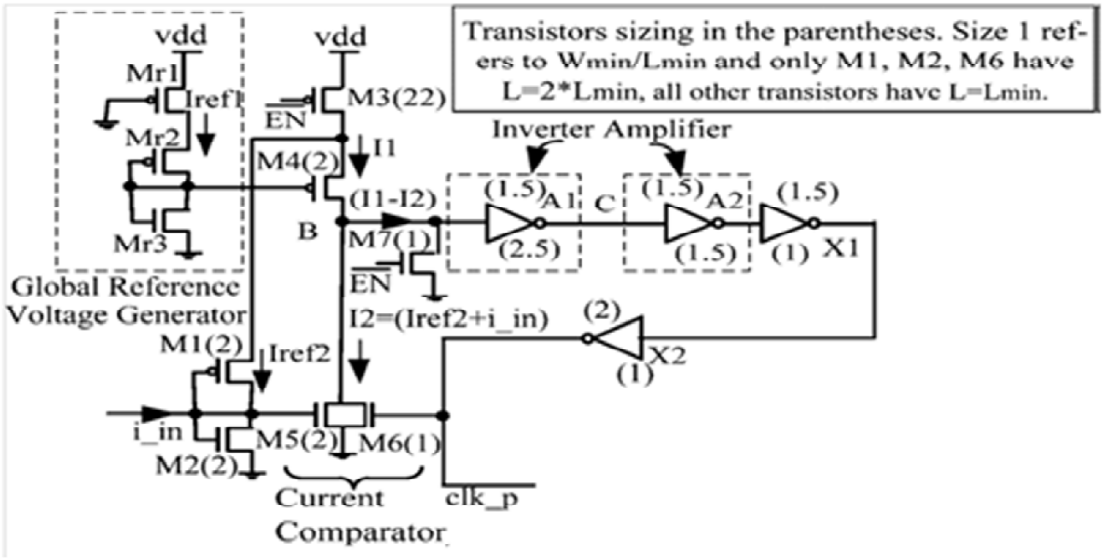

Figure 6: Current-Mode Clock Distribution Network

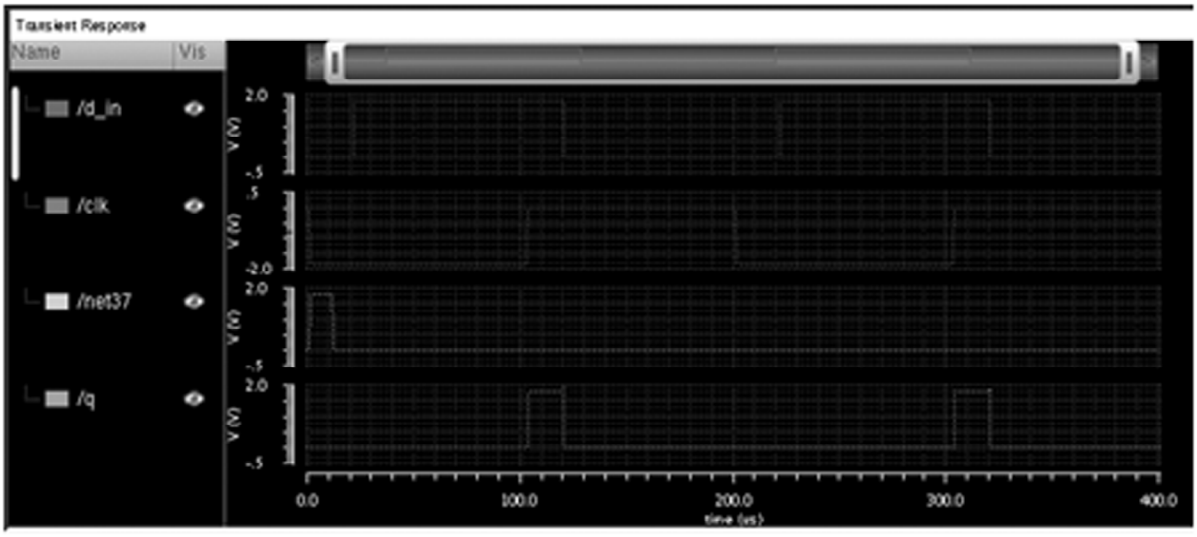

Figure 7: Transient Response of the Proposed final model

The clock input to the final proposed structure of the D flip-flop (Fig. 4) is provided from the output of the Current-Mode Clock Distribution Network (Fig. 5).

4.3. Design Considerations

For designing the proposed D Flip-Flop, some design issues have to be kept in mind. For the determination of the size of the transistors used in the input stage i.e., the current comparator stage, it is mandatory to ensure that the time which the current comparator stage consumes as much as for the other transistors present in the circuit.

The condition discussed in the previous paragraph could be achieved easily by providing the perfect design to the transistors in the stage of Global Reference Voltage Generator. In addition to it, if there is any possibility in the fabrication technology, sometimes, the low-threshold pMOS transistors could also be used as the transistors to control which leads to speed turning on. For the design the nMOS transistors, located in the Pull-Down Network, the voltage across drain and source of these switches must be taken into consideration as it might provide limitations to the headroom in voltage, which might probably restrict the advantage of being used in applications of low-voltage. For reducing the above stated effect, nMOS transistors with low-resistance are essential. It can also be said that, transistors with large area have to be employed. Because of the parasitic capacitances present in these switches might be ineffective to the parasitic capacitances present in the nMOS and pMOS transistors, it is possible for optimal selection of the size of the nMOS switch transistors. It should happen in a way such that both the operations likely, low-power and low-voltage are satisfied.

5. RESULTS AND COMPARISONS

Since that the D Flip-Flop is the basic circuit element of almost all the synchronous and asynchronous sequential circuits, the reduction in power consumption in such a basic circuit element multiplies the effect as the size and complexity of the circuit, involving such type of D Flip-Flop, increases.

The average power consumption in the Existing System in 180nm technology has been found to be 901.3e-3 W. Whereas, the average power consumption in the proposed idea has been found to be 154.8e-3 W. Hence, it is proven that the average power consumption of the proposed is 17.175% of the existing system. Such a power efficient D Flip-Flop can be applied to low-power sequential circuits in the near future.

Figure 8: Average power of the existing system

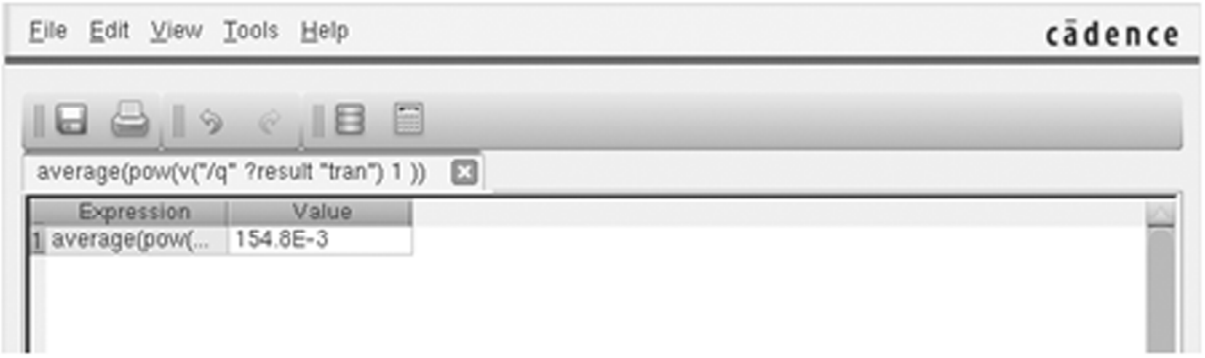

Figure 9: Average power of the proposed system

6. CONCLUSION

In this research, we designed current mode flip-flop implemented using Transmission Gate Logic. This CMPFFE eradicates the problem presented in complex CM receiver circuits and use of local VM buffers for high capacitive clock sinks to be driven into Current Mode signaling schemes that are proposed previously. Generally, the CMPFFE gives us a power reduction of 24% to 62% on average power compared to conventional VM CDNs, when used in a CM CDN. This is even better because the proposed D Flip-Flop consumes 17.175% of the average power consumed by the existing CMPFFE, requires similar silicon.

REFERENCES

[1] H. Zhang, G. Varghese, and J.M. Rabaey, "Low swing on-chip signaling techniques: Effectiveness and robustness," IEEE Trans. Very Large Scale Integrated. (VLSI) Syst., vol. 8, no. 3, pp. 264–272, Jun. 2000.

[2] C. Anderson, J. Petrovick, J. Keaty, J. Warnock, G. Nussbaum, J. Tendier, C. Carter, S. Chu, J. Clabes, J. DiLullo, P. Dudley, P. Harvey, B. Krauter, J. LeBlanc, P.F. Lu, B. McCredie, G. Plum, P. Restle, S. Runyon, M. Scheuermann, S. Schmidt, J. Wagoner, R. Weiss, S. Weitzel, and B. Zoric, "Physical design of a fourth-generation power ghz microprocessor," in Proc. ISSCC, Feb. 2001, pp. 232–233.

[3] D. Sylvester and C. Hu, "Analytical modeling and characterization of deep-sub-micrometer interconnect," Proc. IEEE, vol. 89, no. 5, pp. 634–664, May 2001.

[4] A. Katoch, H. Veendrick, and E. Seevinck, "High speed current-mode signaling circuits for on-chip interconnects," in Proc. ISCAS, May 2005, pp. 4138–4141.

[5] M. R. Guthaus, G. Wilke, and R. Reis, "Revisiting automated physical synthesis of high-performance clock networks," ACM Trans. Design Autom. Electron. Syst., vol. 18, no. 2, pp. 31:1–31:27, Apr. 2013.

[6] M. Yamashina and H. Yamada, "An MOS current mode logic (MCML) circuit for low-power sub-GHz processors," IEICE Trans. Electron. vol. E75-C, no. 10, pp. 1181–1187, 1992.

[7] E. Seevinck, P. J. V. Beers, and H. Ontrop, "Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAM's," J. Solid-State Circuits, vol. 26, no. 4, pp. 525–536, Apr. 1991.

[8] M. Dave, M. Jain, S. Baghini, and D. Sharma, "A variation tolerant current-mode signaling scheme for on-chip interconnects," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. PP, no. 99, pp. 1–12, Jan. 2012.

[9] F. Yuan, Cmos Current-Mode Circuits for Data Communications. New York: Springer, Apr. 2007.

[10] A. Narasimhan, S. Divekar, P. Elakkumanan, and R. Sridhar, "A lowpower current-mode clock distribution scheme for multi-GHz NoCbased SoCs," in Proc. 18th Int. Conf. VLSI Design, Jan. 2005, pp. 130–135.