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Hardware Implementation of Single Phase Diode Clamped 3-Level Inverter

R. Palanisamy[*] and K. Vijayakumar[**]

Abstract: This work offers an enhanced hardware implementation of single phase diode Clamped 3-Level Inverter (DC-TLI) that is suitable for renewable energy based grid connected systems. The exploit of DC-TLI structure assurance to the reduction of shoot through state risk and provides minimized common mode voltage. This inverter system is controlled by Hysteresis Space Vector Modulation (HSVM) algorithm which assists to reduce Total Harmonic Distortion (THD) in the output voltage and current. Furthermore, the voltage stress in the inverter also minimized by using this proposed control strategy. The proposed system hardware results were verified using dspic microcontroller.

Keywords: Diode Clamped 3-Level Inverter (DC-TLI)**,** Hysteresis Space Vector Modulation (HSVM), PV system, dspic microcontroller.

1. INTRODUCTION

Power generated from PV systems are usually supplied to a grid system through a transformer, which leads to an increase in overall size and cost, and decrease in the efficiency of the system. In order to overcome this issue, the use of transformer-less inverters have been studied implemented [1]. The choice of topology used depends on parameters like Total Harmonic Distortion (THD), reduced common mode voltage, leakage current loss and voltage stress. Multilevel inverters have been drawing interest in the recent past due to their good harmonic rejection capacity, and ability to handle high voltages [2]. The proposed system uses diode-clamped inverter technology that provides reduced *dv*/*dt* stresses on switching, ability to control reactive power flow and increased efficiency of output due to greater reduction of common mode voltages [3]. Reduction of common mode voltages will ensure decrease of electromagnetic interferences disturbing neighboring, and the prevention of premature motor bearing, shaft and winding failures that may be caused by it otherwise. The source of the inverter is derived from a PV system whose energy efficiency is optimized by tracking the maximum power point. PV arrays are generally known to be non-linear in nature and deliver maximum power at a particular operating point. This point is tracked by using a Perturb and Observe (P and O) Maximum Power Point Tracker (MPPT) technique [4].

The analysis and implementation of a three-phase three level inverter is observed in this paper, and modulation index used in it is based on Hysteresis Space Vector Modulation (HSVM). Space Vector Modulation has been gaining popularity due to its performance at low modulation ratio as compared to the standard Pulse Width Modulation (PWM) techniques [5], and simplicity in hardware and software implementation. A Space Vector Voltage Control (SVVC) is analyzed in order to use hexagonal hysteresis areas. This is a modification of the simplified space vector PWM technique [6]. Independent hysteresis comparators are used to identify and control the switching states of the inverter in each leg [7]. Three error voltages are congregated into one space vector component. The tip of the error moves on three separate areas limited by hexagonal contours [8],[9]. This leads to the selection of one among 27 distinct voltage vectors, which determines and controls both the switching state and current flowing in the circuit at Neutral Point (NP). This control technique is further analyzed and verified through simulations [10].

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2. PV SYSTEM MODELLING

The proposed system getting the source from the photovoltaic array system. A photovoltaic cell is a semiconductor device that converts light to electrical energy by photovoltaic effect. A PV array consists of several photovoltaic cells in series and parallel connections [11], [12]. Series connections are responsible for increasing the voltage of the module whereas the parallel connection is responsible for increasing the current in the array [13]. Typically a solar cell can be modeled by a current source and an inverted diode connected in parallel to it. It has its own series and parallel resistance [14], [15]. Series resistance is due to hindrance in the path of flow of electrons from n to p junction and parallel resistance is due to the leakage current.

Modeling of PV array done using output current equations are,

$$I = I_s - I_d \tag{1}$$

$$I_d = I_1(e^{qv_p/gs} - 1) \tag{2}$$

Where I_0 is the reverse saturation current of the diode, q is the electron charge, V_d is the voltage across the diode, k is Boltzmann constant and T is the junction temperature.

3. CONTROL UNIT AND DC-TLI INVERTER CIRCUIT

The control circuit consists of a 28-pin microcontroller (dcPIC30F) which controls the generation of switching pulses for the gate. It works at a CPU speed of 30 MIPS and is based on a modified Harvard Architecture. It has a Flash type memory and RAM space of 1024 Bytes. The dcPIC30F controls the functioning of Hysteresis Space Vector Modulation in the inverter, and generates clock pulses accordingly. It works at a clock frequency of 10.00MHz controlled by an external Quartz crystal oscillator (SCTF10.000) attached to its clock signal terminal. The input supply for the microcontroller must stay constant within a range of 4-5V. To achieve this, voltage regulator L7805 is attached in series with the source, which withholds the input within permissible limits. Source to this Voltage regulator is converted to DC form by a full wave rectifier connected in series with the input supply of the secondary transformer. Figure 1 shows the control circuit of dcPIC30F microcontroller.

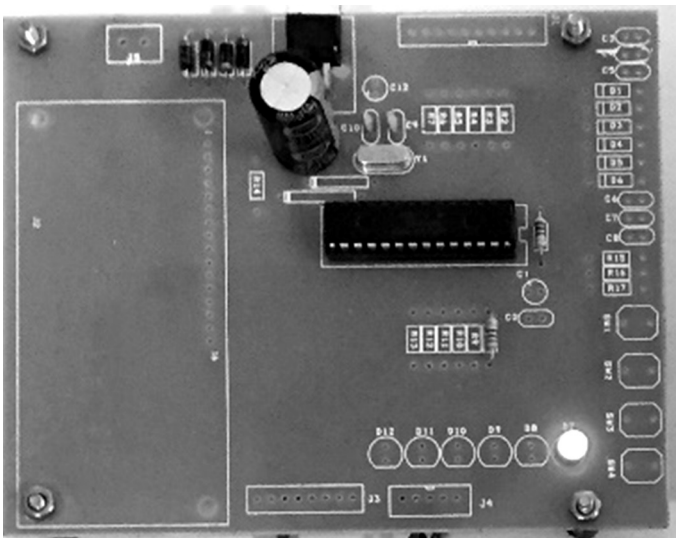

Figure 1: Control Circuit with dcPIC30F

A gate driver is a power amplifier that accepts a low-power input from a controller IC (dcPIC30F in this case) and produces a high-current drive input for the gate of a Power MOSFET. The switching signal for a Power MOSFET is usually generated by a logic circuit or a microcontroller, which provides

an output signal that typically is limited to a few milli-amperes of current. Consequently, a device which is directly driven by such a signal would switch very slowly, with correspondingly high power loss. Also, during switching, the gate capacitor of the MOSFET may draw current so quickly that it causes a current overdraw in the logic circuit or microcontroller, causing overheating which leads to permanent damage or even complete destruction of the chip. To prevent this from happening, a gate driver is provided between the microcontroller output signal and the power transistor.

In the implementation of this project, TLP250 has been used. Optical isolation is the primary advantage of using this driver when compared to other drivers. It is an 8-pin IC with input current threshold at 7-10mA and an ideal voltage input of 5V. Input supply is rectified by a full wave rectifier cascaded to each input. There are a total of 6 drivers in the circuit, 4 primary drivers and 2 backup drivers to provide firing pulses in the intermediate delay interstices. A capacitor of rating 470uF is attached to each driver so as to prevent damage to the drivers. Driver circuit of the proposed system shown in Figure 2.

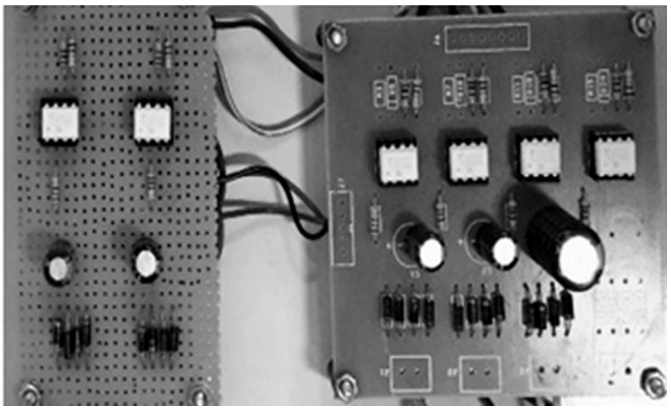

Figure 2: The Driver Circuit using TLP250

A power inverter, or inverter, is an electronic device or circuitry that changes direct current (DC) to alternating current (AC). A typical power inverter device or circuit will require a relatively stable DC power source capable of supplying enough current for the intended overall power handling of the inverter, which is provided by the secondary end of the transformer and subsequent rectification by a full wave rectifier configuration in this case. The circuit consists of a standard NPC single leg 3 step inverter, which is controlled by HSVM from the control circuit. The capacitors implementing the NPC structure are each rated 1000uF and are rated for a voltage of 50V. The switching operation is performed by Power MOSFETs IRF840 rated for 8A and 500V. The gate voltage threshold varies between +20V to –20V. Figure 3 shows single phase DC-TLI Inverter Circuit.

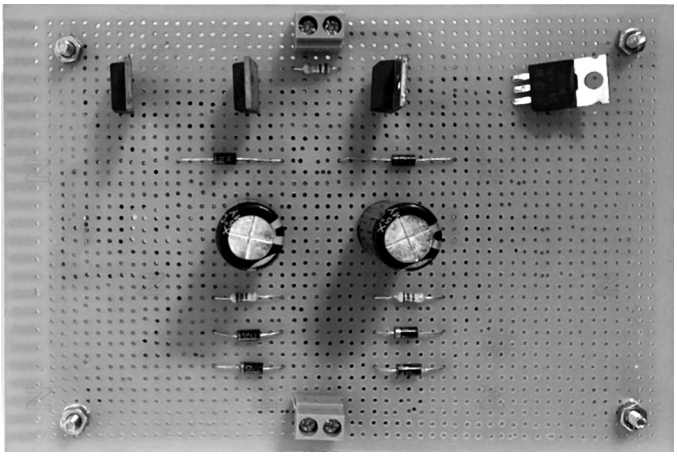

Figure 3: Single phase DC-TLI Inverter Circuit

4. HYSTERESIS SPACE VECTOR MODULATION

Hysteresis Space Vector Modulation is similar to SVPWM, but the vector represented in the stationary coordinate frame is the error vector. In the proposed system, the error vector is calculated as a difference of the output voltage from the MLI with respect to a predefined reference voltage giving better control over the DC Voltage balancing problem, and dynamically modify triggering pulses. The three error voltages derived from the output are represented using a single space vector. The DC bus voltage is balanced and a Space Vector Voltage Control is examined in order to use hexagonal small vectors and the outer portion contains 6 medium and 6 large vectors, making 27 vectors in all, each representing a switching state. The flowchart of HSVM process in shown in Figure 4.

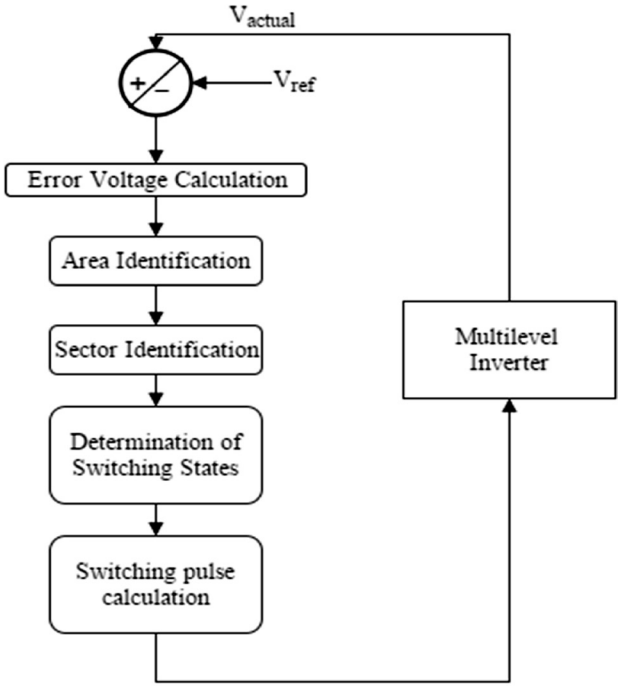

Figure 4: HSVM Algorithm Flowchart

5. EXPERIMENTAL RESULTS AND DISCUSSION

To authenticate the simulation results of the proposed system, experimental setup Voltage Controlled 3 Level NPC-MLI Based HSVM with Grid Connected PV System was designed and tested. The control strategy of the proposed system is shown in Figure 5. Staircase output voltage of 220.4 V is obtained at the inverter side and its THD analysis is shown in Figure 6 using split inductors a sinusoidal output of 220.4V is obtained which is fed to three phase grid connected system. Figure 7 shows the output current waveform of DC-TLI system.

The output waveforms are obtained on Digital Storage Oscilloscope (DSO). Hysteresis current control is implemented using DSPIC2813F microcontroller fed with 5V dc voltage. And experimental setup of the proposed system is shown in Figure 8.

6. CONCLUSION

This paper has offered hardware implementation of single phase DC-TLI using HSVM with PV system. The use of HSVM using hexagonal hysteresis make certain reduced THD and superior DC link voltage balancing in the capacitors of the DC-TLI topology, Reduced common mode voltage, and switching losses are various benefits of this control method. Simplified working of the HSVM configuration along with

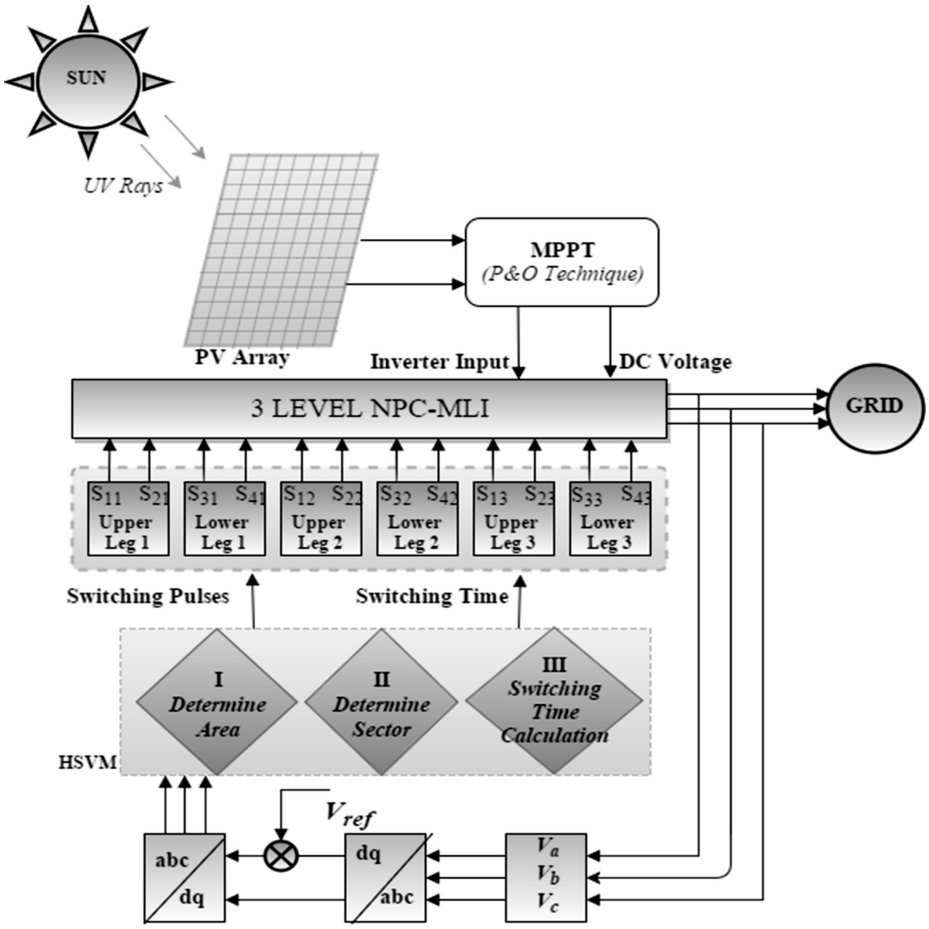

Figure 5: Control strategy for proposed system

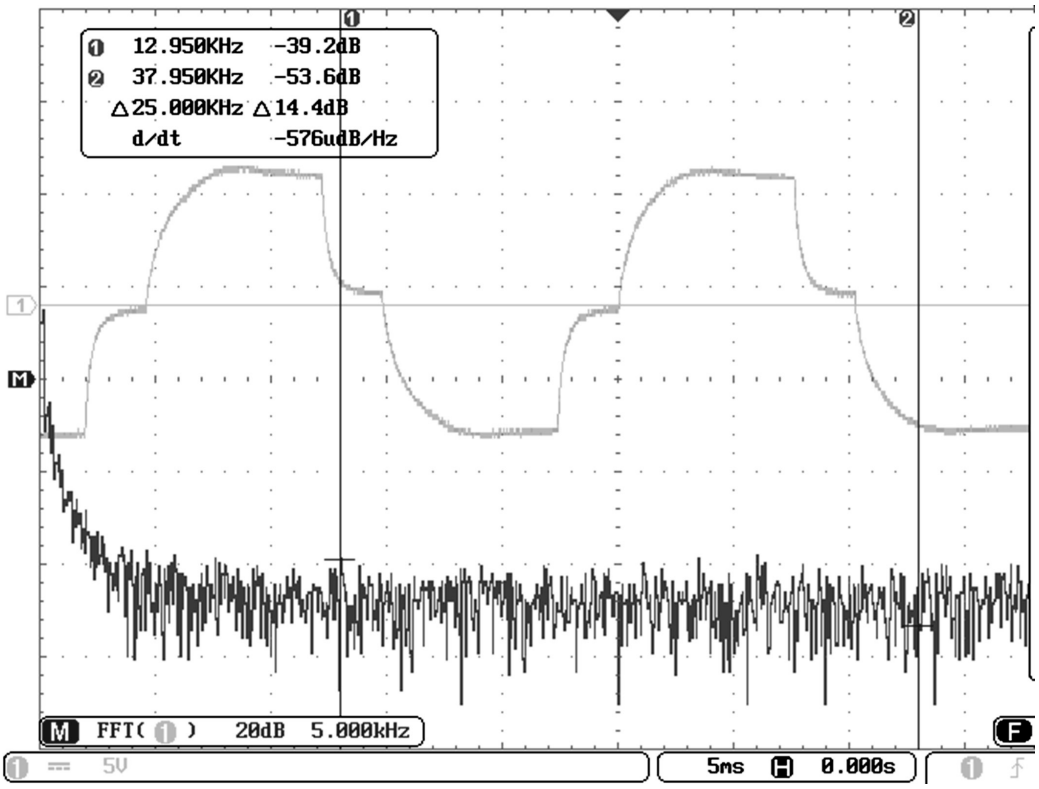

Figure 6. Split inductor based output voltage and it's THD analysis

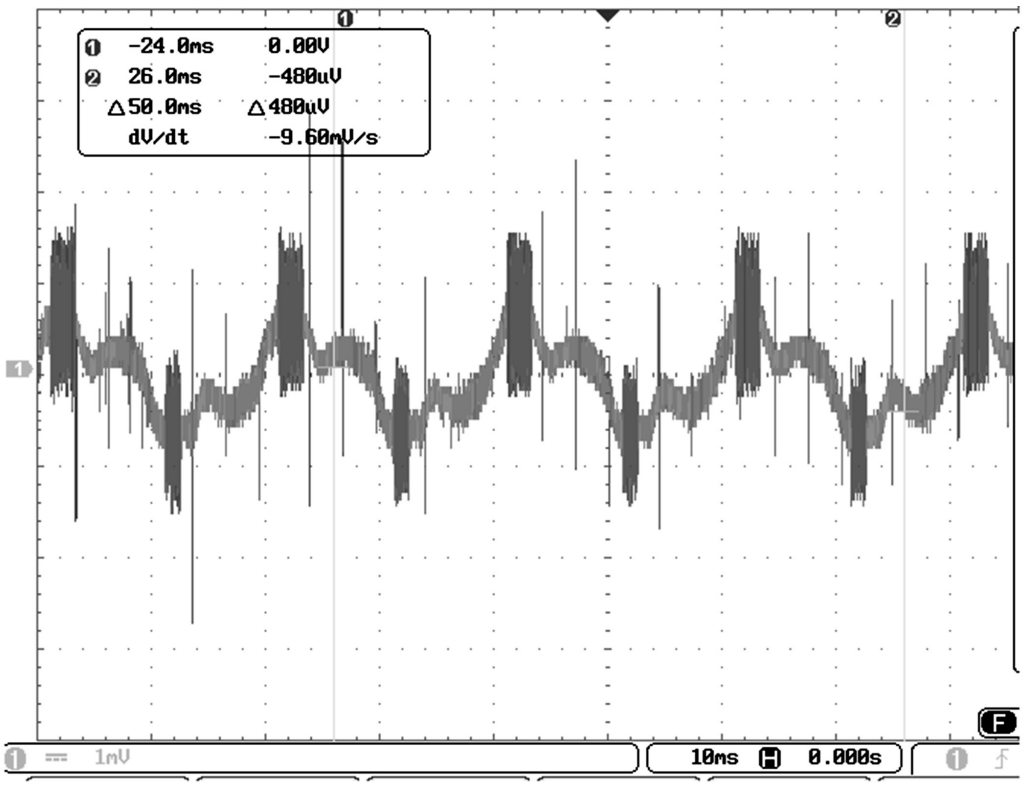

Figure 7: Output current waveform of DC-TLI system

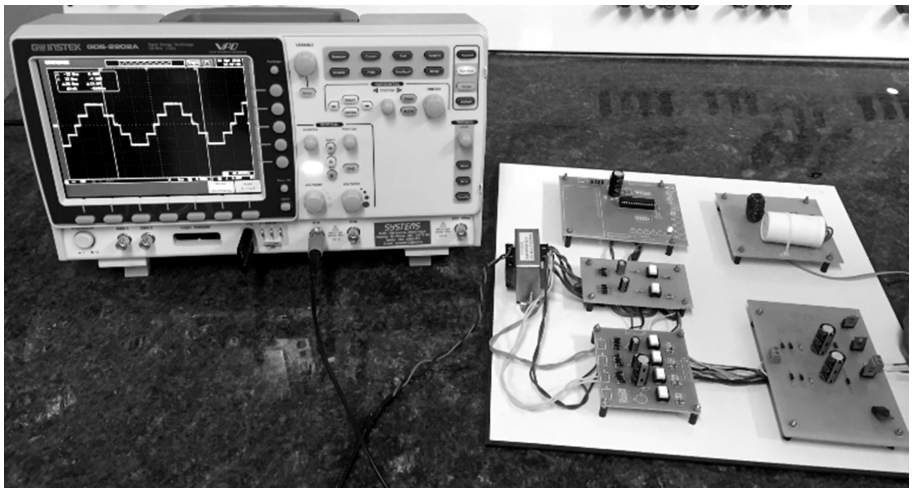

Figure 8: Experimental setup of the proposed system

precise calculations of switching time and vector location has been accessible. The hardware results were discussed with help dsPIC micro controller. For full elimination capacitor balancing problem and common mode voltage, this proposed system will extended for 3D-SVM technique.

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