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Optimized Low Leakage Design of Standard Cells and Accumulator Using Gate Length Biasing and Submicron Sleep Transistor Technique in Cadence and SOC Encounter

***Mrs. P.Ramani **Mrs. R.Kavitha Sudha ***Mrs. G.Priya**

Abstract : As technology is scaling into nanometers , the leakage current, power and area have become import parameters in circuit designing. The logic gates are specific elements in digital circuits.Gate length biasing is a method to optimize the design by varying the gate length so as to decrease power dissipation. The leakage power is the main contributor to the power consumption. Power gating and clock gating are used to minimize the power by switching off the unused transistors and clock using sleep transistor technique.

Keywords : Standard cell, gate length, power dissipation, sleep transistor, power gating , clock gating, leakage power.

1. INTRODUCTION

Energy dissipation in CMOS designs is mainly of two types .Its either static or dynamic. [1]. The Techniques to reduce the power dissipation in CMOS circuits

(*a*) Gate Length Blasing of Standard Cell

Power Delay Product is good compromise between speed and delay, which is written as [1]

$$EDP = E.\, t_{delay} \quad (1)$$

The basic gates are the important elements in digital circuits. In this paper, a two input Inverter is optimized using gate length biasing by varying gate length from 180 nm to 250 nm.

Submicron Technique and Optimized Sleep Transistor

Micron is the measurement of length. In Submicron technology, billions of transistors on a single die, working at GHz frequencies. Submicron condition is sub threshold condition.This method employs power gating.Power gating method is used to reduce the leakage power using sleep transistor.

In this work, several basic standard cell inverter is simulated with different gate lengths and delay and power is calculated .All simulation are performed using Spectre in cadence and delay and power are calculated.Also a RTL-to-GDSII design of a 4 bit accumulator is generated using RTL synthesis NClaunch and SOC encounter.Then Sub micron technique is used to design a low leakage accumulator. Power gating is implemented.

* M.E,(PhD), Assistant Professor, SRM university,Tamil Nadu, India,

** M.Tech, Assistant Professor, SRM university, Tamil Nadu, India

*** M.Tech, Assistant Professor , SRM university, Tamil Nadu, India

2. GATE LENGTH BIASING METHODOLOGY

The gate-length biasing (GLB) technology increases the channel length of transistors and reduces leakage exponentially in both active and standby modes [6]. In this work a testcase is designed in cadence virtuoso 9.1. The design is of two input inverter in 180nm. Spectre simulation is performed.Delay is calculated and leakage power is calculated.

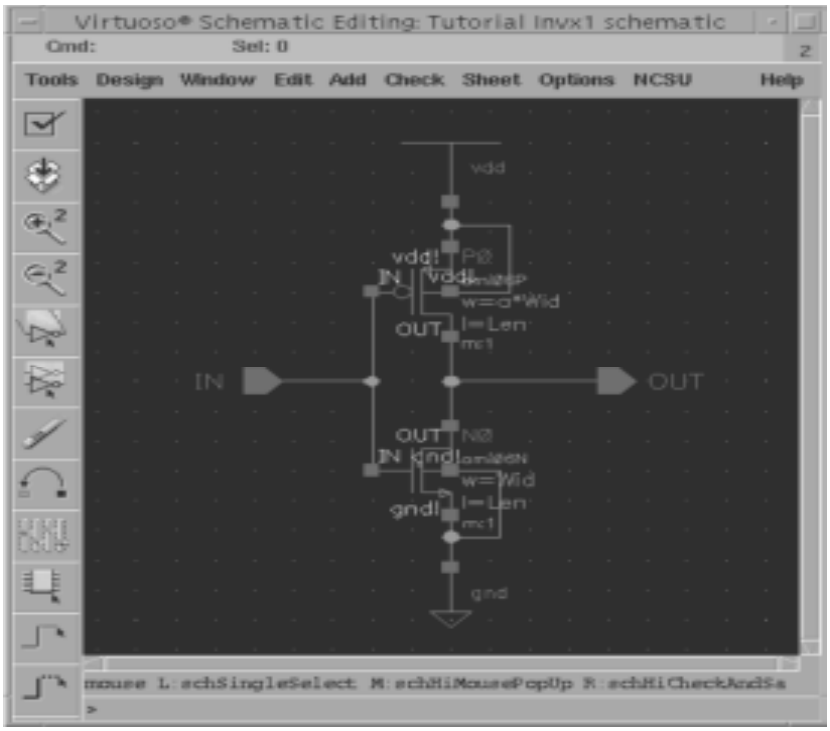

Fig. 1. Schematic of two input inverter incadence virtuoso 9.1.

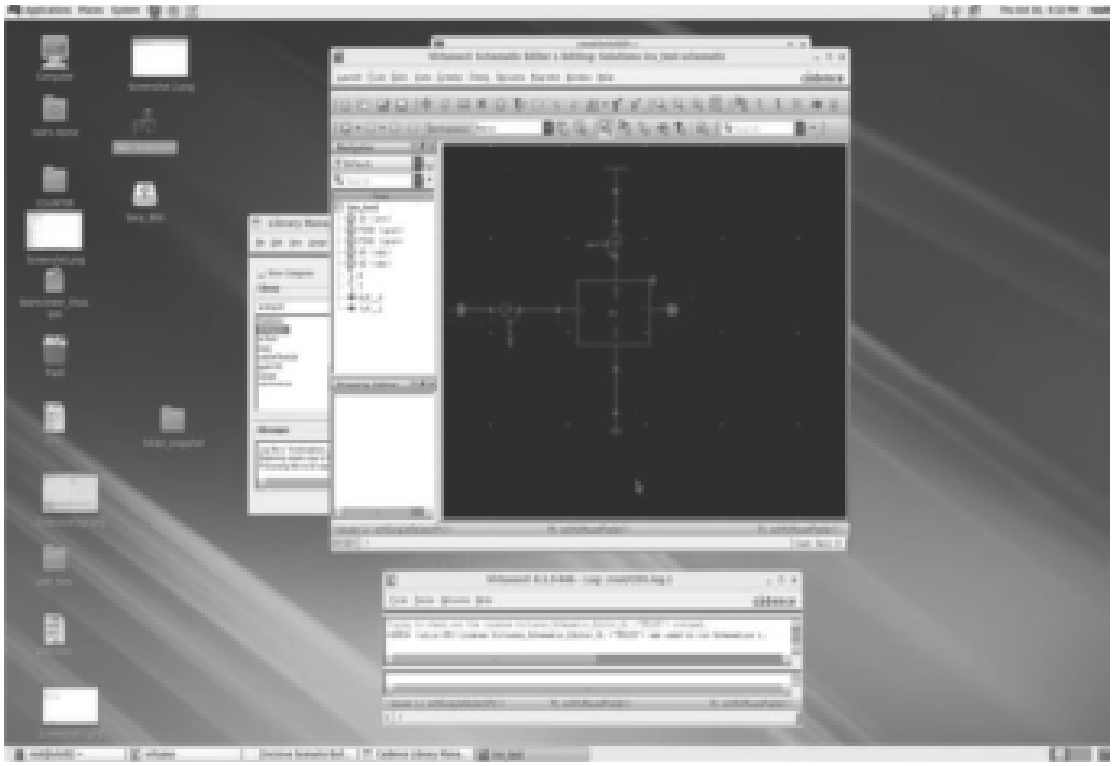

Fig. 2. Testcase of inverter in cadence.

Spectre simulation is performed in cadence. DC and Transient analysis are performed.

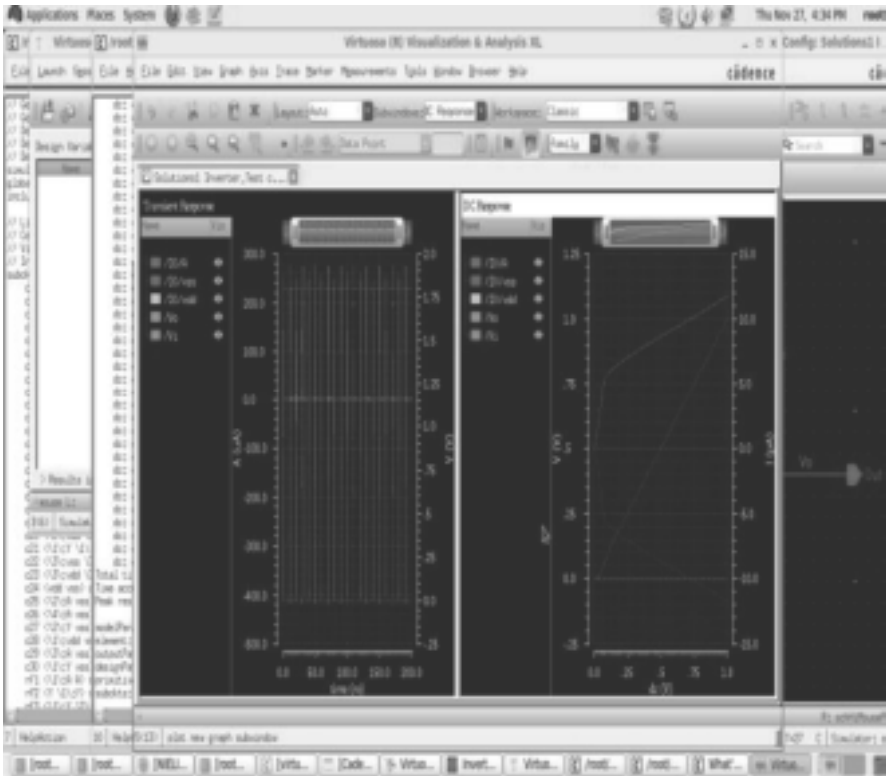

Fig. 3. DC and Transient analysis of inverter using spectre simulation

Next Delay and power dissipation is calculated.

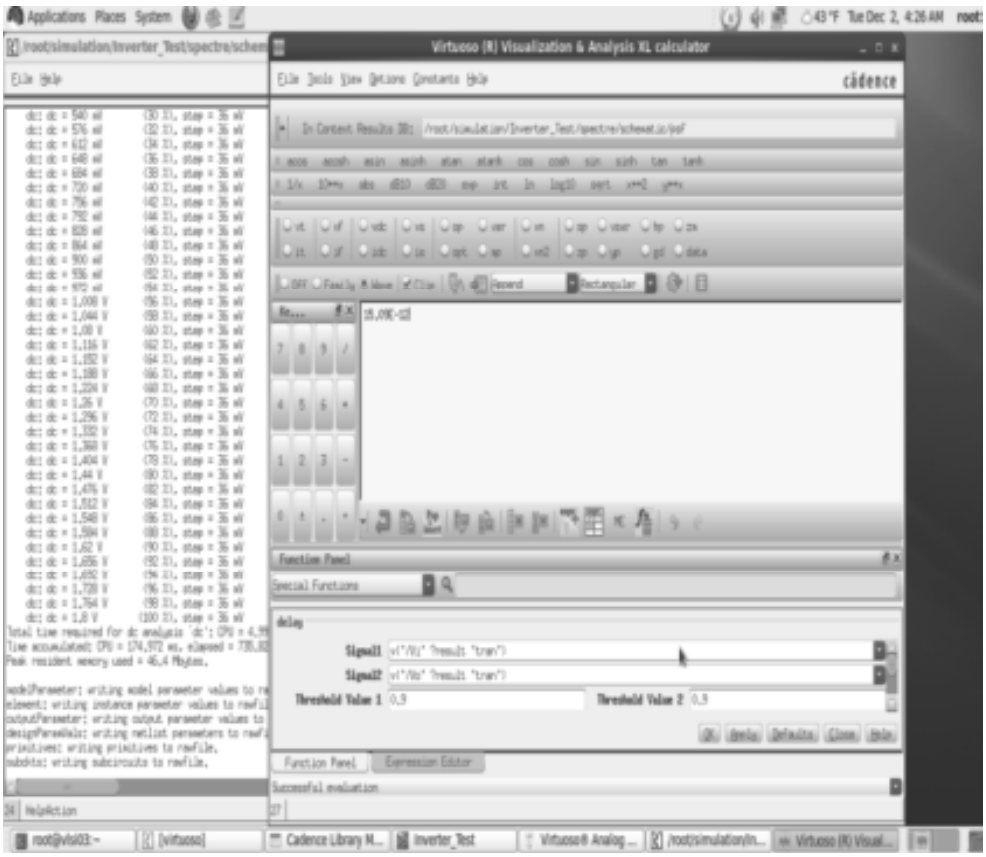

Fig. 4. Delay calculation using virtuoso tool

Next , values of gate length of inverter cell are changed to bating different values of power dissipation and delay.

Following are the value of delay and power dissipation calculated when gate length is varied from 180, 200, 250nm.

Table 1. Delay and power dissipation value for differentgate length.

Gatelength(nm)	*Delaycalculation(ps)*	*Powerdissipated(pw)*
180	13.65	61.7
200	15.09	59.7
250	18.89	50.8

Thus the value of Power dissipation decreases exponentially on increasing the gate length of design

As the gate length is increased we observe that leakage power decreases.This concept can be used to design circuits employing standard cells .By using gate length biased cells instead of normal standard cells.This is however at cost of increased delay. Hence optimized design is obtained.

3. SUBMICRON TECHNIQUE AND OPTIMIZED SLEEPTRANSISTOR

Firstly a four bit ALU is designed using RTL synthesis, NClaunch and SOC encounter . The full RTL to GDS flow is performed to obtain the design.

RTL to GDS flow

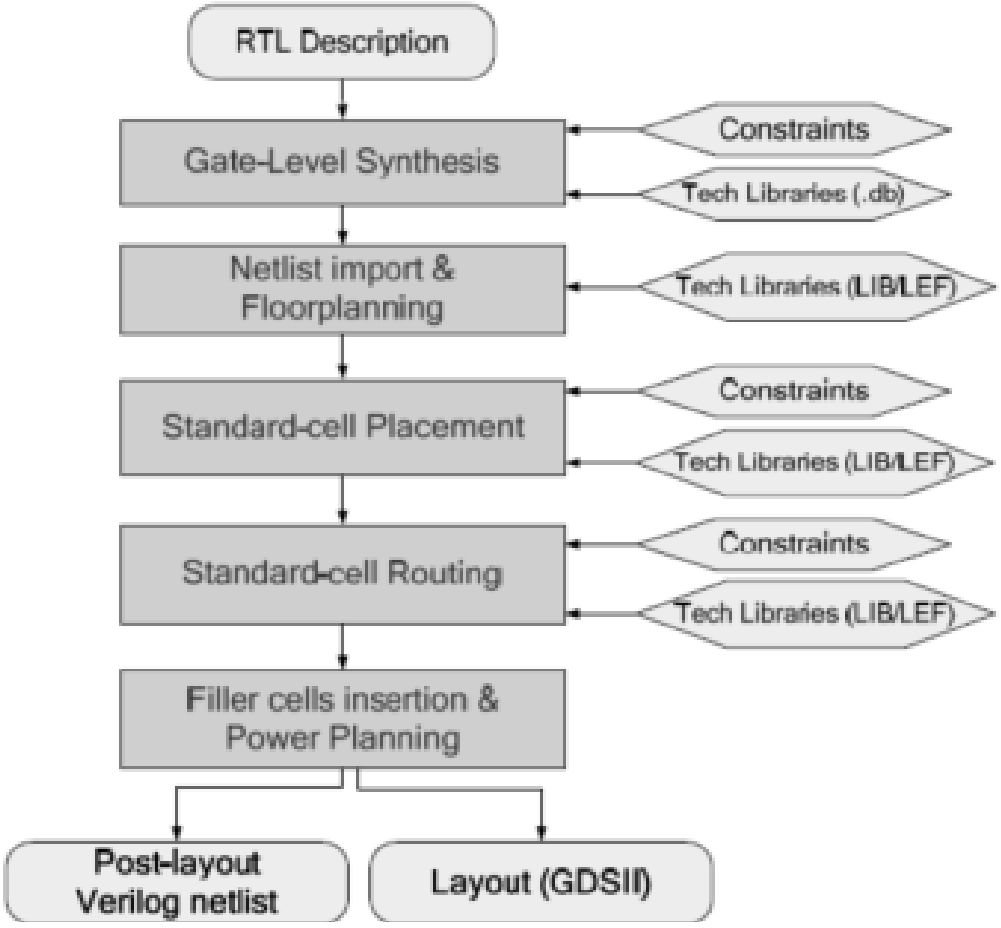

Fig. 5. Flow diagram of complete RTL to GDS [5]

Leakage power is calculated is calculated as 13.757 *n*W.

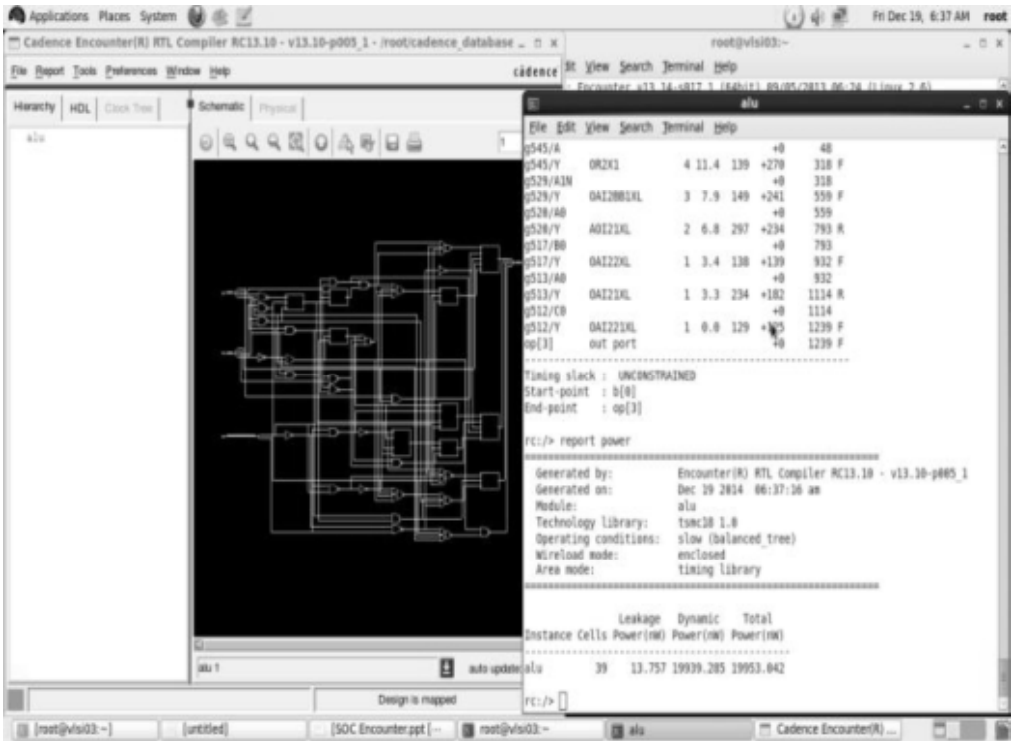

Fig. 6. Leakage power calculation of 4 bit ALU design

Floorplanning and Routing of design are performed in SOC Encounter.

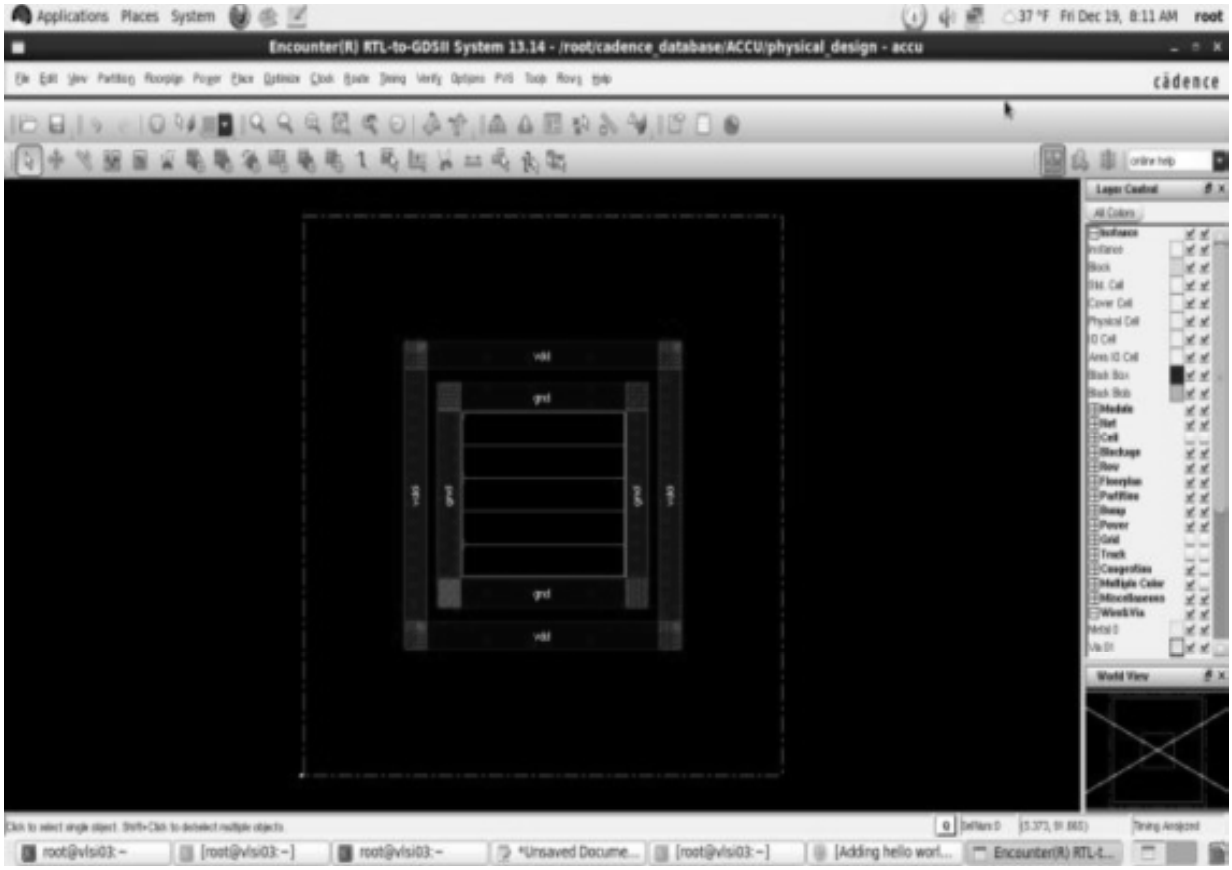

Fig. 7. Floorplanning of alu.

Thus ALU is designed as shown in figure 8.

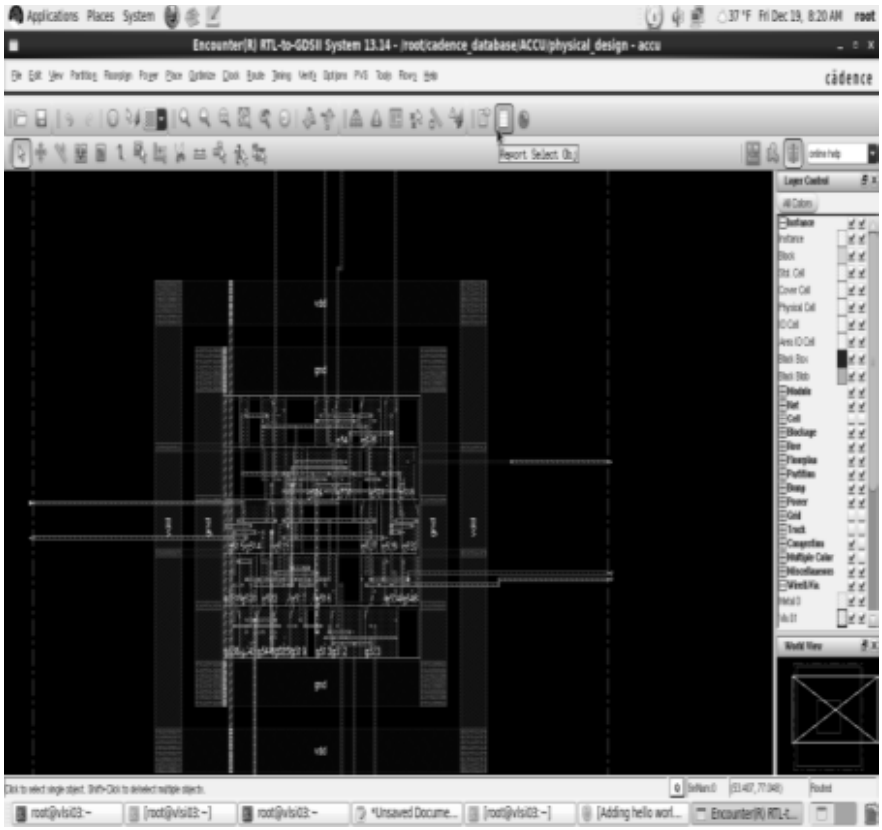

Fig. 8. Complete design of ALU in SOC encounter

4. SLEEP MODE POWER GATING

Power-gating technique or sleep mode sub micron technique uses a high Vth sleep transistor in series with the pull-up and/or the pull-down of a low Vth logic block to reduce leakage power.

Delay of a single gate without sleep mode is given as [7]

$$\tau d = \frac{C_L V_{DD}}{(V_{DD} - V_{tL})^{\alpha}} \quad (1)$$

Where, VDD is the supply voltage, VtL is low level threshold voltages, á is Saturation Velocity Index and CL is the load capacitance.

If a sleep transistor of High Vt is introduced, we get delay as

$$\tau d^{\,sleep} = \frac{C_L V_{DD}}{(V_{DD} - Vx - V_{tL})^{\alpha}} \quad (2)$$

Allowing 5% overhead in the delay for this design, we get

$$\frac{\tau d}{\tau d^{\,sleep}} = 95\% \quad (3)$$

The current through the sleep transistor is represented approximately by

$$I_{Sleep} \approx \mu_n C_{ox} \left(\frac{W}{L}\right)_{Sleep} (V_{DD} - V_{tL})(V_{DD} - V_{tH}) \quad (4)$$

Where, ìn is mobility of electrons = 150 cm^2/V.s at 90°C, C_{ox} is oxide capacitance = 19.7 X 10^{-6} F/m for 45nm [7].

So the width over length ratio of a sleep transistor is given by

$$\left(\frac{W}{L}\right)_{Sleep} = \frac{I_{Sleep}}{0.0281\,\mu_n C_{ox}\,(V_{DD} - V_{tL})\,(V_{DD} - V_{tH})} \quad (6)$$

I_{sleep} is calculated by simulating the ALU circuit without sleep transistor network and finding maximum current that flows through ground.

5. CONCLUSION AND FUTURE WORKS

The Gate length biasing is an effective method to reduce the power dissipation. As gate length is increased from 180nm to 250 nm, the paw dissipated decreases exponentially and delay increases linearly.Thus design is optimized. Also a complete RTL to GDS flow of a Accumulator is performed in SOC encounter. Power gating sleep mode transistor method reduces the leakage power consumption of a combinational logic block during inactive state. In sleep transistor mode, 99% of the total power consumption is saved. The switching currents/ fluctuations can be further reduced by applying a constant low leakage vector at the input of the circuit during sleep mode.In future, this power gating method can be applied to other combinational and sequential blocks like PLA, ROM, and RAM with higher bytes etc.

7. REFERENCES

1. Jan M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice-Hall, Inc., Upper Saddle River, NJ, 1996.
2. A. Agarwal, C. H. Kim, S. Mukhopadhyay and K. Roy, "Leakage in Nano-Scale Technologies: Mechanisms, Impact and Design Considera- tions," in Proc. ACM/IEEE Design Automation Conference, 2004, pp. 6– 11.
3. A. Wang, B. H. Calhoun, and A. P. Chandrakasan., Sub-threshold Design for Ultra Low-Power Systems, Springer, 2006.
4. R. Gonzalez, et al., "Supply and threshold voltage scaling for low power CMOS," *JSSC*, vol 32 (8), pp. 1210-1216, 1997.
5. Cadence Abstract Generator User Guide, Product Version 5.1.41
6. P. Gupta, A. B. Kahng, P. Sharma, and D. Sylvester, "Gate-length biasing for runtime- leakage control", IEEE Trans. on Computer- Aided-Design, Vol.25 (8), pp. 1475-1485, 2006
7. David Chinnery, Kurt Keutzer, "Closing the Power Gap Between ASIC & Custom, Tools and Techniques for Low-Power Design", chapter 10 authored by Jerry Frenkil, co-author Srini Venkatraman, Springer
8. Y. Ye, S. Borkar and V. De, "A New Technique for Standby Leakage Reduction in High- Performance Circuits," in *Proc. Symposium on VLSI Circuits*, 1998, pp. 40–41.