I J C T A, 9(2) 2016, pp. 639-653

Development of a New Boost Multilevel Inverter Topology with Reduced Switch Count

R. Gandhi Raj[*], S. Palani[**] and H. Habeebullah Sait[***]

ABSTRACT

This paper presents a new topology of boost multilevel inverter, to achieve thirteen level inverter output voltages with twice the input voltage. The significant features of the proposed topology are; reduction of the switch count, reduction of switching losses, reduction of the gate drive power supply unit and the provision of a galvanic isolation between load and sources by a mid-point transformer. An exhaustive comparison has been made of the existing multilevel inverter topology and the proposed topology. A computer aided simulation has been carried out to analyze the performance of the proposed topology with resistive, resistive-inductive loads are simulated in MATLAB environment.

Keywords: Multilevel Inverter (MLI), cascaded boost, mid-point transformer, Total Harmonic Distortion (THD)

I. INTRODUCTION

Recently, power electronics researchers have been working towards the development of a topology in multilevel inverters, because of the following reasons; it has higher voltage operating capability, reduced rate of change of voltage (dv/dt), lower common mode voltages, reduced harmonic content, smaller input and output filter, reduced switching and conduction losses, and increased efficiency. Multilevel inverters are considered as one of the industrial solutions for high dynamic performance and power quality demanding applications. The researchers are contributing to further improve energy efficiency, reliability, power density, simplicity and cost of multilevel inverters as they become more attractive and competitive than classical topologies [1], [2]. There are three classical topologies such as; Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascade H-bridge (CHB). Each topology has its own merits and drawbacks. The NPC topology has been employed in industry up to three levels, in view of the fact that, the number of clamping diodes needed to share the voltage increases dramatically, and together with the increase in difficult to control the DC link capacitor voltage unbalance. In a flying capacitor topology, an excessive number of storage capacitors are required, when the number of converter levels is high. Thus, the inverter control will be very complicated and high switching frequencies are necessary to keep the capacitors properly balanced and hence, switching losses will be high. The cascaded H-bridge MLI is well suited for high power applications because of the modular structure. However, the CHB topology needs separate dc sources for real power conversion. In general, multilevel inverters have some disadvanges such as, excessive number of switching components, more gate driver circuits resulting in increased cost, and complex control circuits which limit their applications [3], [4]. To overcome these problems many novel topologies of multilevel inverters are presented [5]-[13].

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In [10] the authors presented a cascaded transformer based multilevel inverter, which utilized twelve unidirectional switches, twelve diodes, two isolated power supplies and two cascaded transformer to develop a nine level output voltage. This topology has more in conduction and switching losses and less efficiency, because at any instant of time, three switches need to be turned on to gets a single step of output voltage.

The proposed inverter configuration of the single phase multilevel inverter consists of ten unidirectional switches, a three series connected capacitor, a single input power supply unit, and two mid-point transformers to develop a thirteen level output voltage. The aim of developing the proposed topology is, to boost the inverter output voltage with single input cascaded configuration, to reduce the number of power switches and driver circuits, to reduce the gate driver power supply unit. The proposed topology has inherent features such as a galvanic isolation between an input dc source and output loads, and ensures the reliability of the inverter. A computer aided simulation and experimental results are used to justify the new topology and to show the validity of the presented inverter structure for real time applications.

This paper is organized as follows: Section II presents the structure of the proposed inverter and also explains the detailed mode of operation of the proposed thirteen level inverter with mathematical formulations. Section III addresses the power loss calculation for the proposed inverter. Section IV investigates the detailed simulation results of the proposed inverter. Section V focuses on the comparison of the proposed topology with classical and recent topologies. Section VI discuss with conclusion.

II. PROPOSED INVERTER TOPOLOGY

The proposed Boost configuration of the single-phase thirteen-level inverter comprises ten unidirectional power switches, a two mid-point transformer and a capacitor voltage divider network, which is formed by the series connection of two equal value capacitors C_1, C_2 and C_3 as depicted in Fig. 1.

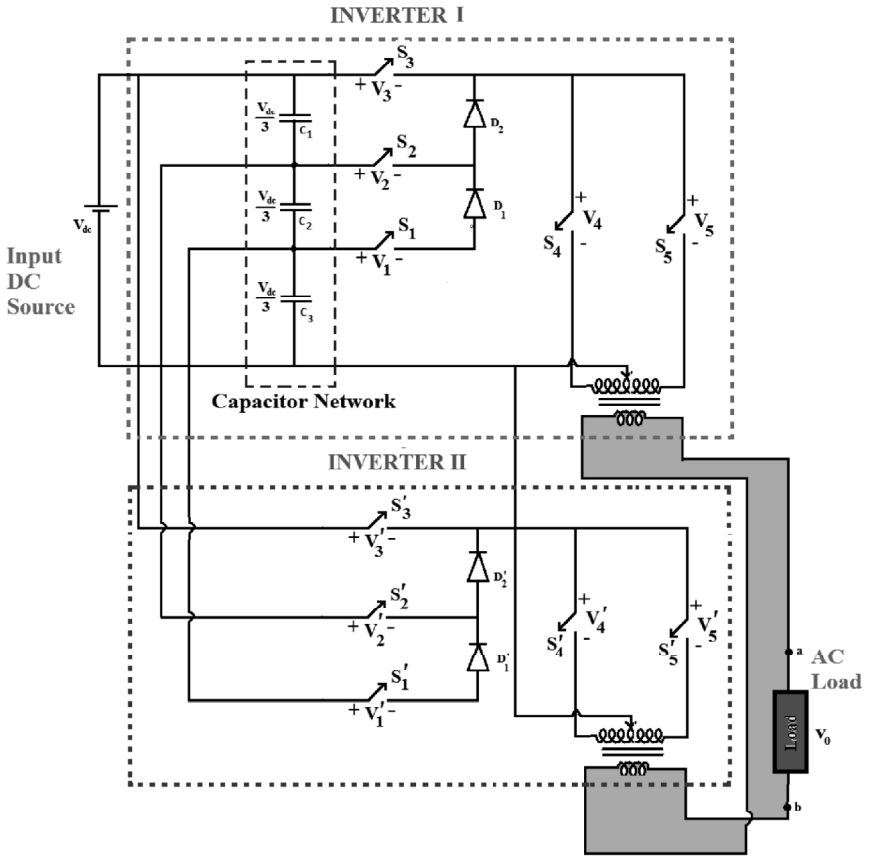


Figure 1: Circuit diagram of the proposed Single phase cascaded boost thirteen level inverter topology

The supply voltage (V_{dc}) is divided into three equal values, by means of the capacitor divider network. Each capacitor has a voltage of $V_{dc}/3$. The proposed inverter can produce an output of thirteen levels such as; $2V_{dc}$, $5V_{dc}/3$, $4V_{dc}/3$, V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, 0, $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$, $-4V_{dc}/3$, $-5V_{dc}/3$, $-2V_{dc}$ from the constant input dc voltage of V_{dc}. The switches $S_{1,}$ $S_{2,}$ $S_{3,}$ $S_{1',}$ $S_{2',}$ and $S_{3'}$ are determine the level of the output voltage, and the switches S_4, S_5 and S_4, $S_{5'}$ are decide the polarity of the output voltage. The number of output voltage levels (N_{STEP}), and the required number of IGBTs (N_{IGBT}) can be synthesized as;

$$N_{STEP} = 4\,N_C + 1 \tag{1}$$

$$N_{IGBT} = 2\,N_C + 4 \tag{2}$$

where, N_c is the number of capacitors. Here, the number of capacitors decides the output voltage level.

Fig. 2 indicates the typical thirteen-level inverter output voltage waveform for understanding the modes of operation of the proposed inverter. The switching state of the proposed inverter is such that, at any instant of time, four power switches are in the conducting state and the other devices are in the non-conducting state. The proposed inverter has a reduction in conduction and switching losses because the switches are operating at fundamental frequency, which results in an increase in the efficiency of the proposed inverter.

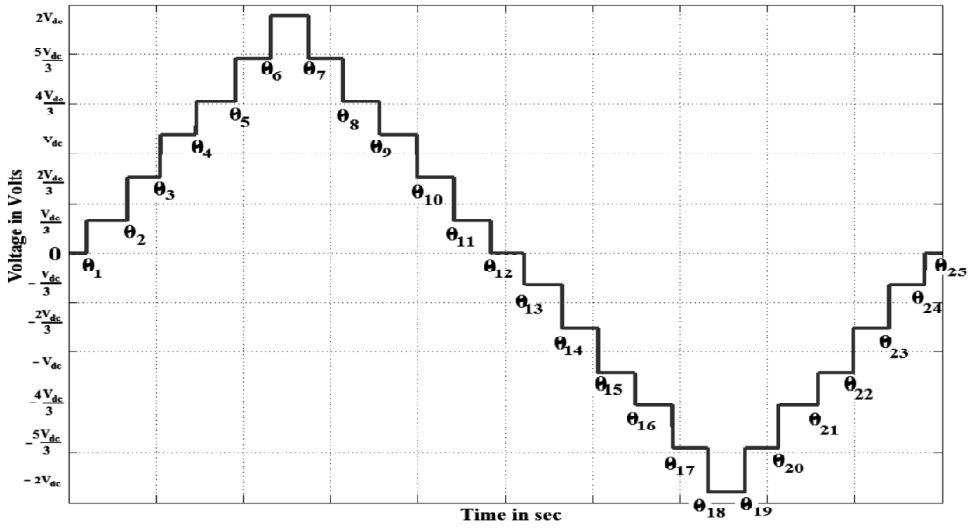


Figure 2: Typical stepped thirteen level inverter output voltage waveform

To understand the operation of the proposed inverter, the production of positive output voltage are explained using seven switching states, as shown in Fig. 3 (a)–(g). Here, the red line represents the conduction path of the current flow. The positive cycle output voltage levels are generated as follows.

Mode 1: Output voltage of $+2V_{dc}$

Fig. 3(a) shows the switching state resulting in an output voltage +2Vdc. When level modulated switch $S_{3,}$ $S_{3'}$ and polarity modulated switch S_4, $S_{4'}$ are kept ON, three capacitors ($C_{1,}$ C_2 and C_3) are connected in series, and they supply energy to the load. The load current flows from the terminal **a** to **b** and the voltage across the load terminals is +2Vdc.

Mode 2: Output voltage of $+5V_{dc}/_3$

Fig. 3(b) depicts the switching state delivering an output voltage $+5V_{dc}/_3$. When level modulated switch $S_{3,}$ $S_{2'}$ and polarity modulated switch S_4, $S_{4'}$ are kept ON, three capacitors ($C_{1,}$ C_2 and C_3) are connected in series, and they supply energy to the load. The load current flows from terminal **a** to **b** and the voltage across the load terminals is $+5V_{dc}/_3$.

Mode 3: Output voltage of $+4V_{dc}/_3$

Fig. 3(c) illustrates the switching state generating an output voltage of $+4V_{dc}/_3$. When level modulated switch S_3, S_1, and polarity modulated switch S_4, S_4, are kept ON, three capacitors (C_1, C_2 and C_3) are connected in series, and they supply energy to the load. The load current flows from terminal **a** to **b** and the voltage across the load terminals is $+4V_{dc}/_3$.

Mode 4: Output voltage of $+V_{dc}$

Fig. 3(d) shows the switching state generating an output voltage of V_{dc}. When level modulated switch S_3, and polarity modulated switch S_4, S_5, are kept ON, three capacitors (C_1, C_2 and C_3) are connected in series, and they supply energy to the load. The load current flows from terminal **a** to **b** and the voltage across the load terminals is $+V_{dc}$.

Mode 5: Output voltage of $+2V_{dc}/_3$

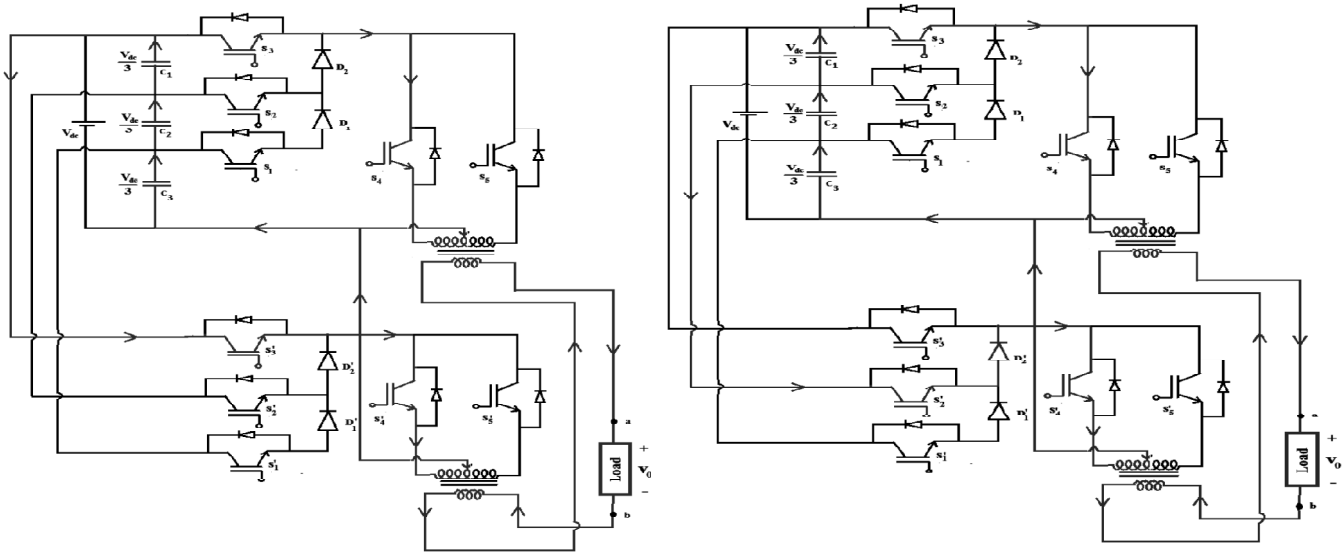
Fig. 3(e) indicates the switching state generating an output voltage of $+2V_{dc}/_3$. When level modulated switch S_2 and polarity modulated switch S_4, S_5, are kept ON, two capacitors (C_2, and C_3) are connected in series and supply energy to the load. The load current flows from terminal **a** to **b** and the voltage across the load a terminal is $+2V_{dc}/_3$.

Mode 6: Output voltage of $+V_{dc}/_3$

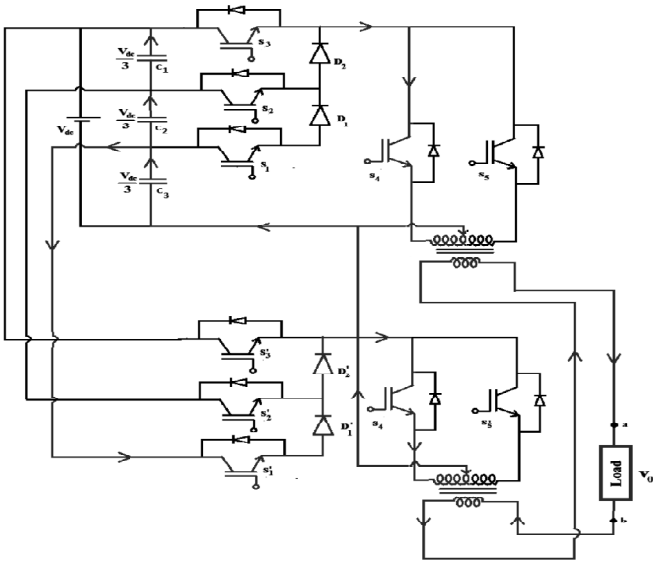
Fig. 3(f) shows the switching state generating an output voltage of $+V_{dc}/_3$. When level modulated switch S_1 and polarity modulated switch S_4, S_5, are kept ON, capacitor (C_1) supply energy to the load. The load current flows from terminal **a** to **b** and the voltage across the load a terminal is $+V_{dc}/_3$.

Mode 7: Output voltage of Zero.

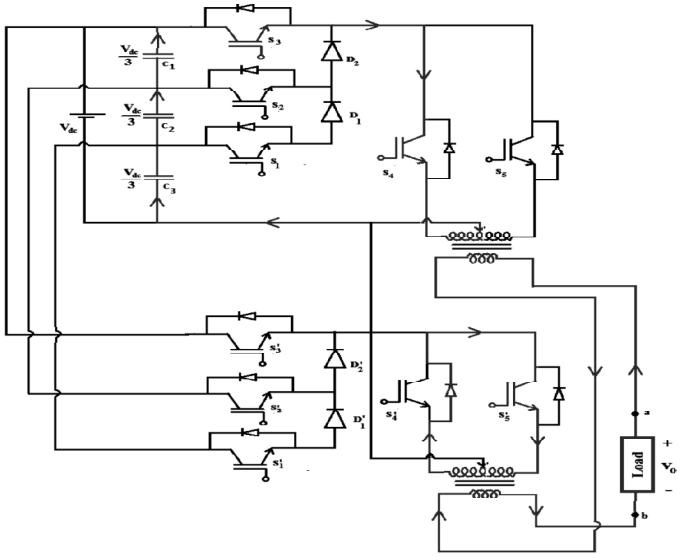
Fig. 3(g) indicates the switching state generating an output voltage of Zero. When polarity modulated switches (S_5 and S_5,) are kept ON, the primary winding of transformers are short circuited. Then the voltage across the load a terminal is Zero.



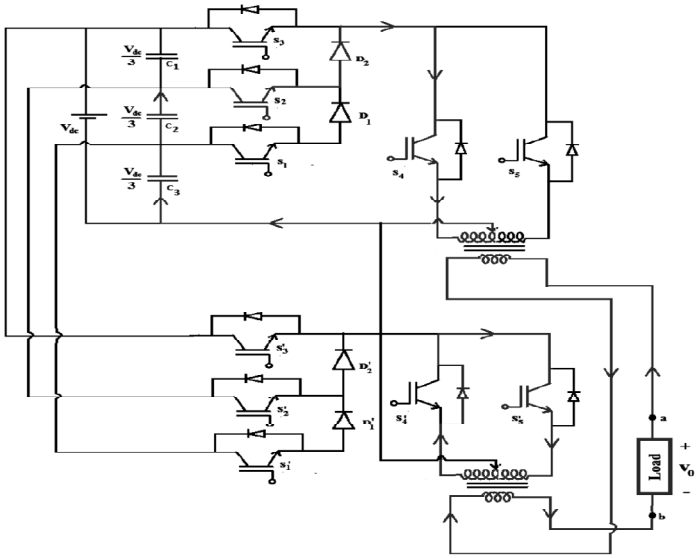
(a) **(b)**



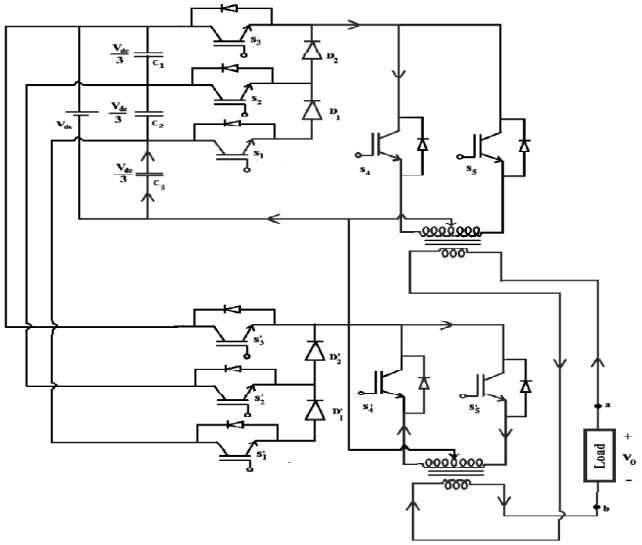
(c)



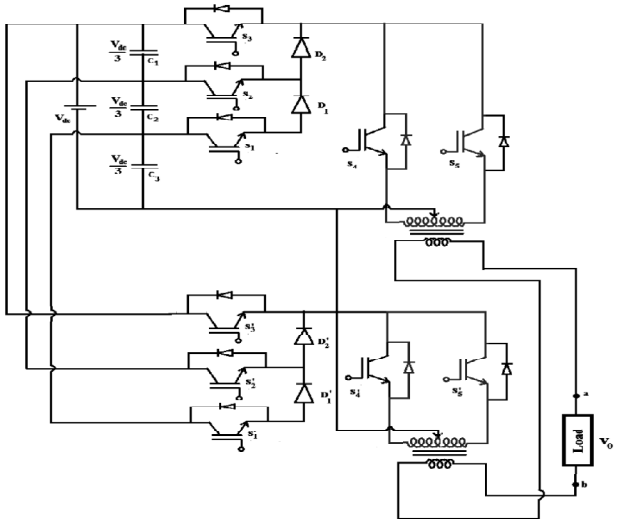
(d)



(e)



(f)



(g)

(A) Mathematical Formulation

The mathematical formulation for the proposed inverter is as follows; Let D_j be a switching function corresponding to switch K_j (j=1 to n) defined as

$$D_j = \begin{cases} 1 \quad ; \quad if \ \ switch \quad K_j \ \ is \ \ ON \\ 0 \quad ; \quad if \ \ switch \quad K_j \ \ is \ \ OFF \end{cases} \tag{4}$$

For $V_O \leq V_{dc}$; the inverter output voltage $V_O(t)$ can be expressed in terms of nodal voltage $V_j(t)$ as

$$V_O(t) = \sum_{j=1}^{N_C} V_j(t) \tag{5}$$

Where,

$$V_j(t) = (1 - D_j)\left(\frac{j}{3}\right) \times V_{dc}$$

$$V_o(t) = \sum_{j=1}^{N_c} (1 - D_j)\left(\frac{j}{3}\right) \times V_{dc} \tag{6}$$

For $V_O > V_{dc}$; the inverter output voltage $V_O(t)$ can be expressed in terms of nodal voltage $V_j(t)$ as

$$V_O(t) = \sum_{j=1}^{N_C} V_j(t) + V_{dc} \tag{7}$$

$$V_o(t) = \sum_{j=1}^{N_c} (1 - D_j)\left(\frac{j}{3}\right) \times V_{dc} + V_{dc} \tag{8}$$

The instantaneous inverter output current of the proposed inverter,

$$i_j(t) = D_j(t) \times i_o(t) \tag{9}$$

III. POWER LOSS CALCULATIONS

The total power loss is calculated by the summation of the switching loss and conduction loss. The details of the switching loss and conduction loss calculations are given below.

(A) Switching Loss

The switching waveforms are represented by linear approximation to the actual waveforms in order to simplify the discussion. When the switch is turned on by applying a positive gate signal to the switch, the current builds up to the maximum value of I_o at the time of t_{ri} (current rise time) and the switch voltage falls to V_{on} - at the time of t_{fv} (voltage fall time) as shown in Fig. 4.

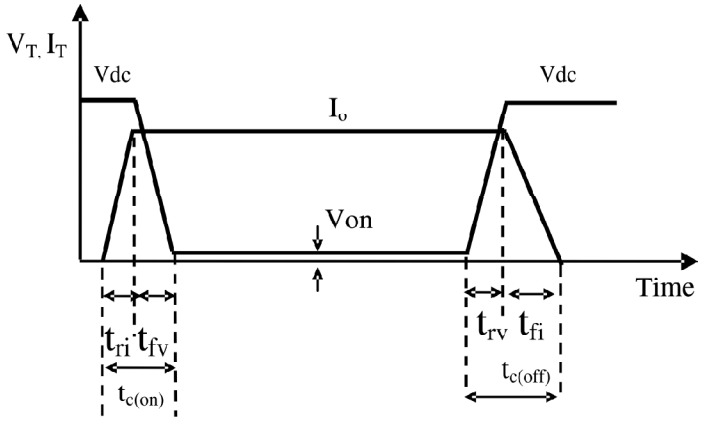


Figure 4: Instantaneous switch waveform

During the turn on cross over interval $t_{c(on),}$ large values of the switch voltage and current are present simultaneously [14]. The turn on cross over interval is

$$t_{c(on)} = t_{ri} + t_{fv} \tag{10}$$

The Energy dissipated in the device during $t_{c(on)}$ can be expressed as

$$W_{C(on),j} = \int_0^{t_{c(on)}} v(t)i(t)dt \tag{11}$$

$$W_{c(on)} = \int_0^{t_{c(on)}} \left[\left\{ V_{O,j} \frac{t}{t_{c(on)}} \right\} \left\{ -\frac{I_o}{t_{c(on)}} \left(t - t_{c(on)}\right) \right\} \right] dt \tag{12}$$

$$W_{c(on),j} = \frac{1}{6} V_{o,j} I_o t_{c(on)} \tag{13}$$

During the turn off transition, the voltage builds up to the maximum voltage of V_{dc} at the time of t_{rv} (voltage rise time), and the current in the switch, falls to zero value at the time of t_{fi} (current fall time). During the turn off cross over interval $t_{c(off),}$ large values of switch voltage and switch current are present simultaneously.

The turn off cross over interval is

$$t_{c(off)} = t_{rv} + t_{fi} \tag{14}$$

The energy dissipated in the switch during the turn off transition can be written as

$$W_{c(off),j} = \int_0^{t_{c(off)}} v(t)i(t)dt \tag{15}$$

$$W_{C(off)} = \int_0^{t_{c(off)}} \left[\left\{ V_{O,j} \frac{t}{t_{c(off)}} \right\} \left\{ -\frac{I_o}{t_{c(off)}} \left(t - t_{c(off)}\right) \right\} \right] dt \tag{16}$$

$$W_{c(off),j} = \frac{1}{6} V_{o,j} I_o t_{c(off)} \tag{17}$$

The total switching loss can be calculated as,

$$p_s = \sum_{j=1}^{2N_c+4} \left[\frac{1}{6} V_{o,j} I_o \left(t_{c(on)} + t_{c(off)}\right) f_j \right] \tag{18}$$

where f_j is the switching frequency, and the j^{th} switch makes f_j number of transitions; and I_o is the current through the switch after turning on and before turning off. In classical topologies all the switches are operated at a high switching frequency (f_s), but in the proposed topology ($N_{IGBT} - 4$) switches are operated at a high switching frequency, and the remaining four switches are operated at the fundamental frequency (f_o). Hence, the switching power loss equation for the proposed topology can be expressed as,

$$p_s = \delta \left\{ \sum_{j=1}^{2N_c} \left(\frac{j}{3} \right) V_{dc} \; f_s + 4 \left(2 V_{dc}\right) f_o \right\} \tag{19}$$

where $\delta = \frac{1}{6} I_o \left(t_{c(on)} + t_{c(off)}\right)$ is constant.

(B) Conduction Loss

The instantaneous conduction loss of a typical insulated gate bipolar transistor (IGBT) is:

$$p_{c,}T(t) = [V_T + R_T i^{\alpha}(t)]i(t) \tag{20}$$

The instantaneous conduction loss of a typical diode is

$$p_{c,}D(t) = [V_D + R_D i(t)]i(t) \tag{21}$$

where V_T, and V_D are the on state voltage drop of the IGBT and the diode. R_T, and R_D are equivalent to an on-state resistance of the IGBT and the diode, α is the gain constant of IGBT. The average conduction loss can be expressed as,

$$p_{c(avg)} = \frac{1}{\pi}\int_0^{\pi}\left[\{N_T(t)V_T + N_D(t)V_D\}i_o(t) + \{N_T(t)R_T i_o^{\alpha+1}(t)\} + \{N_D(t)R_D i_o^2(t)\}d(\omega t)\right] \tag{22}$$

For the proposed topology, only four switches bear $2V_{dc}$ and the voltage across the remaining switches is $\left(\frac{j}{3}\right)V_{dc}$. The conduction losses for the proposed multilevel inverter can be calculated from the following equation;

$$p_{c(avg)} = \sum_{j=1}^{2N_C}\left(\frac{j}{3}\right)V_{dc}I_o + I_o^2R_T + 4(2V_{dc})I_o + \sum_{j=1}^{2N_C-2}V_D I_o + I_o^2 R_D \tag{23}$$

In the proposed inverter, the level modulated switches have a PIV of less than or equal to V_{dc}, and the remaining four polarity changed power switches have a PIV of $2V_{dc}$. But, in classical topologies, all the switches have a peak inverse voltage of V_{dc}. The proposed thirteen level inverter utilized less number of components than the existing topologies. So, the average conduction loss of the proposed inverter is less compared to that of the existing topologies.

Total loss, $$p_{losses} = p_{c(avg)} + p_s \tag{24}$$

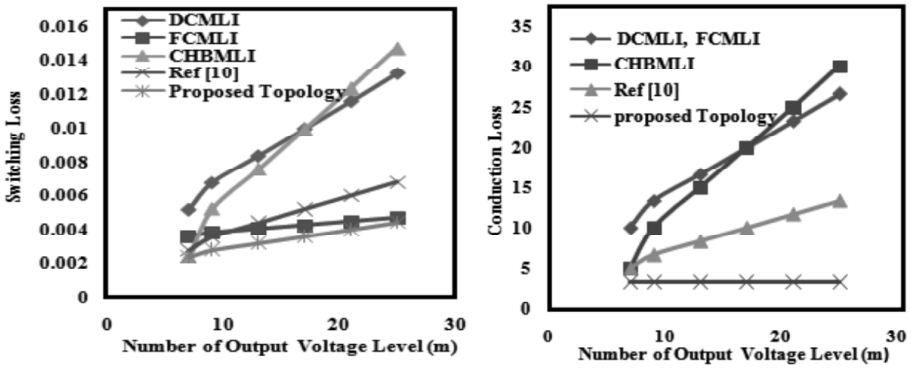


Figure 5: Comparison of losses of the proposed topology with other topologies. (a) Switching Loss (b) Conduction Loss

For switching loss and conduction loss calculations, all of the transistors the on-state resistance and voltage drop is considered to be 0.15ohm (R_T = 0.15 Ω) and 2.5V (V_T = 2.5 V), respectively. The on state resistance and voltage drop of the diodes is assumed to be 0.1 ohm (R_D = 0.1 Ω) and 1.5 V (V_D = 1.5 V), respectively. The on-time (t_{on}) and off-time (t_{off}) of the switches is assumed 2¼s. The source voltage has the value of 24 V. According to Fig. 5(a), switching power loss of the proposed topology is lower than that conventional topologies and topology presented in [10]. Fig. 5(b) depicts, the proposed topology having lower conduction loss than the other topologies. This result was expected since the number of semiconductor

devices in current path at any instant of time for the proposed topology is always two, which is lower than that of the other topologies.

It is concluded that, the total power loss of the proposed inverter is less, and the efficiency is increased, because the conduction and switching losses are minimized, as compared to the existing topologies.

IV. INVESTIGATION OF THE SIMULATION RESULTS

The simulation results are presented to verify the validation of the proposed cascaded single phase single DC source multilevel inverter. A computer-aided simulation has been carried out to validate the performance of the proposed thirteen level inverter with R and R-L Load using the MATLAB/Simulink environment.

The simulink model of the proposed thirteen level inverter is shown in Fig. 6. This simulink model has control signal generation unit and power circuit unit. The power circuit unit consist of a series connected capacitor network, power IGBT's and a mid-point transformer. Control signal generation unit is used to generate pulses for driving the IGBTs in the power circuit. The switching signal for the inverter is generated according to the switching Table I. The switching Pattern for the proposed Cascaded Thirteen level inverter is shown in Fig. 7. It is observed that, the level modulated switches are operating in high frequency and polarity modulated switches are operating in fundamental frequency**.**

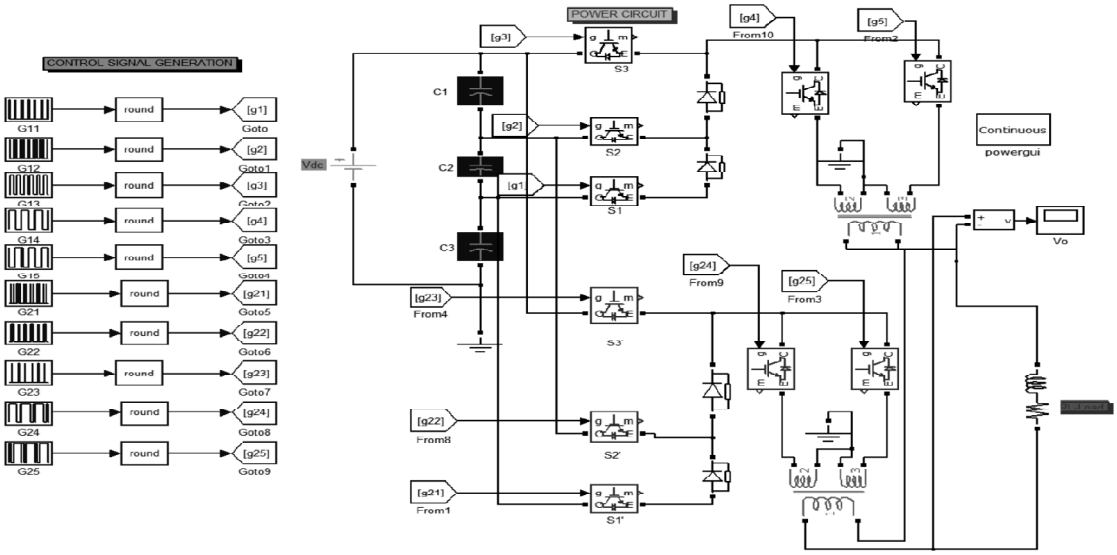


Figure 6: Simulink model of the proposed thirteen level boost inverter

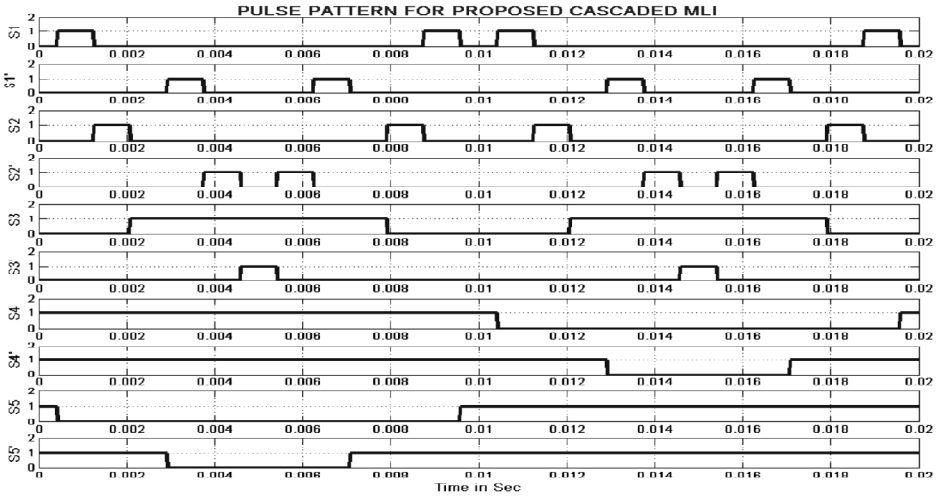


Figure 7: Switching Pattern for the proposed thirteen level boost inverter

Table 1
Switching State of the Proposed MLI

Switching State										*Inverter Output Voltage*
S_1	S_2	S_3	$S_{1'}$	$S_{2'}$	$S_{3'}$	S_4	$S_{4'}$	S_5	S_5'	(V_o)
0	0	1	0	0	1	1	1	0	0	$+2V_{dc}$
0	0	1	0	1	0	1	1	0	0	$+5V_{dc}/_3$
0	0	1	1	0	0	1	1	0	0	$+4V_{dc}/_3$
0	0	1	0	0	0	1	0	0	1	$+V_{dc}$
0	1	0	0	0	0	1	0	0	1	$+2V_{dc}/_3$
1	0	0	0	0	0	1	0	0	1	$+V_{dc}/_3$
0	0	0	0	0	0	0	0	1	1	**0**

In this study, the proposed inverter produces an output voltage magnitude of 48V, 50-Hz output waveform from a single DC input voltage of 24V. Each capacitor has a value of 330μF with an equal voltage of 24/3V. Here, both R and R-L loads with the values of 50Ω and 22mH are considered for simulation investigation.

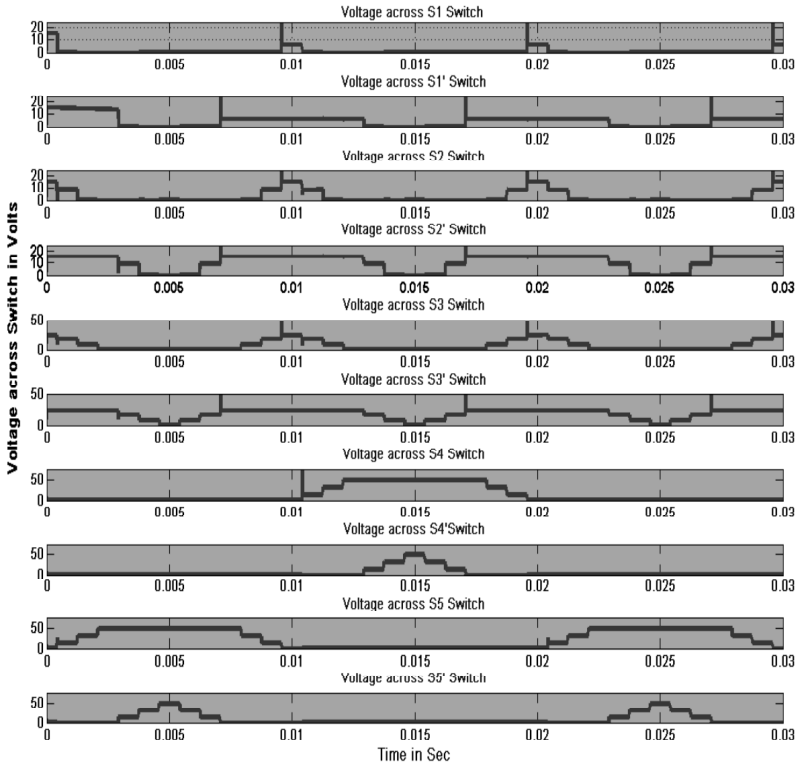


Figure 8: Voltage stress across each switches of proposed inverter

Each switches bear different voltage stress, which is presented in Fig. 8. The higher voltage rating switch must be employed for polarity modulated switches, because the voltage stress across each switch has twice the input voltage. But, the level modulated switches receive a voltage stress of less than the input dc voltage. The voltage stress across each level modulated switch has different value, which is depend on the position of the switch.

The simulated output voltage and current waveform for R and R-L loads obtained at the inverter terminal are shown in Figs. 9, 10 respectively. From Fig. 9, it is observed that, the inverter output current waveform, which follows the shape of inverter output voltage, but the magnitude of the current, depends on the load

resistance. In case of R-L load, the shape of the current waveform never follows the voltage shape, which is depends on the magnitude of R-L value used. Hence, this topology along with the proposed control algorithm can be a good choice for inverter circuits.

The simulated voltage and current harmonic spectrum of proposed cascaded boost thirteen level inverter for R and R-L load is depicted in Figs. 11, 12, 13 and 14. The total harmonic distortion (THD) in the inverter output voltage waveform for R and R-L loads are 16.36% and 19.38% respectively. Similarly, the total harmonic distortion (THD) in the inverter output current waveform for R and R-L loads are 16.36% and 8.80% respectively.

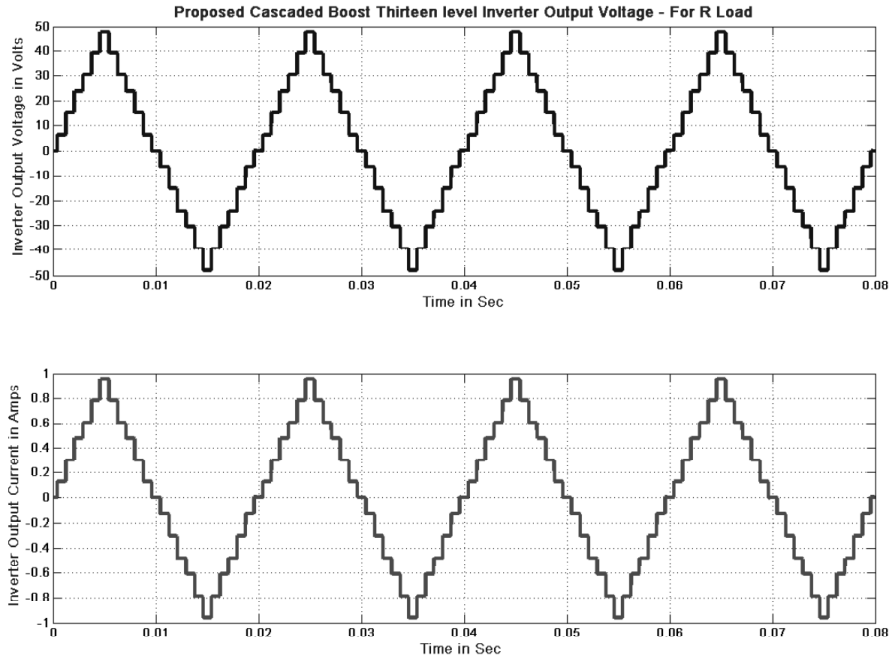


Figure 9: Simulated Inverter Output Voltage and Current waveform for R load

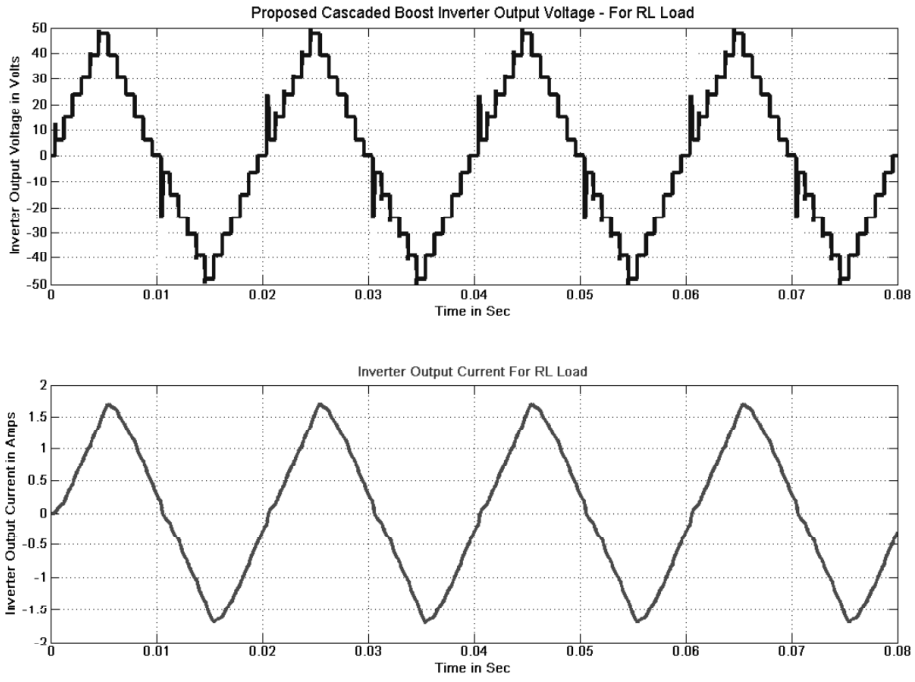


Figure 10: Simulated Inverter Output Voltage and Current waveform for R-L load

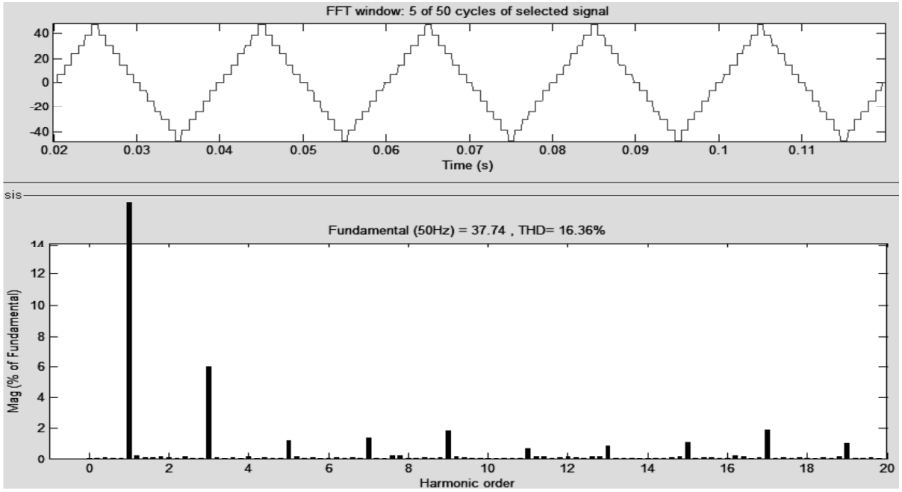


Figure 11: Simulated Voltage Harmonic spectrum of the proposed thirteen level Inverter with R load (without filter)

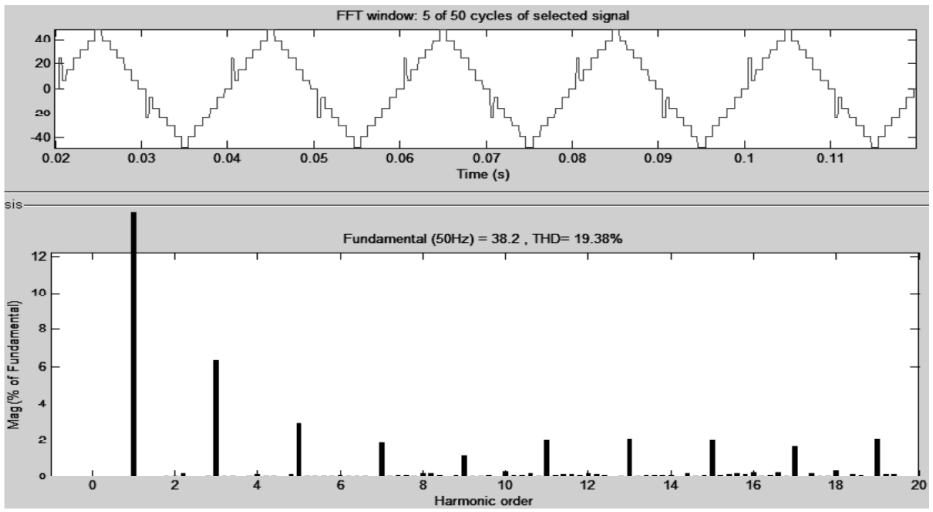


Figure 12: Simulated Voltage Harmonic spectrum of the proposed thirteen level Inverter with R-L load (without filter)

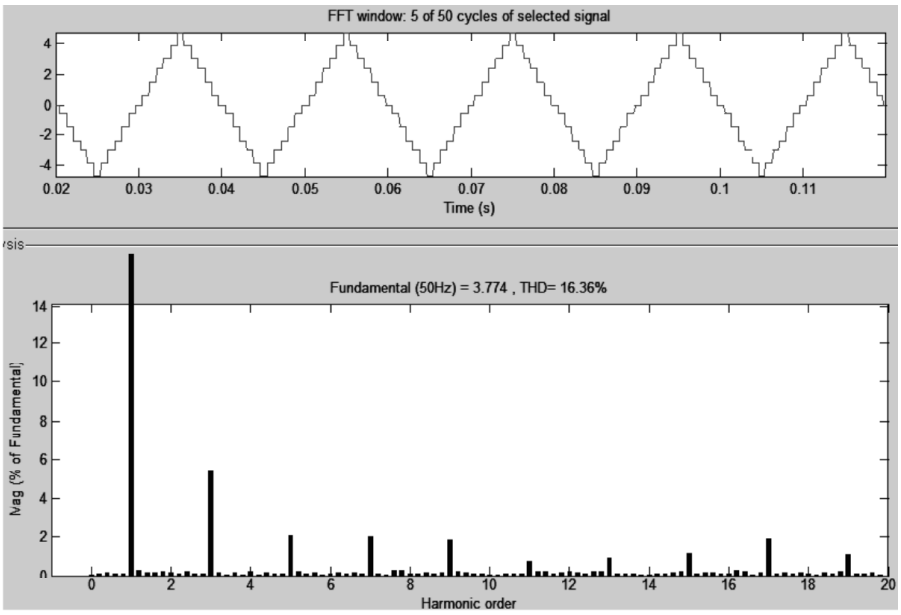


Figure 13: Simulated Current Harmonic spectrum of the proposed thirteen level Inverter with R load (without filter)

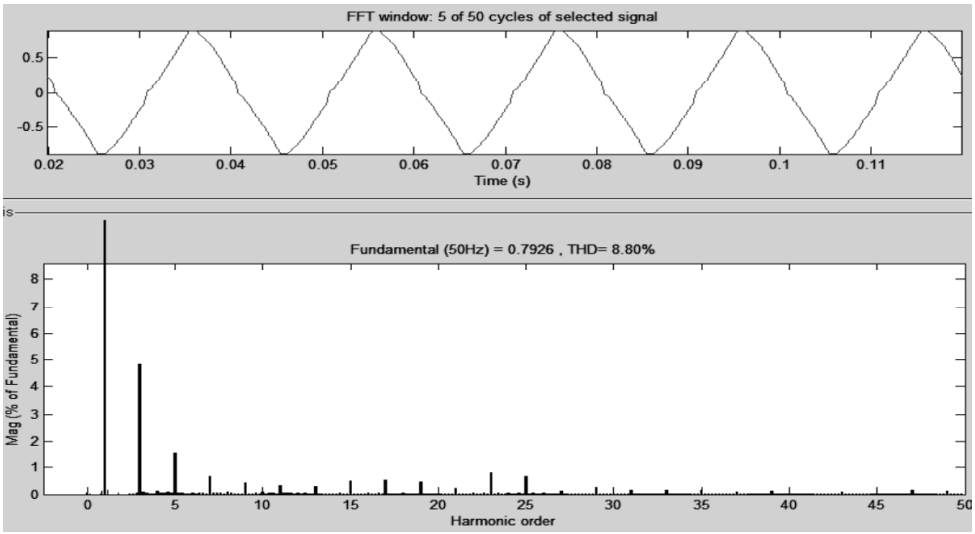


Figure 14: Simulated Current Harmonic spectrum of the proposed thirteen level Inverter with R-L load (without filter)

V. COMPARATIVE STUDY

The main purpose of this paper is the reduction of switches in multilevel inverters. Compared to all the existing multilevel inverters, the proposed topology requires fewer numbers of components. Table II shows the comparison of the components requirement between the proposed topology and the existing topologies. Fig. 15(a) shows that, the recommended topology needs fewer switches for generating an m-level output voltage. In this work, the thirteen level inverter is implemented using only ten switches, whereas other existing topologies require more than ten switches for obtaining a thirteen level output voltage. The proposed topology utilizes the minimum number of switches with minimum number of gate driver circuits, which reduces the circuit complexity in the inverter. Fig. 15(b) compares the number of main diodes required for the different existing topologies and the proposed topology. From this figure, it is clearly understood that, the proposed topology utilizes less number of diodes than the existing topologies. As a result, the overall

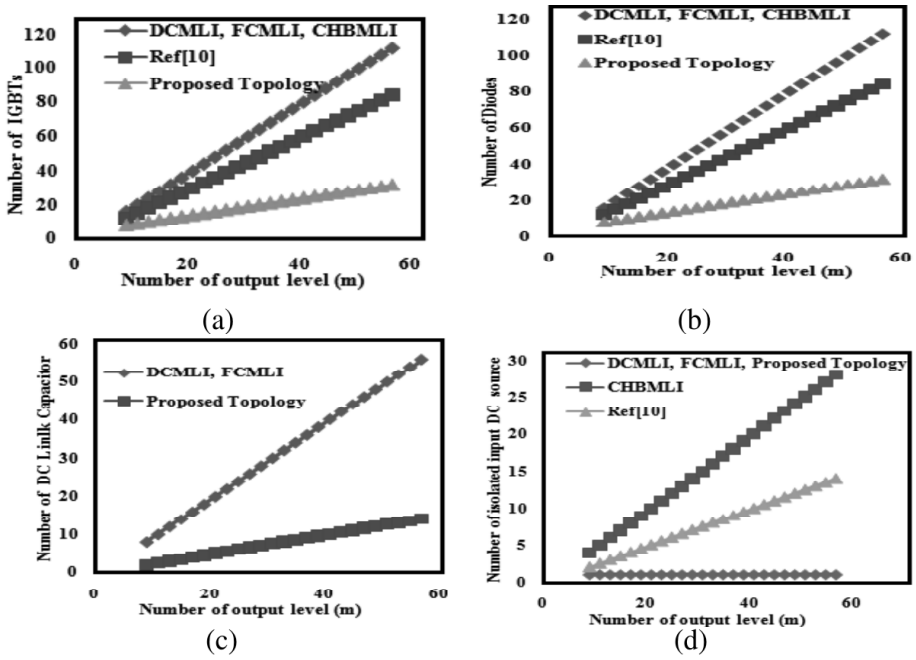


Figure 15: Comparison of the proposed topology with other topologies

(a) Number of IGBTs (b) Number of Diode (c) Number of DC link Capacitor (d) Number of isolated input DC sources

inverter power loss, size, cost and circuit complexity are reduced. Fig. 15(c) illustrates the comparison made between the proposed topology and the existing topologies in terms of the number of dc link capacitors with respect to the number of voltage levels. The comparison has been done of a single input dc source proposed multilevel inverters. Equal values of capacitors are used to make the voltage divider network, to provide different voltage levels in the inverter output. To develop a thirteen level output voltage level, the proposed topology requires three equal values of capacitors. Fig. 15(d) depicts the comparison between the proposed topology and the existing topologies in terms of the number of isolated input DC sources with respect to the number of voltage levels. The proposed topology requires only one isolated DC source, where as CHBMLI and the topology presented in [10] require more number of isolated DC sources. From this comparison, it is concluded that there is a reduction of power switches, diodes, and gate drive circuits, resulting in lower switching and conduction losses, in the proposed inverter compared to other topologies.

Table 2
Comparison of the Components Requirements for 13-level

Components	*DC MLI*	*FC MLI*	*CHB MLI*	*Presented Topology in [10]*	*Proposed Topology*
No. of main switches	24	24	24	18	10
No. of main diodes	24	24	24	18	10
No. of Bi-directionalswitches	0	0	0	0	0
No. of clamping diodes	132	0	0	0	0
No. of flying capacitors	0	66	0	0	0
No. of DC link capacitors	12	12	0	0	3
No. of isolated Input DCsources	1	1	6	3	1
No. of gate driver circuits	24	24	24	18	10

VI. CONCLUSION

In this paper, proposed a cascaded boost type single phase single source thirteen level inverter with switching technique has been developed and simulated. The proposed multilevel inverter utilized ten switches, two mid-point transformer and three capacitors to generate a thirteen level output voltage. The working nature of the proposed topology, mathematical formulation and simple switching techniques were analyzed in detail. In order to validate the operation and performance of the proposed inverter the MATLAB simulation model is developed and tested with R, and R-L loads. This work has been compared with classical and recent MLIs. Based on the study, it is confirmed that the proposed MLI utilized the minimum number of switching components with gate drive circuits, reduced the switching and conduction losses, and enhanced the overall efficiency of the MLI. This topology can be recommended for FACTS controllers and renewable energy systems.

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