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A Novel Design of Address Generator Circuitry for Wimax Deinterleaver

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Abstract : A novel design of address generator circuitry for implementing low complexity two dimensional deinterleaver used in WiMAX transceiver using Xilinx field programmable gate array (FPGA). For the permutation of the incoming bit stream required for the steps associated with floor function for the channel deinterleaver in IEEE 802.16e standard is highly difficult to implement inside FPGA. Elimination of the floor function inside FPGA is very difficult. A simple mathematical formulation and by sharing of resources for quadrature phase shift keying, 16 quadrature amplitude modulation (16-QAM), and 64 quadrature amplitude modulation (64-QAM) with all the required possible code rates will make this project to be efficient highly when compared to the other approaches. Reduction of hardware leads to compact address generator circuitry for Wimax Deinterleaver.

Keywords: Field Programmable Gate Array (FPGA's), Digital Circuits, Wireless systems.

1. INTRODUCTION

WiMAX is the standard based technology which enables the delivery for large mile wireless broadband access which is the recent time replacement for the cable and DSL. WiMAX provides a small portable, fixed wireless mobile broadband connectivity without the need of wire for direct line of sight for the base station.By integrating QPSK block, 16 QAM block and 64 QAM block and by sharing some resources all the possible code rates can be achieved for the address generation for the WiMAX Deinterleaver. Is the work in[1]. The Interleaver channel associated in WiMAX transceiver plays a major role in redusing the burst error effect. In brief in this, a novel less complex, high speed and efficient resource address generator which eliminates the floor function required. Even looking at the literature there is very less works related to this kind of Interleaver or Deinterleaver in WiMAX systems. The work in [2].

This paper is organised such that: section II will discuss about deinterleaver technique, section III discusses about algorithm proposed for the two dimensional deinterleaver associated with address generator with its mathematical formulation. In section IV algorithm is being transformed into hardware circuitry, later in section V, simulation results of QPSK block, 16 QAM block and 64 QAM block is presented along with integrated result showing the overall address generator for WiMAX deinterleaver. Finally the conclusion is given in brief in the last section VI.

2. DEINTERLEAVING TECHNIQUE IN WIMAX SYSTEM

Fig. 1 shows the WiMAX transmitter and receiving end from the complete WIMAX transceiver. Transmitter consists of a source, Randomizer, RS-CC Encoder, Channel Interleaver, Mapper, IFFT and a Channel. Receiver end consists of the same channel, FFt, De-mapper, Channel De-Interleaver, RS-CC Decoder, De-Randomizer and a sink.Source acquires and feed to randomizer, the RS-CC Encoder encodes the bits automatically and gives to channel interleaver and the signal is mapped through IFFT and the bits are

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passed through channel[3]. In the receiver end the bits coming from channel is followed the same way as the reverse way on transmitter end.

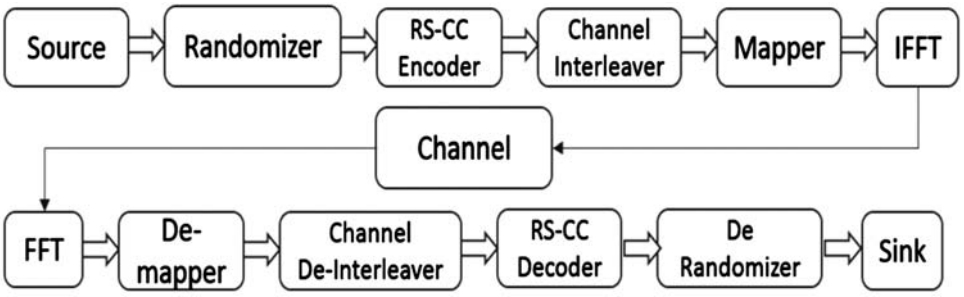

Figure 1: WiMAX Transmitter and Receiver Blocks

Interleaving/Deinterleaving structures in two dimentional form used in WiMAXis shown in Fig. 2. There is a memory block M-1 and M-2, corresponding multiplexer connected to it for the selection. There is a read address and write address generator connected to multiplexer[4]. Final memory block is connected to mux with selection switch. With selection 0, memory 1 will be selected and with selection 1, memory 2 will be selected, through which Interleaved data will be obtained.

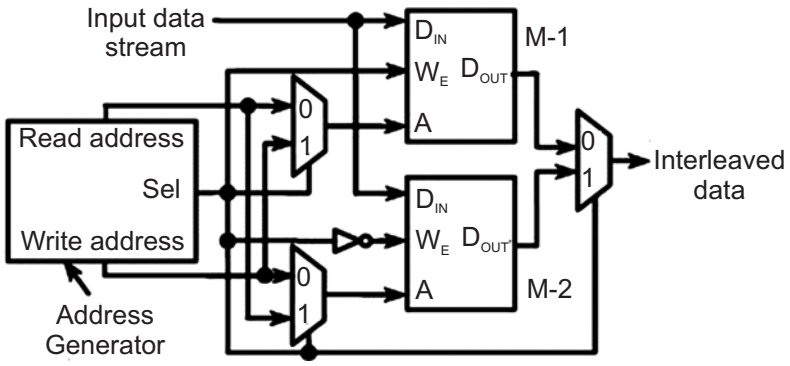

Figure 2: Block diagram showing Interleaver/Deinterleaver structure

In the Interleaver or Deinterleaver blocks, there are different depths in it which is given as Ncbps which helps in incorporating multiple code rates with all the modulation schemes (Table 1) in IEEE 802.16*e*.

Table 1

All the Permitted Deinterleaver Depth in Wimax Standard IEEE 802.16E for Multiple Code Rates and Possible Modulation Scchemes

Modulation Schemes	*QPSK (s = 1)*		*16-QAM (s = 2)*		*64-QAM (s = 3)*		
Code Rate	*½*	*¾*	*½*	*¾*	*½*	*2/3*	*¾*
Interleaver Depth, Ncbps in bits	96	144	192	288		384	432
	192	288	384	576		–	–
	288	432	576	–	–	–	–
	384	576	–	–	–	–	–
	480	–	–	–	–	–	–
	576	–	–	–	–	–	–

In table 2 all the possible address for multiple code rates are obtained considering for rows and five columns with the formula given for channel interleaver and channel deinterleaver.

Table 2
Sample Addresses in Deinterleaver for All modulation Typess Showing first Four Rows and Five Columns and Three Code Rates

Ncbps, code rate & modulation type	*De-Interleaver addresses*				
Ncbps = 96 bits, ½ code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
Ncbps = 192 bits, ½ code rate, 16-QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
Ncbps = 576 bits, 3/4 code rate, 64-QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

3. ALGORITHM PROPOSED FOR ADDRESS GENERATOR CIRCUITRY

The algorithm proposed for generating address generation in WiMAX deinterleaver with its mathematical formulations has been discussed. Through mathematical coding conversion in Matlab for all modulation schemes and for all the possible code rates has been proposed[5]. Usually in FPGA directly we can't implement floor function, so we are here with the help of mathematical formulation, trying to avoid that floor function. In the design, number of rows (d) are fixed as 16 for all the number of coded bits (Ncbps), and the column number is varied with simple calculation by dividing Ncbps/d. A divider circuit is replaced in this work as an enhancement for the work, which automatically generates the column number with all the possible modulation techniques and for all the code rates.

Table 3 shows the values obtained from mathematical formulation for all the modulation schemes and for all the code rates with 4 rows and 5 columns.

$$\text{K}n,\ \text{QPSK} \ = \ \{d * i + j \text{ for } \forall j \text{ and } \forall i\} \tag{1}$$

$$\text{K}n,\ \text{16-QAM} \ = \ \begin{Bmatrix} d * i + j \text{ for } j\%2 = 0 \text{ and for } \forall i \\ d * (i+1) + j \text{ for } j\%2 = 1 \text{ and for } i\%2 = 0 \\ d * (i-1) + j \text{ for } j\%2 = 1 \text{ and for } i\%2 = 1 \end{Bmatrix} \tag{2}$$

$$\text{K}n,\ \text{64-QAM} \ = \ \begin{Bmatrix} d * i + j \text{ for } j\%3 = 0 \text{ and for } \forall i \\ d * (i-2) + j \text{ for } j\%3 = 1 \text{ and for } i\%3 = 2 \\ d * (i+1) + j \text{ for } j\%3 = 1 \text{ and for } i\%3 \neq 1 \\ d * (i+2) + j \text{ for } j\%3 = 2 \text{ and for } i\%3 = 0 \\ d * (i-1) + j \text{ for } j\%3 = 2 \text{ and for } i\%3 \neq 0 \end{Bmatrix}$$

In the above mathematical equations, Kn is the deinterleaver address generated through the equation. D is the fixed value, *i.e*. 16 which is the number of rows and *i*, *j* vary according to the equation[6]. First equation shows the mathematical equation for the addresses of QPSK block, the second shows for the addresses of 16-QAM block and the last equation shows for the addresses of 64-QAM block.

Table 3
Determination of Correlation Between Addresses

Row No.(j)	*Column No. (i)*	*0*	*1*	*2*	*3*	*4*
0	Ncbps = 96 bits, ½ code rate, QPSK	*d*.0 + 0 = 0	*d*.1 + 0 = 16	*d*.2 + 0 = 32	*d*.3 + 0 = 48	*d*.4 + 0 = 64
1		*d*.0 + 1 = 1	*d*.1 + 1 = 17	*d*.2 + 1 = 33	d.3 + 1 = 49	d.4 + 1 = 65
2		*d*.0 + 2 = 2	*d*.1 + 2 = 18	*d*.2 + 2 = 34	*d*.3 + 2 = 50	*d*.4 + 2 = 66
3		*d*.0 + 3 = 3	*d*.1 + 3 = 19	*d*.2 + 3 = 35	*d*.3 + 3 = 51	*d*.4 + 3 = 67
0	Ncbps = 192 bits, ½ code rate, 16 QAM	*d*.0 + 0 = 0	*d*.1 + 0 = 16	*d*.2 + 0 = 32	*d*.3 + 0 = 48	*d*.4 + 0 = 64
1		*d*.1 + 1 = 17	*d*.0 + 1 = 1	*d*.3 + 1 = 49	*d*.2 + 1 = 33	*d*.5 + 1 = 81
2		*d*.0 + 2 = 2	*d*.1 + 2 = 18	*d*.2 + 2 = 34	*d*.3 + 2 = 50	*d*.4 + 2 = 66
3		*d*.1 + 3 = 19	*d*.0 + 3 = 3	*d*.3 + 3 = 51	*d*.2 + 3 = 35	*d*.5 + 3 = 83
0	Ncbps = 576 bits, ¾ code rate, 64 QAM	*d*.0 + 0 = 0	*d*.1 + 0 = 16	*d*.2 + 0 = 32	*d*.3 + 0 = 48	*d*.4 + 0 = 64
1		*d*.1 + 1 = 17	*d*.2 + 1 = 33	*d*.0 + 1 = 1	*d*.4 + 1 = 85	*d*.5 + 1 = 81
2		*d*.2 + 2 = 34	*d*.0 + 2 = 2	*d*.1 + 2 = 18	*d*.5 + 2 = 82	*d*.3 + 2 = 50
3		*d*.0 + 3 = 3	*d*.1 + 3 = 19	*d*.2 + 3 = 35	*d*.3 + 3 = 51	*d*.4 + 3 = 67

4. CIRCUIT TRANSFORMATION

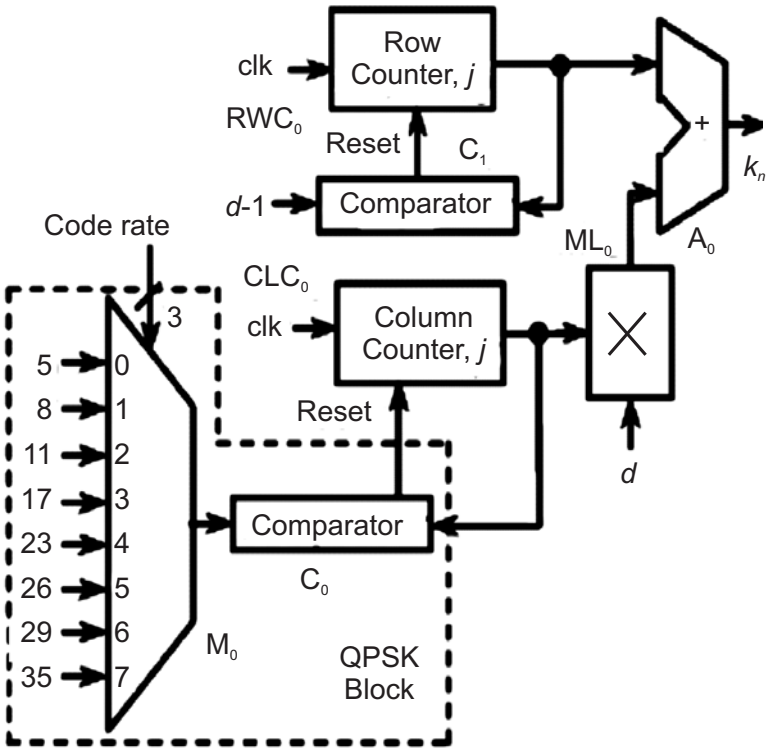

Figure 3: Hardware structure of address generator circuitry for QPSK Block

To verify the circuit for all the possible code rates, transformation of mathematical formulation into digital circuit is absolutely necessary. QPSK hardware shown in Fig 3, has a row counter (RWCo), a column counter (CLCo), with a comparator (Co) to compare the values, a multiplier (MLo) and a adder circuit (Ao)[7]. Replacement of divider hardware will automatically select the code rate based on modulation schemes for wide range. Fig 4 shows the hardware replacement for the mux with a divider circuit for selection of all the possible code rates with the selection of modulation schemes automatically[8]. Fig 5 shows the 16-QAM circuitry transformed through its mathematical formulation, mux replaced with divider block and in Fig 6 shows the 64 – QAM block is being transformed into circuitry with divider block and the operation is similar as explained for the QPSK block.

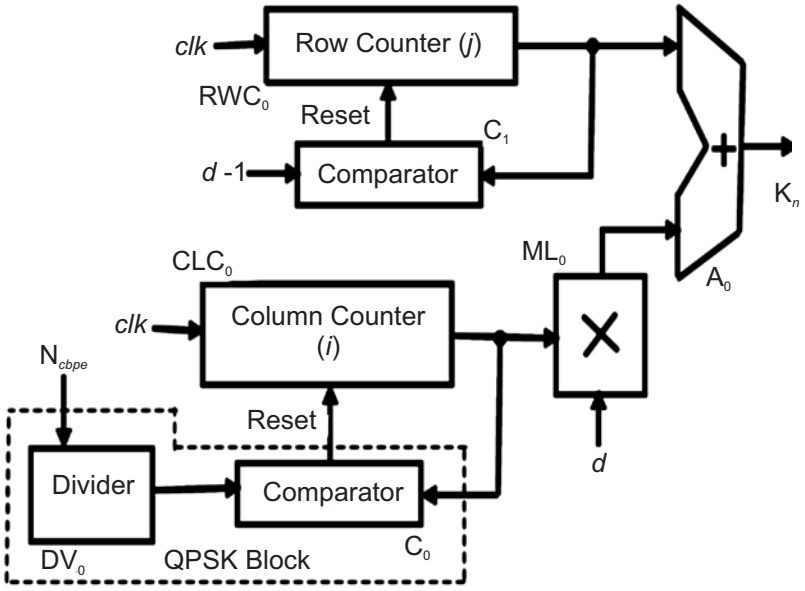

Figure 4: Hardware structure of address generator circuitry for QPSK Block with Divider Block

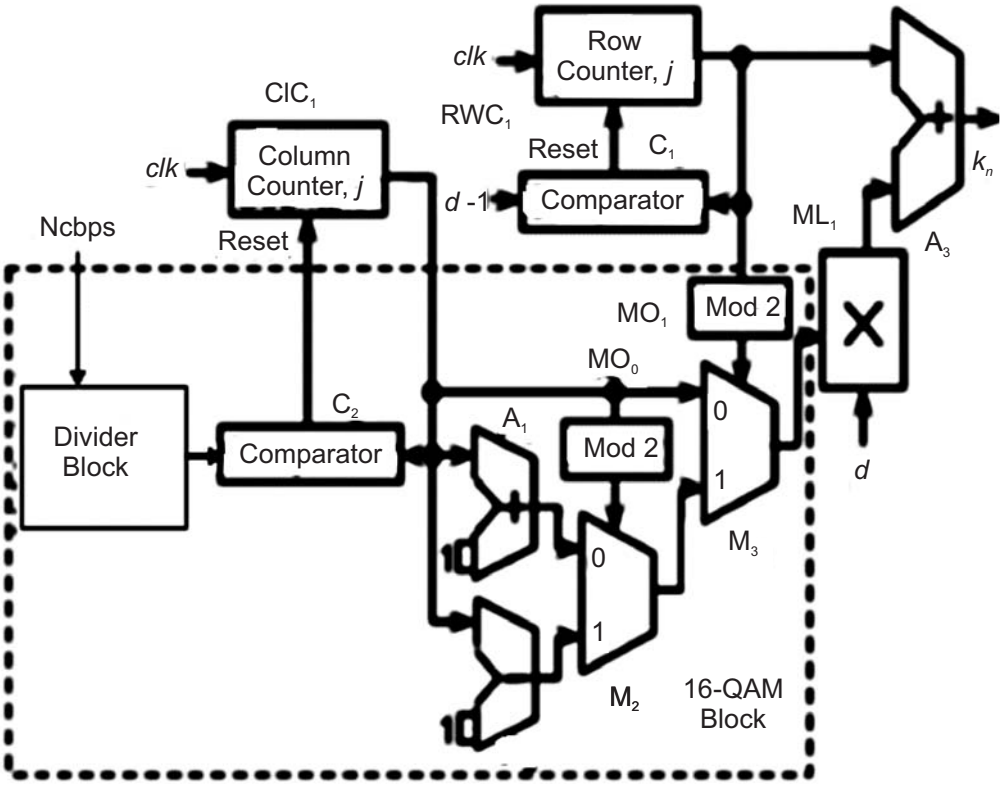

Figure 5: Hardware structure of address generator circuitry for 16-QAM with Divider Block

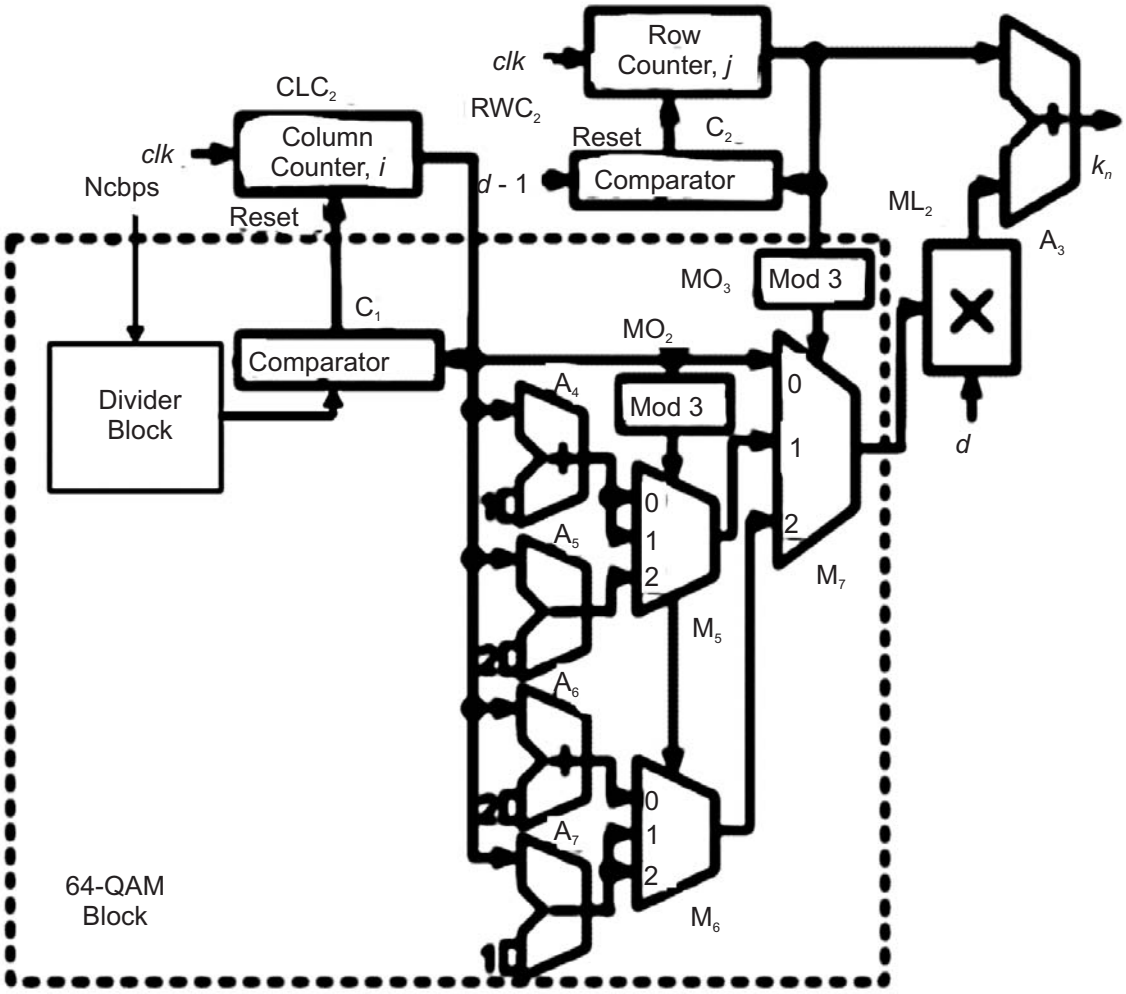

Figure 6: Hardware structure of address generator circuitry for 64-QAM with Divider Block

With the integration of all the three circuits, QPSK Block, 16-QAM block and 64-QAM block, by sharing the common resources between them, the overall top level circuit for the deinterleaver address generator circuitry is shown in Fig 7.

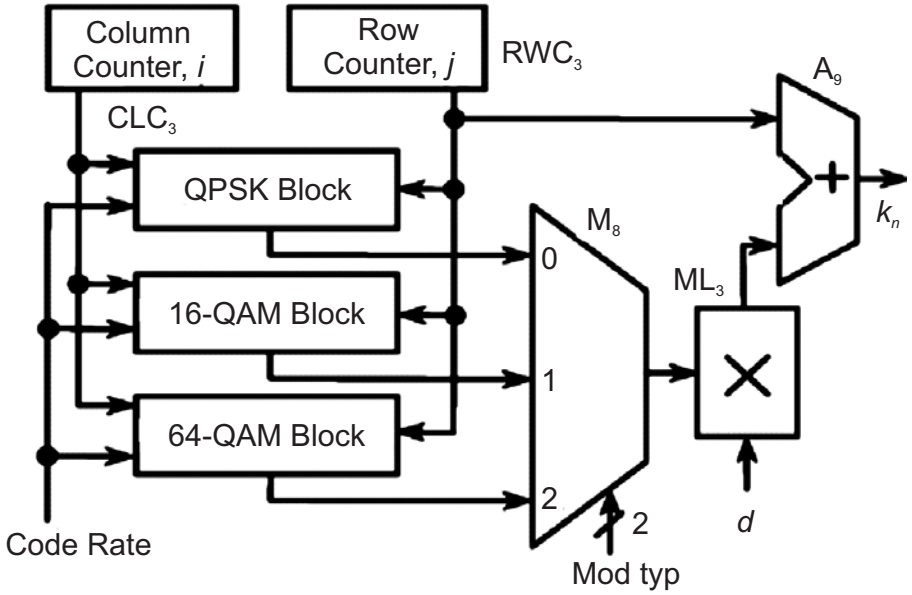

Figure 7: Hardware structure of address generator Top-Level Complete circuitry

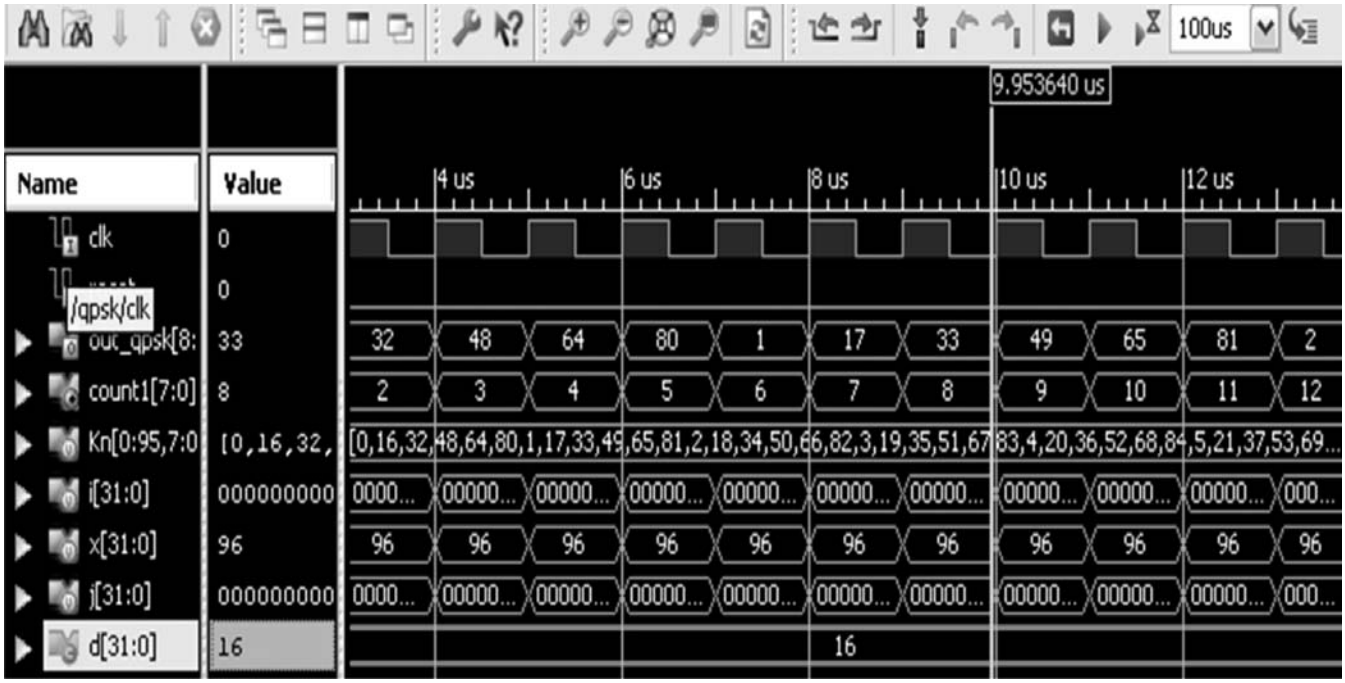

Figure 8: Simulation Results showing address generated for QPSK Block

5. SIMULATION RESULTS

Verilog coding for the hardware of the address generator is done for individual QPSK, 16-QAM and 64-QAM blocks and the integrated circuit design results are shown for the deinterleaver address generator. In Fig 8, Simulation results of QPSK block address generation is shown, Fig 9 shows the same with 16-QAM block, Fig 10 with 64-QAM block. Fig 11, Fig 12 and Fig 13 shows the selection of QPSK block, 16-QAM block and 64-QAM block respectively in the integrated address generator circuitry. Results are verified using Xilinx ISim[9]. for all permissible modulation scheme types and for all the possible code rates. The simulation results for different modulation schemes and code rates are shown.

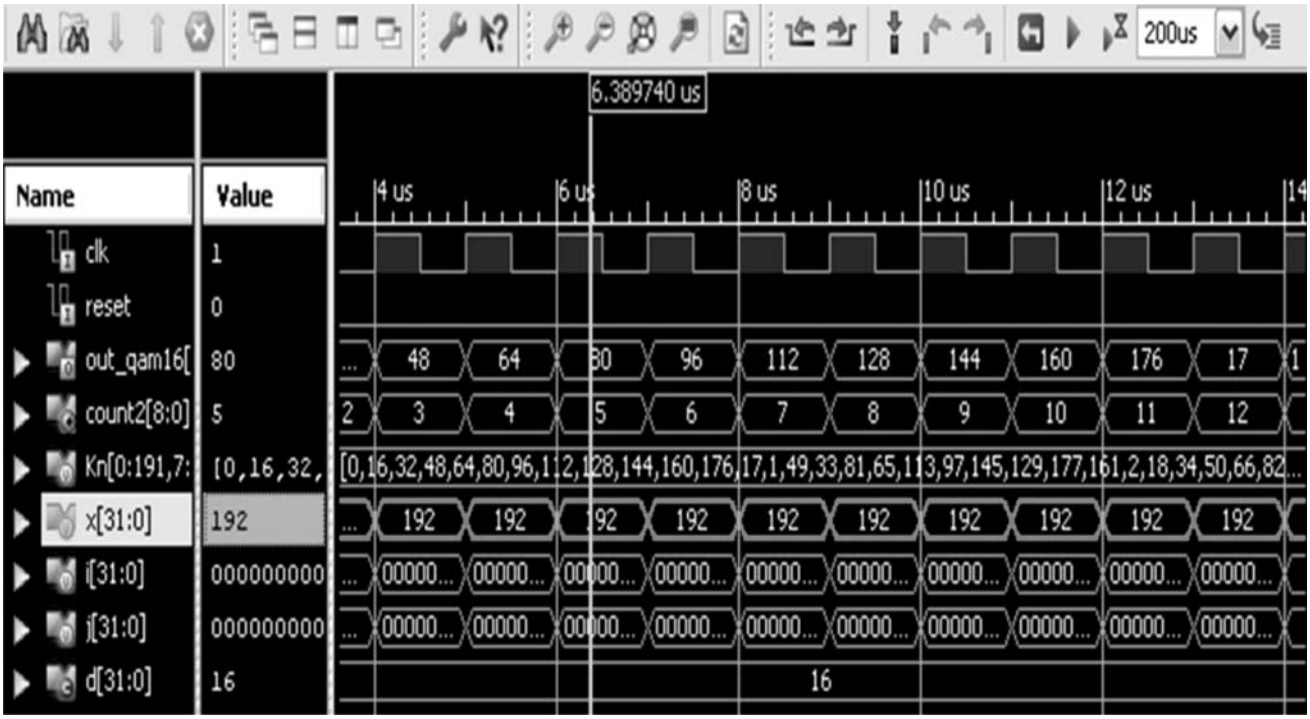

Figure 9: Simulation Results showing address generated for 16 – QAM Block

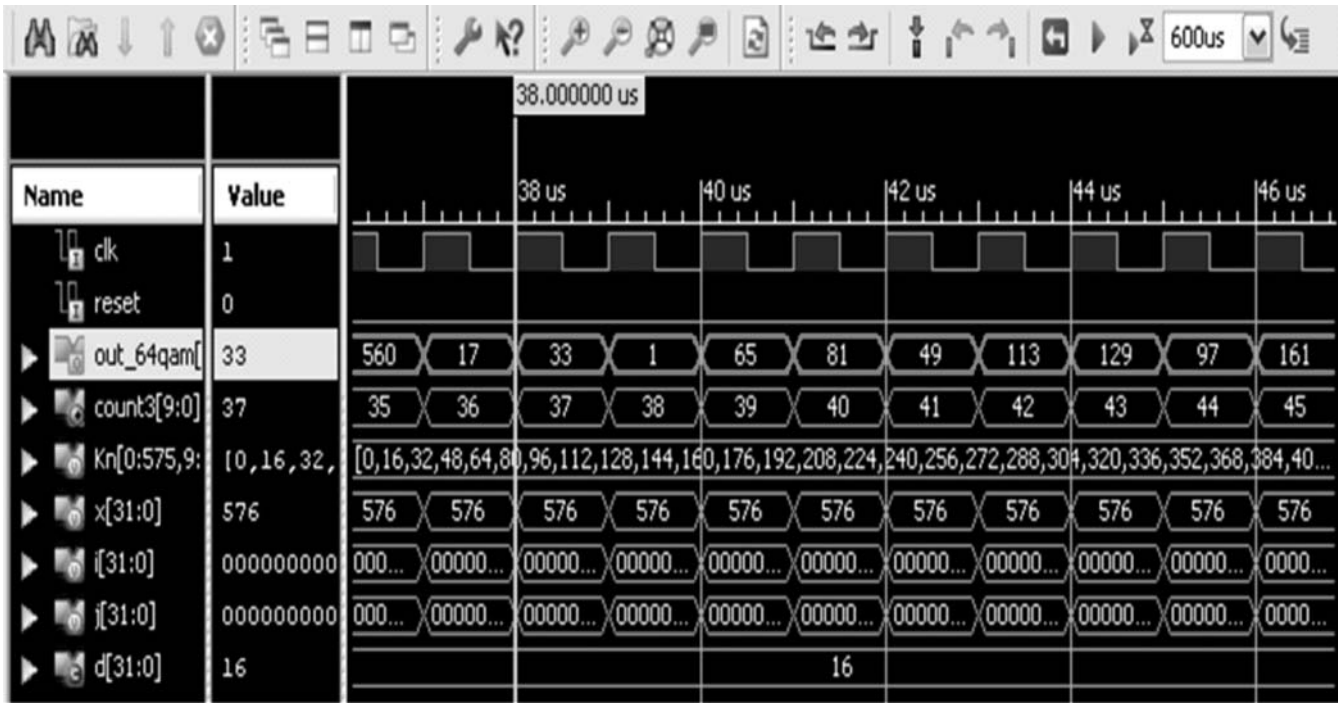

Figure 10: Simulation Results showing address generated for 64 – QAM Block

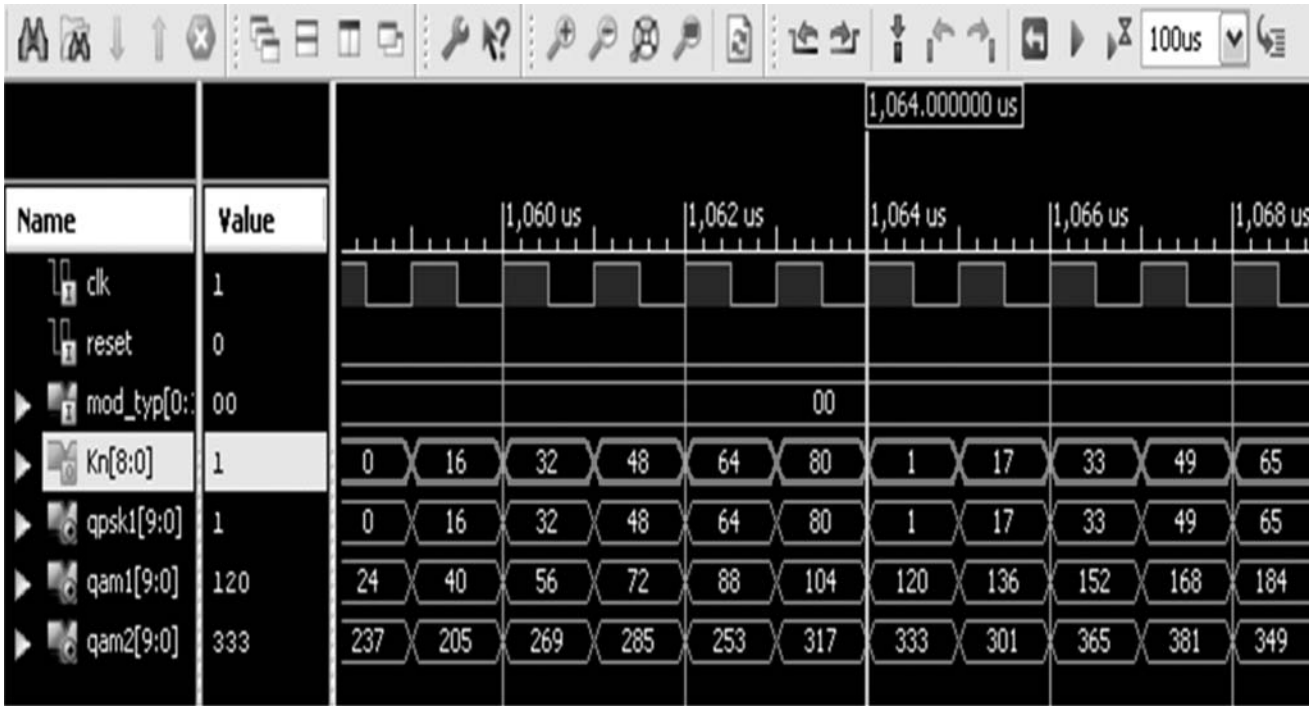

Figure 11: Simulation Results showing integrated circuitry of address generator with QPSK Block selection

6. CONCLUSION

WiMAX Transceiver is a system which is used for transmission and reception of wireless data in the WiMAX technology. A design along with its mathematical formulation for address generation circuitry of the WiMAX transceiver deinterleaver is presented. It supports all permitted code rates and modulation patterns as per IEEE 802.16*e*. The design was coded using Verilog HDL and the simulation was carried out using Xilinx ISE Sim. The simulation results for QPSK (N_{cbps} = 96), 16-QAM (N_{cbps}= 192) and 64-QAM (N_{cbps}= 576) are presented.

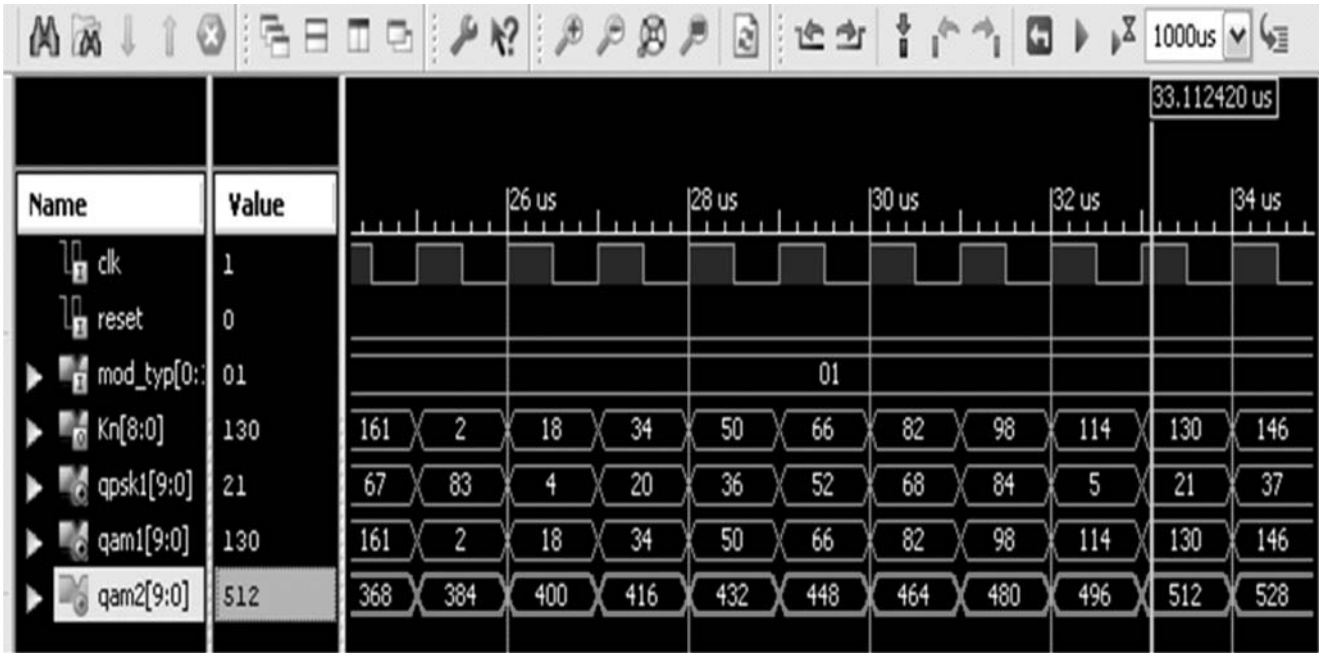

Figure 12: Simulation Results showing integrated circuitry of address generator with 16-QAM Block selection

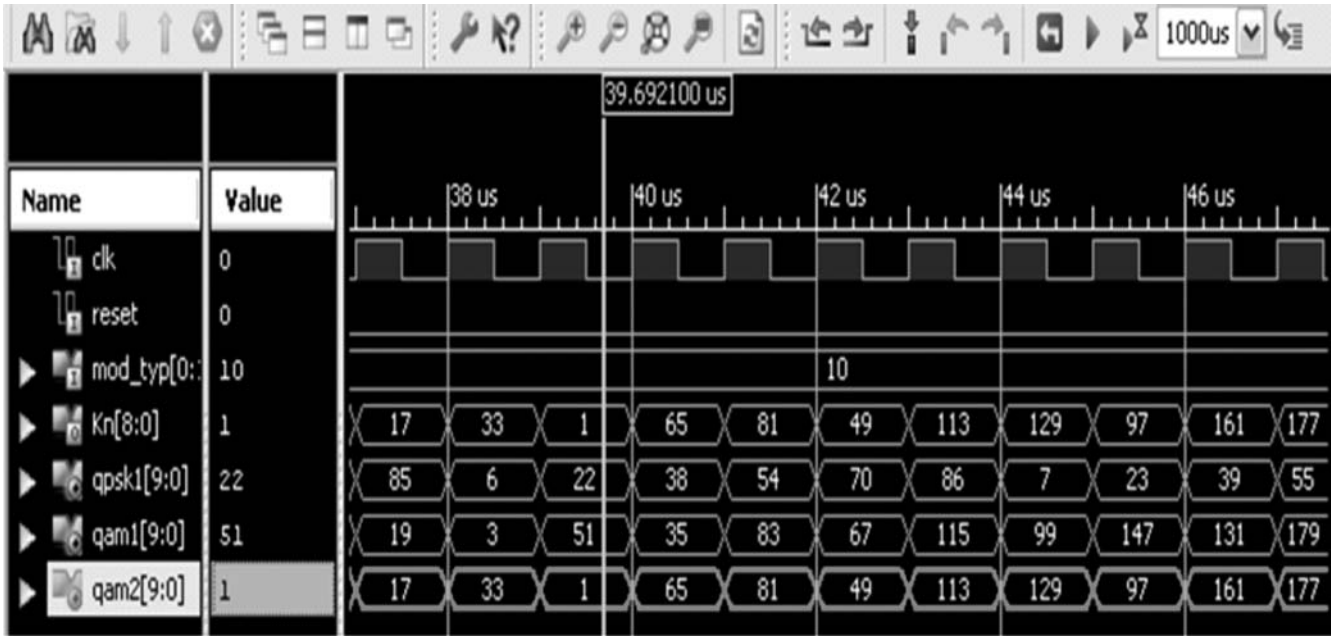

Figure 13: Simulation Results showing integrated circuitry of address generator with 64-QAM Block selection

7. ACKNOWLEDGEMENT

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8. REFERENCE

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