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Read Operation Performance Analysis of Modified Crossbar Array Structures with Self-Rectifying Memristive Device Model

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ABSTRACT

The advances in conventional memory technologies are confronting serious design issues due to continued scaling. Resistive memory is one of the promising emerging applications of the memristor which apparently will replace present memories because of their high density and non-volatility. The crossbar array structure is the best implementation that achieves the highest memory density with less complexity. However, the problem with these resistive crossbar arrays is the current sneak path that is limiting the memory capacity.

In this paper, we use a set of different passive crossbar structures , based on introducing insulating nodes, along with memristive device that exhibits self-rectifying behaviour to suppress the sneak path current. A fundamental evaluation of read operation performance based on the voltage margin and power consumption is conducted. The proposed solution shows a significant enhancement in both read voltage margin and power consumption.

Keywords: Self-rectifying Memristor, Memristive device, Crossbar array, Sneak path current, Voltage margin, Power consumption

1. INTRODUCTION

In 1971, a conceptual theory of the memristor was postulated by Leon Chua [1]. Besides the resistor, capacitor, and inductor, the memristor is considered a fourth basic circuit element with unique characteristics. It is regarded as a promising device as it may be used in diverse applications. The main feature of the memristor is its ability to remember the history of the current passed through it, making it a good candidate for the nonvolatile resistive random access memory (ReRAM). The working principle of the memristive memories is based on two logical states, 0 and 1 that are related to the high resistance state and low resistance state of the memristor, respectively [2]. It is expected to be an excellent replacement for the flash based memory due to small feature size, low power requirement, CMOS compatibility, and resistive nature [3].

Researches in nanoscale memories mainly focus on the crossbar architecture [4]. The crossbar structure consists of a grid of two sets of parallel nanowires that consists of a memristor switch at every crosspoint between the horizontal and vertical wires. Crossbar arrays offer a few advantages including easily fabricated pattern, CMOS process compatibility, high density, and the ability to perform a lot of computations [5]. However, a typical memristive crossbar array suffers from parasitic current that flows through the unselected memory cells (called sneak path current) as shown in Fig. 1. The sneak path current is a major challenge restricting a large scale memristor crossbar arrays that permit a reliable recognition between the two logic states of a memory cell [6].

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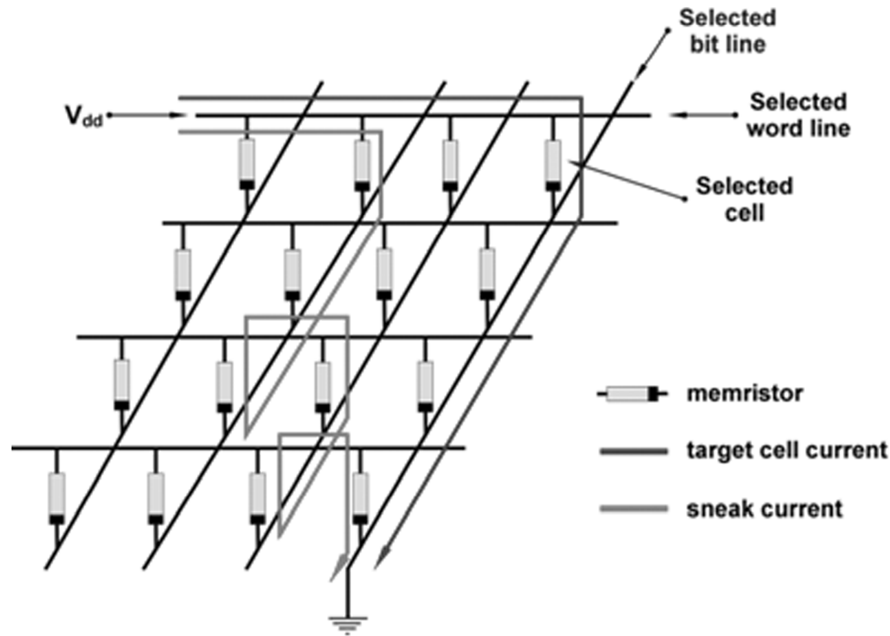

Figure 1: Sneak path current in memristive crossbar array

To avoid the sneak path current, several solutions are proposed. One approach is to use a diode [7], transistor [8], complementary memristor [9], or memistor [6] gating device that acts as a selector to control the flow of the current in the crossbar array. Among many limitations of this approach, it will spoil the memory density because the size of the gating device is larger than the memristor. Another idea is to use a multistage reading scheme based on a repetitive read procedure that require longer time to read the content of a memory cell [10, 11]. A third solution suggests the use of AC signal instead of DC signal to sense the content of the desired cell [12], but adds additional complexity to the memory system.

Our motivation in this work is to study the read operation performance of large passive crossbar arrays in terms of voltage margin and power consumption. In our study, we: (i) provide behavioral model of a self-rectifying memristive device, (ii) discuss alternative crossbar topologies with insulating nodes, and (iii) study the effect of different biasing schemes on the read operation. The rest of the paper is organized as follows: section 2 provide a behavioral model for the memristor. Section 3 presents five alternative crossbar architectures. Four different partial biasing schemes are introduced in section 4. The read operation performance in terms of voltage margin and power consumption is presented in section 5; followed by a conclusion in section 6.

2. SELF-RECTIFYING MEMRISTOR MODEL

Several memristive devices with diodelike I-V characteristics are reported [13]-[19]. These special memristors have the ability to suppress the current passing through it when reverse biased. A rectification ratio of $10^6$is achieved using amorphous silicon (a-Si) memristive device without affecting the switching speed or data retention, suggesting a possible solution to the sneak path current problem in crossbar arrays without any extra selector device [20].

To demonstrate the behavior of the self-rectifying memristor, a mathematical model is derived based on a modified voltage threshold adaptive memristor (VTEAM) model presented in [21]. Besides its computational efficiency, VTEAM model is flexible to fit any practical memristive device accurately. Modifying the original VTEAM model to fit with the self-rectifying memristor behavior, then the I-V relationship and state derivative equations of the device are given as:

$$i(t) = R_m^{-1}.v(t) \tag{1}$$

$$R_m = \begin{cases} R_{off} & for(v < 0) \\ R_{on} + \dfrac{R_{off} - R_{on}}{W_{off} - W_{on}}(w - w_{on}) & for(v > 0) \end{cases} \tag{2}$$

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\dfrac{v(t)}{v_{off}} - 1\right)^{a_{off}} & for(0 < v_{off} < v) \\ 0 & for(v_{on} < v < v_{off}) \\ k_{on}\left(\dfrac{v(t)}{v_{on}} - 1\right)^{a_{on}} & for(v < v_{on} < 0) \end{cases} \tag{3}$$

Fig. 2 shows the I-V characteristic of the self-rectifying memristor model. The modelled memristor has a state variable $w \in [w_{off}, w_{on}]$ that is related to the memristance R_m as follows: when $w = w_{off}$ then $R_m = R_{off}$ and the memristor is said to be in the high resistance (OFF) state. When $w = w_{on}$ then $R_m = R_{on}$ and the memristor is said to be in the low resistance (ON) state. The model relies on a threshold voltage (v_{on} and v_{off}) such that the memristance (state) of the memristive device only changes when the applied voltage is above (or below) a certain voltage level. Furthermore, when the memristor is reverse biased (yet not exceeding the threshold voltage v_{on}), it will suppress the current passing through it without changing the state variable

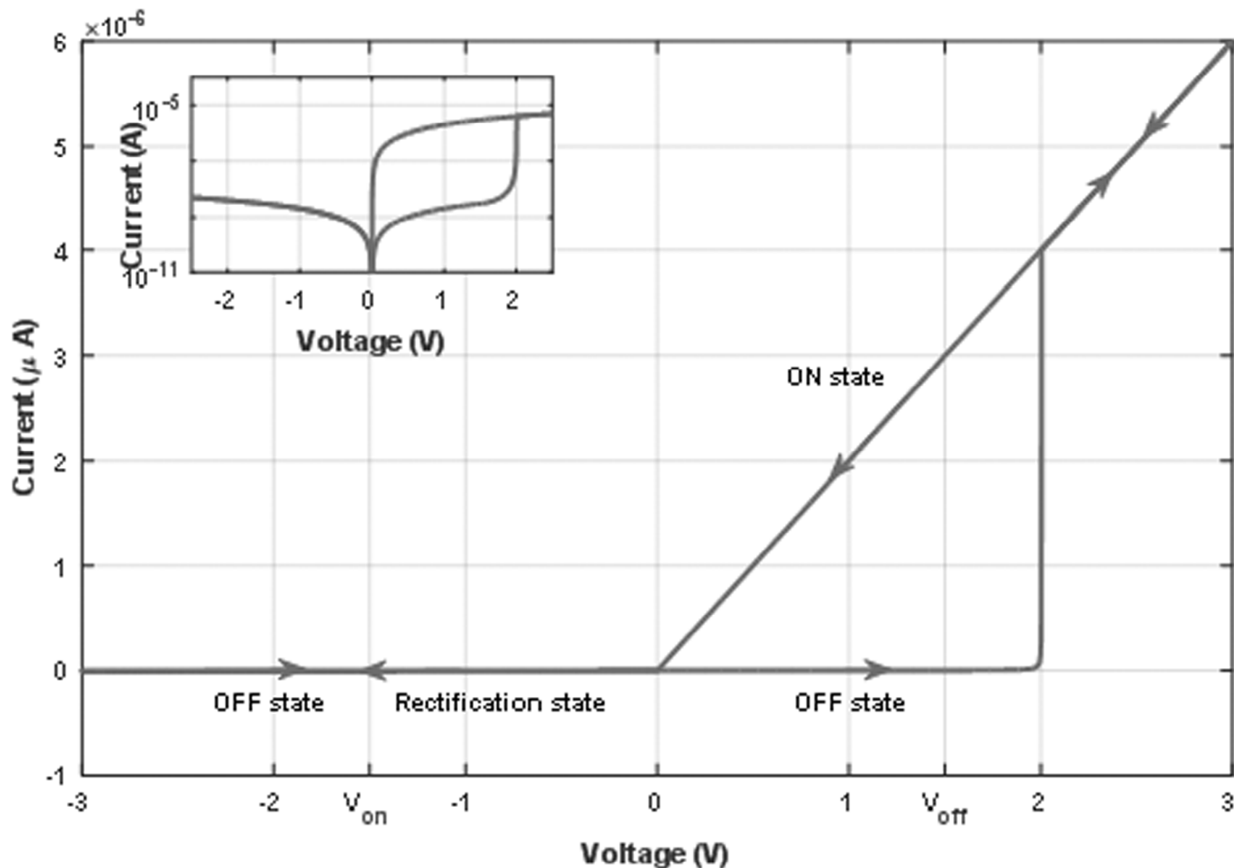

Figure 2: I-V characteristics of the self-rectifying memristor. Inset: I-V in semilogarithmic scale

similar to the behavior of the one-diode, one-memristor (1D1M) memory cell. The mathematical model of the memristor is created in Verilog-A hardware description language (HDR).

3. ALTERNATIVE CROSSBAR ARRAY STRUCTURES

In [22], a possible solution to limit the sneak path current and improve the voltage margin is proposed using passive crossbar array. This solution is based on introducing five alternative crossbar topologies that have insulating junctions distributed according to a specific patterns within the crossbar to minimize the impact of sneak current, as shown in Fig. 3. The results reveal that significant improvements of the sensed voltages can be realized. Despite the fact that this practice will minimize the number of the available memory cells but it is a feasible solution because of the huge memory cell density of the crossbar architecture besides its simplified fabrication process. A description of these crossbar topologies is as follows:

1) *Column topology:* The insulating nodes are placed in columns in a uniform manner.
2) *Row topology:* It is same as column topology except that the insulating nodes are uniformly located in rows.
3) *Column and row topology:* It is a combination between the column and row topologies.
4) *Rectangular ring topology:* The insulating nodes are distributed in rectangular rings pattern starting from the four inmost cells.
5) *Diagonally distributed topology:* The insulating nodes are distributed across the diagonal of the array such that the nearest neighborhood insulating nodes are placed in equal horizontal and vertical distances.

It should be noted that the number of insulating nodes is different for each topology provided that the array size is the same as shown in Fig. 4. Along with the number of the insulating nodes, their distribution play a role in improving the performance of a crossbar array.

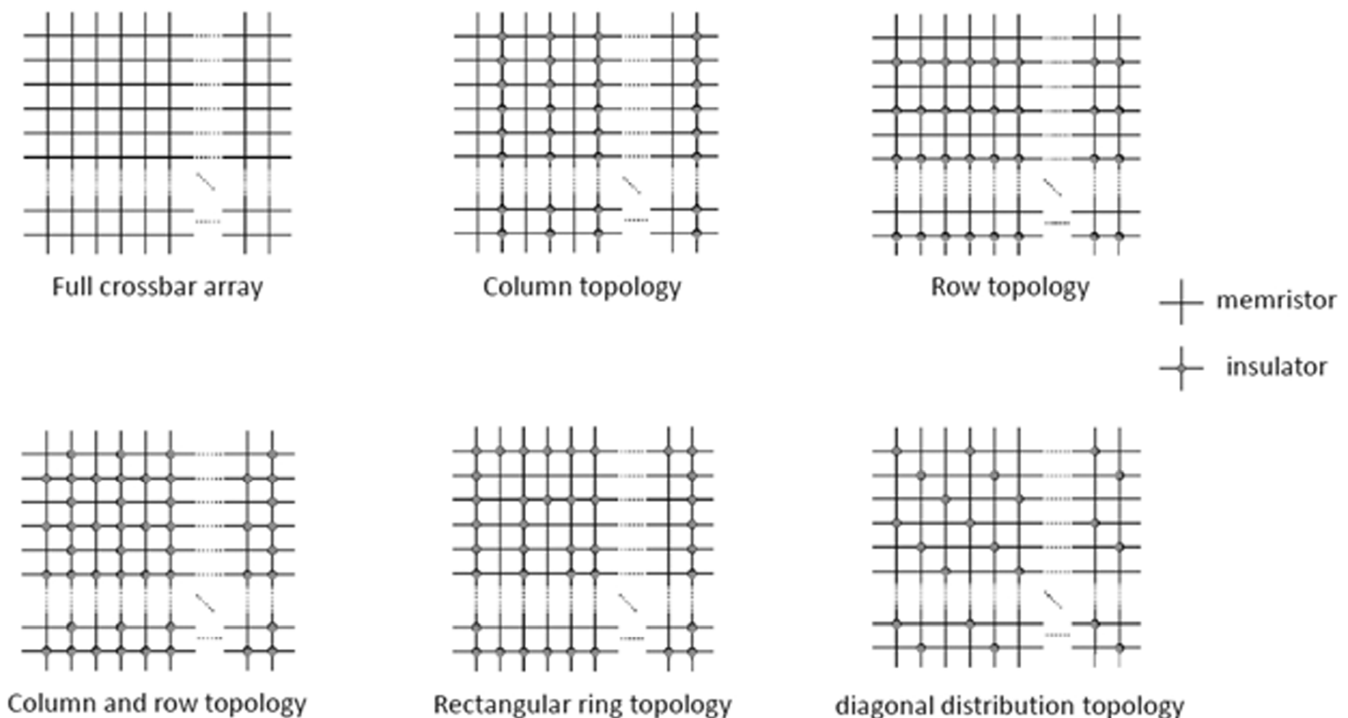

Figure 3: Modified crossbar structures compared with the full crossbar array

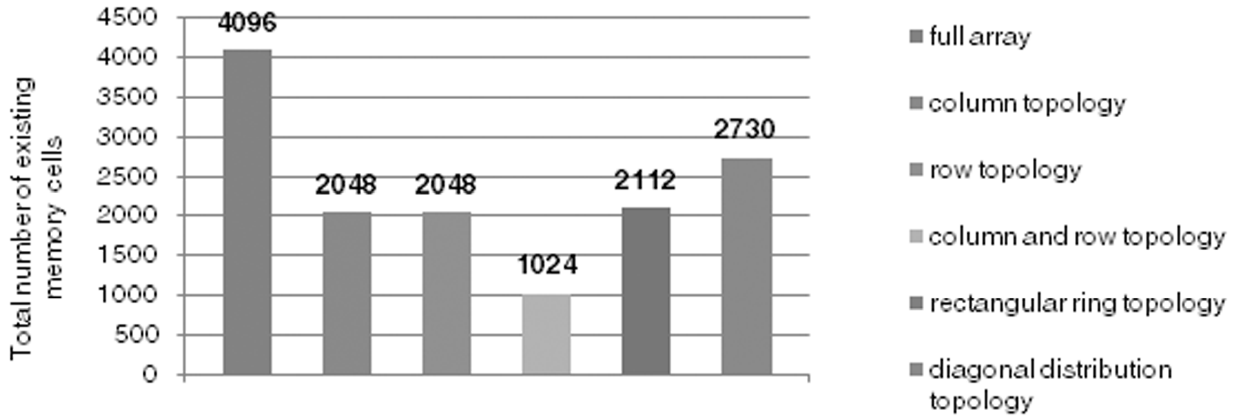

Figure 4: number of memory cells in different alternative topologies for 64 × 64 crossbar array

4. PARTIAL BIAS SCHEMES

To the best of our knowledge, the circuit-level simulations of the alternative crossbar array structures do not consider the intrinsic resistive and capacitive loads of the word/bit lines of the array. On one hand, wire resistivity increases when nanowire sizes decrease as a result of surface scattering and grain boundary scattering [23]. The current passing through the metal wires causes significant voltage degradation in large crossbar arrays, thus decreases the voltage drop on the furthest cell in the crossbar and resulting in write failure/disturbance [24]. On the other hand, the crossbar line capacitance will add both read/write delay time and extra current sneak paths, causing further degradation in memory performance [25]. It should be noted that, when considering the crossbar line resistance into account, the position of the selected cell will also deteriorate the voltage margin. The worst position will be located at the furthest corner from the voltage source and ground.

In order to solve the aforementioned irregular voltage drop, different bias schemes have been proposed to bias the unselected cells with a fraction of the selected cell voltage (V_{dd}) [26]. The four commonly used bias schemes are summarized in Table 1.

Table 1
Different Biasing Schemes

Bias scheme	*Selected word line*	*Selected bit line*	*Non-selected word lines*	*Non-selected bit lines*
Floating Terminals (FT)	V_{dd}	*Grounded*	*Floating*	*Floating*
Grounded Terminals (GT)	V_{dd}	*Grounded*	*Grounded*	*Grounded*
V/2 bias	V_{dd}	*Grounded*	$V_{dd}/2$	$V_{dd}/3$
V/3 bias	V_{dd}	*Grounded*	$V_{dd}/2$	$2V_{dd}/3$

5. RESULTS AND ANALYSIS

In this section, the memristor model presented earlier in section 2 is merged into each junction of a 64×64 crossbar array in order to study the read voltage margin and power consumption for different crossbar topologies and biasing schemes. All simulations were carried out using Cadence IC tools to measure the output voltage and power consumption of the array, then these data are extracted for post-processing using MATLAB. For a more realistic performance evaluation, interconnected line resistance and capacitance are also considered. The line resistance (R_{line}) between two adjacent cells is calculated to be 3.356Ω/Feature assuming copper wire . The word line to bit line capacitance (C_{wtb}) and coupling capacitance between two adjacent parallel wires (C_{couple}) are calculated to be 7.4310^{-8}pF/cell and 9.4110^{-7}pF/Feature respectively, assuming SiO_2 insulator. To simulate the worst case reading scenario, all the memristor cells are assumed

to be in ON state (low resistance state). Performance is examined by applying a 1V read voltage to a target cell and measuring the output voltage across a sense resistance (R_{sense}). The optimal value of Rsense that achieves maximum voltage margin is calculated to be 15.81MΩ [27].

To study the sneak path effect, the output voltage margin of the crossbar array is compared to the ideal case where no sneak current is present. Therefore, we define the normalized voltage margin (Δ/V) as

$$\Delta / V = \frac{\Delta V_{array}}{\Delta V_{device}} = \frac{\left(V_{LRS} - V_{HRS}\right) array}{\left(V_{LRS} - V_{HRS}\right) device} \tag{4}$$

Where V_{LRS} and V_{HRS} are the voltage drops across R_{sense} when the state of the target cell is ON and OFF, respectively. ΔV_{device} is the voltage margin of a single memristor circuit and ΔV_{array} is the voltage margin of a memristor placed in a crossbar array. Meanwhile, the power consumption during read operation is also calculated.

Fig. 5 shows that the GT bias scheme performs better than other schemes in terms of the voltage margin whilst performance of the FT bias scheme is the poorest. This is because the cells connected to the same word line of the target cell are grounded in GT scheme, so the sneak path current flowing into the target cell is relatively low so that the voltage margin grows higher. On the contrary, the sneak path current in the FT bias scheme will flow through the target cell, causing lower voltage margin. In addition, the Column and Row topology gives a further significant improvement in voltage margin but it is unattractive topology as it has the lowest number of memory cells. The diagonal distribution topology is more efficient than other topologies in terms both of the number of memory cells and voltage margin.

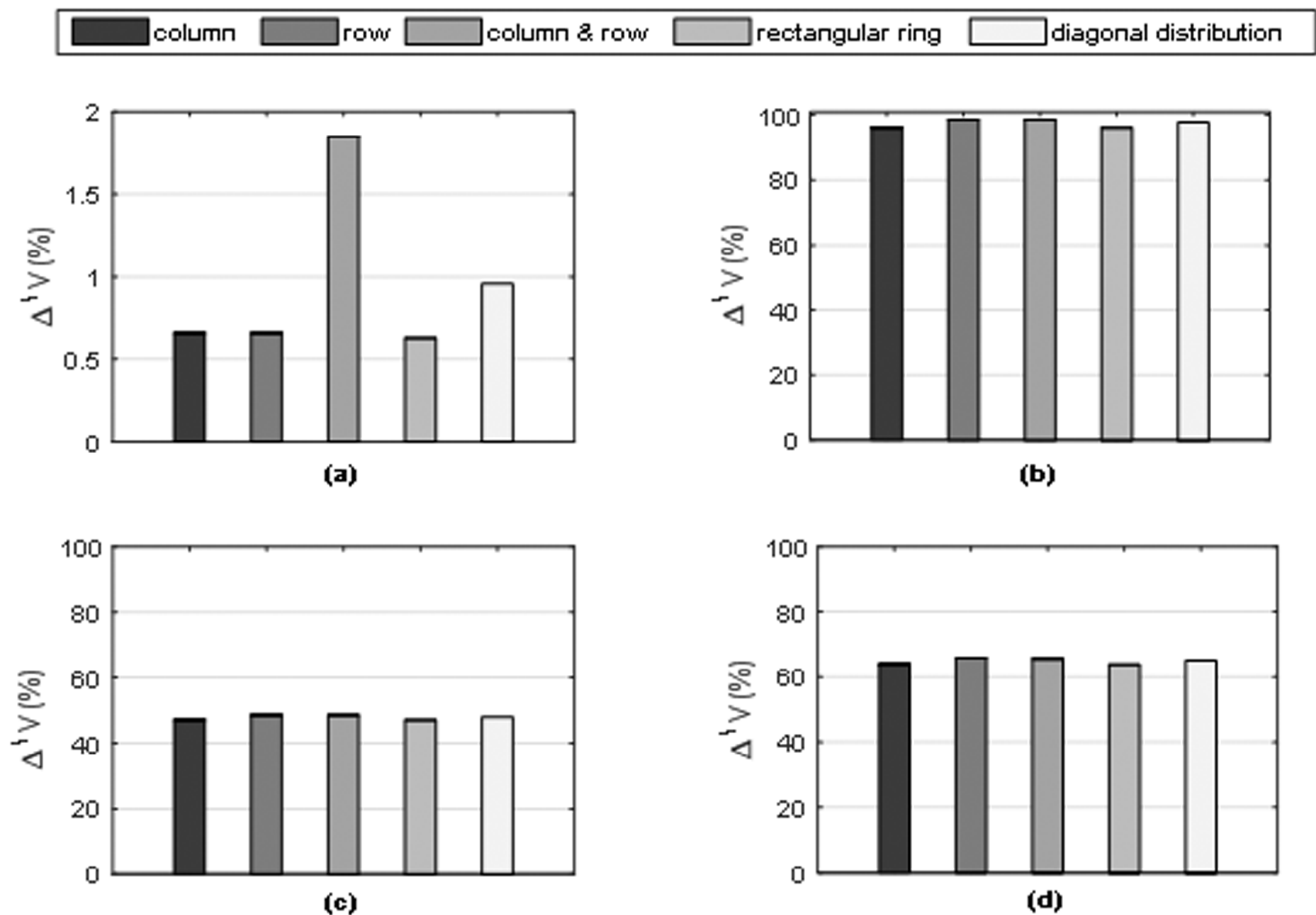

Figure 5: Normalized voltage margin for the worst case reading scenario of 64 × 64 array with (a) floating terminals, (b) ground terminals, (c) V/2 bias, and (d) V/3 bias scheme

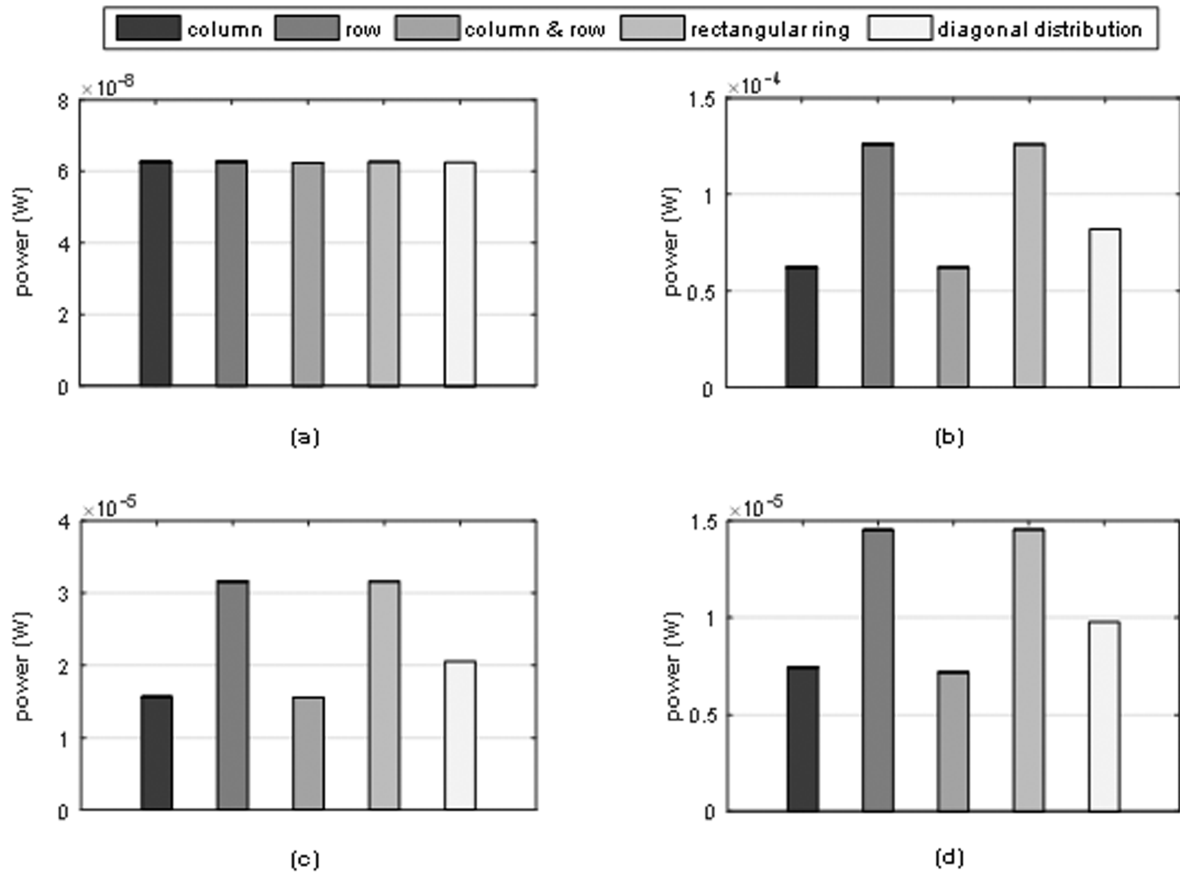

Figure 6: Power consumption for the worst case reading scenario of 64 × 64 array with (a) floating terminals, (b) ground terminals, (c) V/2 bias, and (d) V/3 bias scheme

The power consumption is shown in Fig. 6. The FT bias scheme consumes least power while the GT scheme consumes highest power. An explanation to these results is that the power is more consumed by the fully-selected cells. And because the number of fully selected cells in GT scheme is higher than other schemes, then it consumes higher power.

6. PERFORMANCE COMPARISON

In order to test the validity of the performance results, a benchmarking comparison is introduced in this section. The alternative crossbar topologies are compared with the full crossbar array with both linear and self-rectifying memristive devices. The linear memristor device is modelled based on VTEAM model [21], while the full array has 64 word and bit lines with 4Kbit storage capacity.

Table 2 summarizes the voltage margin of the alternative crossbar topologies with self-rectifying memristive device for different biasing schemes. It is equally important to include the full crossbar performance to have a clear insight of how much improvement is achieved. It is clear that there is a great performance boost when using a full crossbar array with self-rectifying memristive device compared to the linear memristor arrays under any biasing scheme. A further improvement can be achieved when combining theself-rectifying memristor with the alternative array topologies. As aforesaid, GT, V/2, and V/3 biasing schemes help to minimize the sneak path current flowing through R_{sense} and improving the read voltage margin.

In the same manner, the power consumption of both alternative and full crossbar topologies are presented in Table 3.

The same conclusion can be made that the alternative crossbar topologies consume less power during

Table 2
Normalized voltage margin for different biasing schemes.
Worst case read scenario is considered with 64×64 array size

Biasscheme	*Column topology*	*Row topology*	*Column and row topology*	*Rectangular ring topology*	*Diagonal distribution topology*	*Full array*	*Full array (linear memristor model)*
Floating Terminals	0.66%	0.66%	1.85%	0.63%	0.958%	0.21%	0.003%
Grounded Terminals	96.21%	98.58%	98.58%	96.21%	97.79%	94.91%	1.63%
V/2 bias	47.15%	48.59%	48.59%	47.15%	48.08%	46.49%	0.82%
V/3 bias	63.89%	65.81%	65.6%	63.87%	65.13%	63.43%	1.09%

Table 3
Power consumption for different biasing schemes.
Worst case read scenario is considered with 64×64 array size

Biasscheme	*Column topology*	*Row topology*	*Column and row topology*	*Rectangular ring topology*	*Diagonal distribution topology*	*Full array*	*Full array (linear memristor model)*
Floating Terminals	62.54nW	62.54nW	62.21nW	62.55nW	62.43nW	62.81nW	63.18nW
Grounded Terminals	62.17µW	126.1µW	62.11µW	126.1µW	82.14µW	125µW	126.7µW
V/2 bias	15.58µW	31.57µW	15.57µW	31.59µW	20.58µW	31.29µW	31.7µW
V/3 bias	7.43µW	14.52µW	7.18µW	14.55µW	9.79µW	14.86µW	881.4µW

the read operation than the full crossbar array. The floating terminals has the least power consumption but worst voltage margin. While V/3 bias scheme has a good balance of and power consumption compared to others, it is noted that it consumes greatest power when linear memristive device is used as a memory cell. This is the only case where V/3 has the worst power consumption.

7. CONCLUSION

In this work, the read operation performance of alternative memristive crossbar structures are studied. Based on the depicted results, these structures can produce a significant improvement in terms of voltage margin and power consumption, hence tolerating the sneak path current problem. A useful addition of the self-rectifying memristive device is proposed providing further enhancement of the crossbar array performance. To provide a uniform voltage drop across each cell, four biasing schemes are examined. It can be concluded that the diagonal distribution topology is more efficient than other topologies in terms of voltage margin and number of remaining cells and for any biasing scheme. These structures with self-rectifying memristors and proper biasing scheme are well suited for large data storage applications at minimal fabrication processes since they do not require any selector device at each junction.

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