IJCTA, 10(02), 2017, pp. 133-138

VLSI Implementation of Gabor Filter in Image Detection–Research Direction

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Abstract : Digital Gabor filter to minimize the sizing problem and the coding style that synthesizable. A Gabor filter is linear filter whose impulse response is defined by a harmonic function multiplied by Gaussian function.This paper mainly investigate the various type of VLSI implementation of gabor filter that are existing and put its altogether for a literature survey. Scope of this study focuses on the different algorithims and its VLSI implementation.

Keywords : FPGA,VLSI,Verilog HDL.

1. INTRODUCTION

Image processing is widely used in many fields, such as medical imaging, scanning techniques, printing skills, license plate recognition, face recognition and so on. A Gabor filter is linear filter whose impulse responseis defined by a harmonic function multiplied by Gaussian function.In image processing gabor filter is a linear filter used for edge detection. Frequency and orientation representations of gabor filters are similar to those of the human visual system and they have been found to be particularly appropriate for texture representation and discrimination.It is for simple and less complex circuits VLSI implementation are preferred.

2. LITERATURE SURVEY OF VLSI IMPLEMENTATION OF GABOR FILTER

2.1. Improvisation of gabor filter design using verilog HDL

In 2010, Idros, M.F.M Mohamed, S.A Razak, A.H.A Zoolfakar, A.S Al-Junid, S.A.M presented the improvisation of Gabor Filter design using Verilog HDL. This paper dealt with important enhancement made to the Digital Gabor filter to minimize the sizing problem and the coding style that synthesizable. The main characteristic of the approach was to replace the parallel multiplication-accumulation unit (MAC) to a serial multiplication-accumulation unit. This significant change helps to reduce the sizing problem without jeopardizing the functionality of the Digital Gabor Filter. The result provides area efficiency architecture for the effective design. The area of the design has been significantly reduced while the function of the filter is perfectly maintained. The numbers of slices used from previous design reduce from 5759 slices to 1625 slices. Even though, the precision of this Gabor Filter is 0.001% away from the calculated data. By minimizing the area, the speed of the design is relatively slower. It took 222 complete cycles to finish the convolution.[1]

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2.2. Design and Simulation of Cascaded Gabor Filter Using Verilog HDL

In 2016, Vijay Laxmi, Dr. P. K. Chaturvedi discussed the Design and Simulation of Cascaded Gabor filter for fingerprint recognition using Verilog HDL. The application of Gabor Filter technique to enhance the fingerprint image and it is used to define the ridges and valley regions of fingerprints is by convoluting the image pixel with Gabor filter coefficient. The experimental result was the signal convoluted with the Gabor coefficient. The effect of image enhancement has an impact on features extraction and the fingerprint identification of recognition rate, according to the research of traditional fingerprint image enhancement technology, Gabor filtering for fingerprint image enhancement technology is proposed. The design enhancement proposed for Gabor Filter has successfully reached. The area of the design has been significantly reduced while the function of the filter is perfectly maintained. By adjusting the memory and the controller unit, the functionality of a complete and correct digital Gabor Filter is obtained.[2]

2.3. Implementation of Gabor-type Filters on Field Programmable Gate Arrays

In 2010, Ocean Y. H. Cheung, Philip H. W. Leong, Eric K. C. Tsang and Bertram E. Shi proposed biological visual systems have been widely studied at the physiological, psychophysical and functional levels, One of the obstacles in this process is the difficulty of dealing with the vast amounts of processing necessary to test real-time temporal models of the visual system. In this paper, authors presented a high performance FPGA-based cellular neural network which implements a Gabor-type filter. The application of the Gabor-type filter in a neuromorphic system consisting of an analog VLSI retina chip interfaced to our Gabor chip is also presented. An implementation of Gabor-type Filters on field programmable gate arrays using cellular neural network (CNN) architecture is described. Compared to other analog VLSI implementations of Gabor-type filters, our implementation has advantages of shorter design time, scalability and flexibility. The design can accommodate different array sizes, as well as simultaneous computation of multiple filter outputs tuned to different orientations and bandwidths.[3]

2.4. Design and simulation of Gabor filter using verilog HDL

In 2007, S.Gayathri Dr V. Sridhar proposed the most important measurement element in fingerprint recognition process is the texture of the fingerprint.The computational complexity of a fingerprint recognition process depends on fingerprint enhancement. The quality of the fingerprint image can be enhanced using Gabor filter. The objective of Gabor Filter in fingerprint recognition is to segment the texture of fingerprint. This includes the design of a single filter to segment multiple (> 2) textures and the design of multiple filters to segment multiple textures. The computational efficiency becomes increasingly important as the size of images, number of Gabor prefilters, number of Gaussian postfilters, and number of textures increases. The implementation of a series of techniques for fingerprint image enhancement to facilitate the extraction of minutia is done effectively with well know algorithms based on ALU. Based on the verification on ALU, expected results are obtained.[4]

2.5. Simulation of Gabor Filter for Fingerprint Recognition using Verilog HDL

In 2008, Geetha M.N and Jagadeesh.B proposed the Simulation of Gabor filter for fingerprint recognition using Verilog HDL. The application of Gabor Filter technique to enhance the fingerprint image and it is used to define the ridges and valley regions of fingerprints is by convoluting the image pixel with Gabor filter coefficient. The experimental result was the signal convoluted with the Gabor coefficient.the conclution isimplementing Gabor Filter in fingerprint recognition was to segment the texture of fingerprint. Texture segmentation was the process of partitioning an image into regions based on their texture. The reason using Gabor filter was due to it characteristic. Gabor filters have the properties of spatial localization orientation selectivity and spatial frequency selectivity.[5]

2.6. High Speed and Low Power FIR Filter Implementation Using Optimized Adder And Multiplier Based On Xilinx FPGA

In 2014, Mr. Pravin Y.Kadu, Ku. Shubhangi Dhengre proposed the Finite impulse response (FIR) filters are widely used in various DSP applications. The low-power or high speed techniques developed specifically for digital filters can be found in. Many applications in digital communication, speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and many other synthesis operations of signal require large order FIR filters ,since the number of multiply-accumulate (MAC) operations required per filter output increases linearly with the filter order, hence implementation of these filters of large orders is a challenging task. Here, we propose designing of FIR filter using high speed low-power multiplier adopting the new implementing approach. The multiplier we are using is Vedic Multiplier. It will reduce the number of partial products generated by a factor of 2. The carry save adder will avoid the unwanted addition and thus minimize the switching power dissipation. [6]

2.7. Low Power FPGA Implementation of Digital FIR Filter Based on Low Power Multiplexer Base Shift/Add Multiplier

In 2013, Bahram Rashidi, Farshad Mirzaei, Bahman Rashidi, and Majid Pourormazd presented the implementation of a low power and low area digital Finite Impulse Response (FIR) filter. The method to reduce dynamic power consumption of a digital FIR filter is to use low power multiplexer based on shift/add multiplier without clock pulse and applied it to FIR filter until power consumption reduced thus reduce power consumption due to glitching is also reduced. [7]

2.8. A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications

In 2016, Basant Kumar Mohanty, and Pramod Kumar Meher proposed Transpose form finite-impulse response (FIR) filters that are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. Authors explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less areadelay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. [8]

2.9. Fast Hardware Implementation of Gabor Filter Based Motion Estimation

In 2007, A.Spinel, D. Pellirin, D. Fernande, J. Herault propose Motion estimation in image sequences fast energy-based method which combines in a direct manner the energetic responses of Gabor spatio-temporal organized in triads. An implementation of this technique on a general purpose Digital Signal Processor (DSP) board is described and the advantages compared with Very Large Scale Integration (VLSI) and parallel machine approaches. Our hardware implementation attains a reasonably fast output rate (several images/second) for a better resolution than in the most recent VLSI implementations. 2D estimation is carried out by associating the results of several triads (2 or 4). In order to accelerate the process, authors proposed the reduction of necessary 1D ¯lters and the approximation of a Gabor ¯lter by a recursive third order ¯lter. This allows good-quality results within a reasonable computing time, according to the results of our simulations. We proved that a DSP implementation of the algorithm is possible using a low-cost PC extension board, making the development process simpler than in the case of VLSI or parallel machine applications.[9]

2.10. VHDL Design for Image Segmentation using Gabor filter for Disease Detection

In 2012 Rucha R. Thakur, Swati R. Dixit and Dr.A.Y.Deshmukh proposed efficient Gabor filter design with improved data transfer rate, efficient noise reduction, less power consumption and reduced memory usage. The filter design is suitable for detecting the early stages of disease using textural properties of anatomical structures. The code for Gabor filter will be developed in VHDL using Modelsim and then implemented on SPARTAN-3E FPGA kit. These systems must provide both highly accurate and extremely fast processing of large amounts of image data.It will improve data transfer rates, provide efficient noise reduction, less power consumption and require less memory storage. The processing time required for simulation is very less as compared to software simulation because of the use of CORDIC algorithm, thus offers much greater speed than a software implementation.[10]

2.11. Design Of a Pixel-Parallel Feature Extraction VLSI System For Biologically-Inspired Object Recognition Methods

In 2003, Takashi Morie, Makoto Nagata, and Atsushi Iwata presented biologically-inspired feature extraction method, which consists of coarse region segmentation by a resistive-fuse network and feature extraction by Gabor wavelet transforms. Their pixel-parallel VLSI implementation based on the pulse modulation circuit architecture is described, and measurement results of Gabor filter operation by a test LSI chip with 1-D 20-pixels are presented. The pixel parallel VLSI implementation based on the pulse modulation circuit architecture was described. We designed a pixel unit circuit and a test LSI chip with 1-D 20-pixels using 0.6 _m CMOS technology, and verified the basic operation by measuring the impulse response in the test LSI chip.[11]

2.12. Real Time VHDL Design of High Speed Gabor Filter for Disease Detection

In 2014, Mrs. Rucha D. Thakur proposed an efficient Gabor filter design and pipelined architecture for input. The hardware implementation of this technique attains a reasonably fast output rate (i.e. several images/second) for a better resolution than in the most recent VLSI implementations. authors first present a hardware efficient FPGA-based shift-add CORDIC algorithm which implements a Gabor-type filter and improves data transfer rate, provide efficient noise reduction, less power consumption and reduced memory usage. The code for Gabor filter will be developed in VHDL using Modelsim and then implemented on SPARTAN-3E FPGA kit for detecting the early stages of disease using textural properties of anatomical structures. The fine-pipeline based architecture improves of the accuracy, performance of the system and extremely fast processing of large amounts of image data). This concept will be helpful in detecting early stage of disease and saving the lives of peoples.[12]

2.13. Design of a Modified Gabor Filter by Using Verilog HDL

In 2013 M Srinivas, M Praveena proposed improvisation of Modified Gabor Filter design using Verilog HDL. This work deals with important enhancement made to the modified Digital Gabor filter to minimize the sizing problem and the coding style that synthesizable. The intention is to study, analyze, simplify and improvise the design synthesis efficiency and accuracy while maintaining the same functionality. The main characteristic of the proposed approach was to replace the parallel multiplication-accumulation unit (MAC) to a compact programming approach where the convolution matrix takes place. This significant change helps to reduce the sizing problem without jeopardizing the functionality of the modified Digital Gabor Filter. The result provides area efficiency architecture for the effective design. The enhancement made in the multiplication-accumulation unit has been proven effectively reliable and functional. By adjusting the memory and the controller unit, the functionality of a complete and correct digital Gabor Filter is obtained. By minimizing the area, the speed of the design is relatively slower.[13]

2.14. Design and Implementation of Gabor Type Filters on FPGA

In 2014, Sunitha M K , Harsha B K proposed realization of Gabor filter architecture using the floating – point operations are discussed The paper presents, a brief mathematical overview of the Gabor-type filters which involves floating point arithmetic operation analysis results, the architectural details of the Gabor-type filter, and, the structure of the FPGA implementation is given. Finally implementation results are discussed. Simulation and Synthesis is done using Xilinx ISE design suite. Verilog HDL will be used as a description language for mapping algorithm in VLSI and hardware implementation on SPARTAN-3E FPGA. . A CNN- Gabor type filter realization method was proposed coded in VHDL and the simulation results are obtained resulting in accuracy. Digital implementation of Gabor-type filters was proposed, which drastically reduces the number of multipliers required for FPGA implementation. The Gabor filters are suitable for a real-time application such as optical character recognition (OCR), facial recognition or license plate recognition and any other system that requires two-dimensional band-pass filters.[14]

2.15. VHDL Implementation for edge detection using log gabor filter for dieases detection

In 2014, V.V. Kumbhalwar1, S.R. Dixit discussed different and many ways for edge detection, However, the most may be grouped into three categories, first order gradient, second order and optimal edge detection.. Sobel edge detection is gradient based edge detection method used for finding edges of image. Also Sobel edge detection method provide one more advantage that it having better noise sensitivity as compared to other edge detection method. Here new concept Log-Gabor filter is used for best contrast ridges, efficient noise reduction and improved edges of an images. Most image processing tools such LabVIEW are not suited for strong real-time constraints, so to overcome this problem hardware implementation FPGA used. Proposed model for disease detection is design in LabVIEW platform with NI Vision Assistant tool 14.0. This paper discusses the design of the sobel edge-detection for tonsillitis images with the help of LabVIEW 14.0 and LabVIEW FPGA tool. Paper conclude that Edge detection using software and hardware is challenging task like total hardware software compatibity. Main advantage of sobel operator is better noise sensitivity and it provide sharp edges as compare to other edge detection method.[15]

2.16. Design of a Modified Gabor Filter with Vedic Multipliers Using Verilog HDL

In 2015, Naheean Rahim, Shamayla Islam, and Iqbalur R. Rokon proposed the gabor filter designed with a RAM type Memory, but a few changes were made in the Controller and the Arithmetic Logic Unit (ALU). The Arithmetic Logic Unit had a new type of multiplier called a Vedic Multiplier. So building a Gabor Filter with Vedic Multipliers is something that authors have introduced in this paper. Using Vedic Multipliers, our filter was made faster without affecting the functionality of filter. The paper included two phases where simulation of the Verilog Codes and synthesis of the whole Gabor Filter. This work has proved the efficiency of Urdhva Triyagbhyam – Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. Analog currentmode complementary metal–oxide–semiconductor (CMOS) circuits are used throughout to perform edge detection, local inhibition, directionally selective long-range diffusive kernels, and renormalizing global gain control. . This modified Gabor Filter has a lot of future scopes as it can be used for Cancer Detection, Brain Tumor Detection, Video Processing and even extracting Satellite Images.[16]

2.17. Focal-Plane Analog VLSI Cellular Implementation of the Boundary Contour System

In 1999, Gert Cauwenberghs and James Waskiewicz proposed an analog very large scale integration (VLSI) cellular architecture implementing a version of the boundary contour system (BCS) for real-time focal-plane image processing. Inspired by neuromorphic models across the retina and several layers of visual cortex, the design integrates in each pixel the functions of phototransduction and simple cells, complex cells, hypercomplex cells, and bipole cells in each of three directions interconnected on a hexagonal grid. The cellular model is fairly easy to implement and succeeds in selecting boundary contours in images with

significant clutter. One area for improvement of the cellular architecture is the angular resolution While this size is small for practical applications, the analog cellular architecture is fully scalable toward higher resolutions. Based on the current design, a 10 000-pixel array in 0.5-_m CMOS technology would fit a 1-cm2 die.[17]

3. CONCLUSION

Hence some existing gabor filter and its VLSI implementation has been discussed. Image quality after enhancement play a vital role. To conclude all the VLSI implementation methods are useful for real time image processing.

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