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Proposed Design of NoC Router Using Small Side Buffer and iSLIP Scheduler

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ABSTRACT

As the numbers of processors or IP modules are increased on the single chip, communication between various modules becomes very crucial using traditional bus system. Network on chip is emerging technology which replaces the traditional bus and crossbar approaches for SoC on chip interconnect. Network on chip has been proposed as a promising solution for scalability and performance demands of next generation SoCs. The router is the main part of NoC. Router consists of an input buffer, arbiter, crossbar and an output port. The input block of NoC router uses buffers to store the incoming packets. These buffers improve the performance but they consume more power and area. Bufferless deflection routing is the solution for an improvement in energy efficiency, but latency may increase because of unnecessary hopping of data packets. Another important block of router is scheduler which allows contention free transfer of data packets among various IP modules or processors. Hence effective design of NoC router is required from performance perspective. In this paper we have proposed effective design of NoC router using small side buffer in input block and starvation free iSLIP scheduler.

Keywords: Network on chip, System on chip, Bus system, Router, Input buffers, iSLIP scheduler.

1. INTRODUCTION

As there are a millions of transistors, gates are integrated on a single chip, it gives emergence of System on chip architecture. The advantage of system on chip is smaller in size, faster in speed, low power consumption, high reliability and cost effective. But there are many challenges for the evolution of SoC. SoC architecture is facing the problem of interconnection among various IP modules which restricts the scalability of the system. As the number of IP modules in SoC increases, it is difficult to meet the performance parameters such as required bandwidth, latency and power consumption using bus based interconnection.[1] A solution for such a communication bottleneck is the use of embedded switching network called Network on Chip (NoC) to interconnect various IP modules in SoC.

NoC provides the solution for communication infrastructure in SoC. It reduces wire delay, power dissipation, latency and enhances signal integrity. It overcomes the issue of scalability by allowing multiple concurrent connections with many devices.[2] It can reduce the wire routing traffic to a great extent. NoC will take care of the communication portion with utmost ease without the interference of the computational portion. Thus a NoC technology can provide following features:

1. separation between computation and communication
2. Support modularity and IP based system
3. Overcomes the issue of scalability, hence larger SoC design is possible
4. Support for clock synchronization issues

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5. Use of regular structure to reduce the complexity of interconnection wires
6. Support for system testing

This paper is organized as follows. In section 1.2 we discussed the NoC architecture. In section 1.3 we proposed the architecture of input block with side buffer. Section 1.4 described the proposed architecture of scheduler and conclusion is given in section 1.5.

2. ARCHITECTURE OF NETWORK ON CHIP

NoC is a technology that is intended to overcome the issues of bus interconnection in traditional SoC. Following Fig.1 shows the architecture of the NoC. Network interface, router and links are the main elements of NoC architecture. The computational and communication parts are kept separate by the network interface. Network interface makes the logical connection between IP cores and the network. The router is the heart of NoC which decides the routing path from source node to destination. Link connects the number of routers of the network for the desired topology.

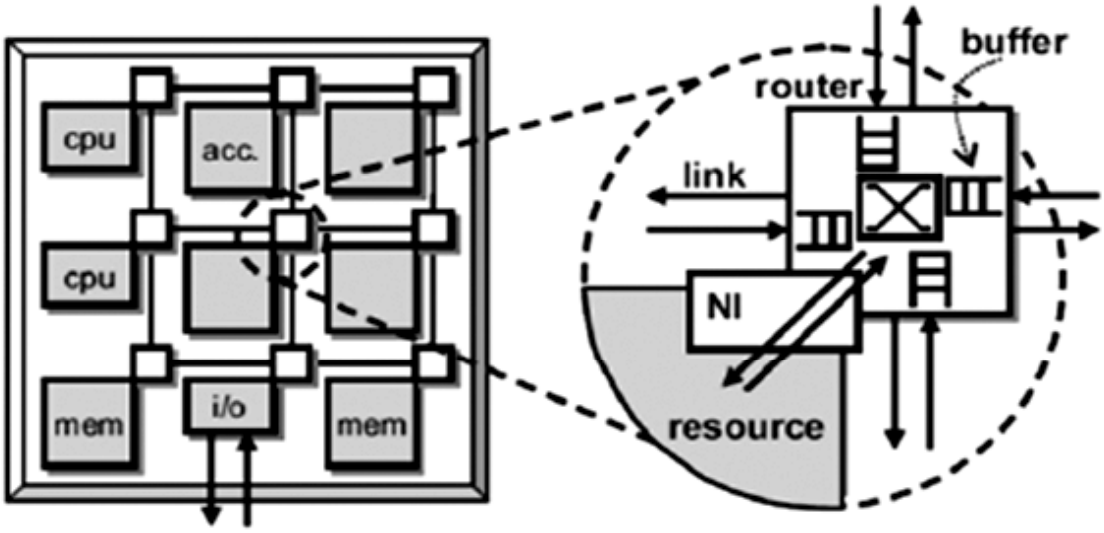

Figure 1: Basic Architecture of NoC[1]

The key issues for designing of NOC architectures are as follows:

2.1. Topology

In network architecture the topology defines how the nodes are interconnected with each other. For NoC architectures, there are various topologies are available, such as mesh, torus, tree, butterfly, polygon, and star topology [3]. But mesh topology is recommended by many researchers because of its layout efficiency, scalability and low power consumption [1, 4].

2.2. Switching Techniques

Data transmission from source node to destination node is determined by switching techniques.

1. Circuit switching: The path is decided prior to the transmission of data. There is no interference as it is a dedicated circuit or network.
2. Packet switching: The data is divided into packets called as flits. There is a header attached to each packet which establishes connection between router. Once the connection is established data packets are transferred to the destination node.

3. Store and forward packet switching: In this routing, the node stores the complete packet before it is being forwarded to the next node, hence it is must to ensure that the size of the buffer at each node must be sufficient to store the whole packet.
4. Wormhole switching: In this technique, the packet is divided into three parts: header, body and tail. Once the header is forwarded, the node makes the routing decision and then forwards the data packets.

2.3. NoC Routing

NoC routing plays very important role in routing of data packets from source to destination node. Routing algorithm decides contention free path for data packets which also prevents dead lock and live lock starvation.

Generally X-Y routing is preferred for NoC routing. In XY routing the packets are routed first in x-direction or horizontal direction till the correct column has arrived and then routes in y-direction or vertical direction to the destination target address. Mostly used for mesh and torus topology. The addresses are its x-y coordinates. It never enters into deadlock or live lock condition.[5]

Performance of NoC can be evaluated by power consumption, area, through put and latency. These performance parameters are majorly depends on router architecture. Hence efficient design of router in Noc is paramount important. Router consists of input port, arbiter, and crossbar and output port. Design of input port deals with area and power consumption while latency is depends on scheduling algorithm. Noc router design with efficient design of input block and scheduler is discussed in the following sections.

3. Proposed Input Block of Router

Most of the router is designed using buffer. Buffer is used to store data packets temporarily and then transfer to the destination port. Advantage of buffer is to improve performance in term of increasing the bandwidth efficiency. But these buffers consume significant dynamic power when read/ write operation is taking place and static power when they are empty. Secondly chip area is also increased due to buffers. In the TRIPS prototype chip, input buffers of routers were occupying 75% of total on chip network area. Hence there is a need for bufferless routers which eliminate input and output buffers [6].

Various bufferless routing algorithms have been proposed to overcome the disadvantages of a buffered router [7, 8, 9, 10, 11]. CHIPPER and BLESS are the best examples of bufferless routers [8, 11]. Yu Cai et al. Prove that bufferless routing saves up to 30% power consumption and 38% area reduction in mesh or tours topology compared with buffered architecture [12]. CHIPPER NoC implementation shows that when compare with buffered routing, it reduces average network power by 54% and area by 36.2% for 8X8 mesh topology [8].

The key idea for bufferless routing is that data packets are never buffered in the network. When two packets contend for the same link, one is deflected. Thus Bufferless deflection routing causes unnecessary hopping of data packets for high network utilization. It increases data packets traversals and reduces network throughput and also increases dynamic power. MinBD (minimally buffered deflection routing) provides the solution for bufferless deflection routing [7]. In this router, small side buffer is added to reduce deflection rate. These side buffers are used to store data packets in case of the contention of data packets. This will reduce deflection caused by using small buffering. Working principles of MinBD router are as follows,

- In case of contention of data packets, it is better to buffer the data packets and arbitrate in a later cycle. In this case, small buffering can avoid many deflections. This helps us reducing in the power consumption and size of the chip.
- It may possible that data packets will be routed to destination port in first attempt. In this scenario, buffering of data packets lead to unnecessary power overhead. Hence router should buffer a data

packet if required. Thus data packets that would have been deflected in a bufferless deflection router are removed from the network temporarily into side buffer. It is called injection of data packets in side buffer. This reduces network deflection rates.

- Finally when the data packet arrives at its destination, it should be ejected from the network, so that it does not continue to contend with other data packets.[13]

Following Fig. 2 shows the block diagram of MinBD deflection router.

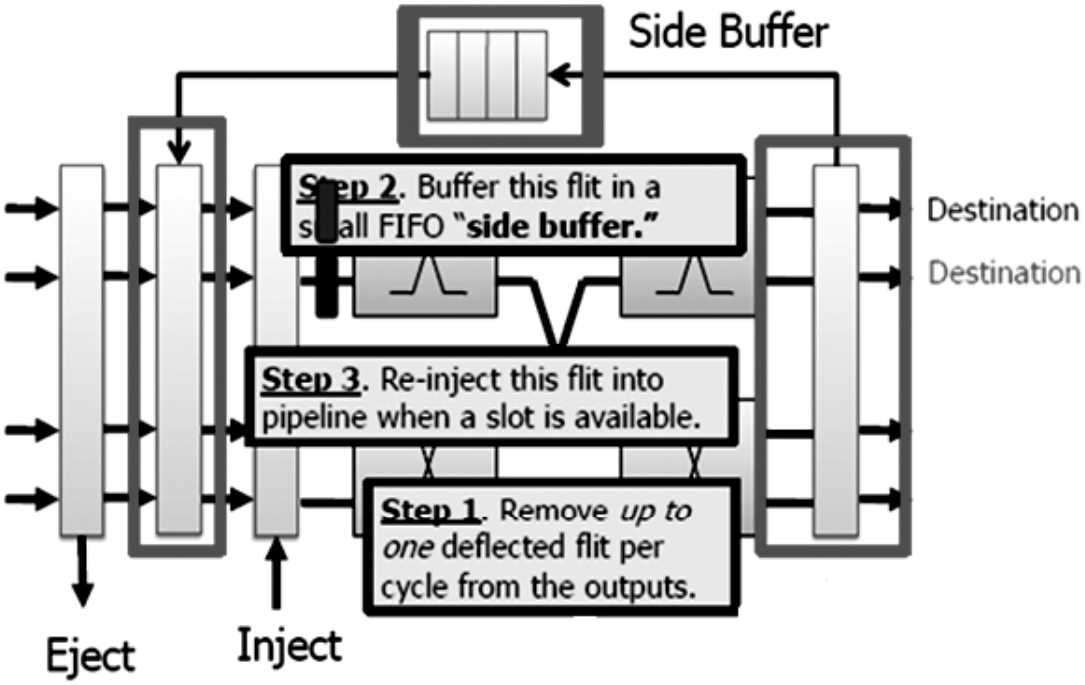

Figure 2: MinBD deflection router [13]

4. PROPOSED ISLIP SCHEDULER

Scheduler plays very important role for traversal of data packets in NoC. The core function of any scheduler (arbiter) is to transfer of data packets through various nodes and to resolve the conflicting requests for the same destination. Since, the arbiters directly determine the operation speed of the router, the design of faster arbiter is of paramount importance. NoC performance depends on how fast scheduling is done. Hence, designing of the appropriate scheduling algorithm is necessary for fast and efficient transfer of multiple data packets through crossbar switch. A lot of research work is done on fast scheduling algorithms for crossbar switches.[14, 15, 16] Fixed priority scheduler, round robin arbiter and iSLIP arbiter are the most important scheduling algorithm in NoC.

In fixed priority arbiters, each node is having fixed priority, hence in a high network load condition there is no limit to how long a lower priority request may need to wait until it receives a grant. A round-robin arbiter is improved version of the fixed priority which allows every requester to take a turn in order. A round robin arbiter operates on the principle that a request which was just served should have the lowest priority on the next round of arbitration. A round robin scheduler gives a reliable prediction of the worst-case wait time for requesting ports. The maximum wait time for any requester is proportional to number of requesters minus one. Tough round robin arbiter is starvation free but due to cyclic nature it increases latency.

iSLIP (Iterarive serial in line protocol) scheduling algorithm overcomes the problem of the round robin arbiter. iSLIP algorithm is based on programmable priority encoder (PPE) with round robin algorithm.

iSLIP scheduler is designed in such a way that it can skip the non-requesting node and find the grant signal for the requested node specifically by keeping priority in order. iSLIP uses principle of round robin arbiter with programmable priority encoder (PPE).The main characteristic of iSLIP is that it is simple and easy to implement in the hardware.[17]

In the proposed design iSLIP scheduler will be implemented with programmable priority encoder. An extra port is used to decide priority for granting the request for input ports. In iSLIP scheduler, for each cycle one of the requester node has the highest priority for accessing a shared resource.

5. CONCLUSION

In this paper we have discussed the advantages of the MinBD(Minimally Buffered deflection) router over the conventional buffered router. MinBD router stores only deflected data packets in small side buffer instead of storing all data packets in input buffers. Hence it requires only a small buffer size for input port as compared to the conventional input buffered router. It saves significant energy and area of a router. We have also discussed advantages of iSLIP scheduler over round robin arbiter. Proposed iSLIP scheduler will be implemented using programmable priority encoder with round robin scheduler. iSLIP algorithm meets the criterion of a fair chance scheduling algorithm which gives good performance, fast and simple to implement in hardware. In future, we intend to implement NoC router architecture with small side buffer in input block and iSLIP scheduler on FPGA.

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