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A Comparative Study of D Flip-flop using CMOS, MTCMOS and Lector CMOS for Low Power Low Noise Applications

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Abstract: Reduction in power consumption makes a device more reliable. System consuming less amount of power is highly preferable. The need for such systems played an important role in the evolution of CMOS technologies. As a result, CMOS devices are well known for their low power consumption. The effort of designers in reducing the power dissipation of CMOS products has lead the manufacturers to reduce the power supply voltage. This requires the transistor threshold voltage to be reduced and also to maintain adequate performance and noise margins. But this ironically increases the sub-threshold leakage current and offsets the power savings that are obtained by lowering the power supply voltage. In this paper we discussed about the MTCMOS and LECTOR techniques that reduce the leakage currents without reducing the power supply voltage and the developed technique is suggested for consideration.

Index Terms: Power, threshold, noise, delay systems, CMOS Technology.

1. INTRODUCTION

In achieving high performance and low power consumption, CMOS devices have made their mark for more than 30 years [1, 2]. The total power consumption in CMOS is mostly dependent on the leakage power. Actual leakage currents vary depending on biasing and physical parameters at the technology node. This leakage current can even exist in the circuit when there is no power supply. Temperature and doping levels also affect the leakage current. Generally when source and drain are reverse biased, they leak current. Typically these values are very small but may increase with scaling since doping levels are very high in present technologies. When drain to source voltage increases to a high level in short channel devices (the devices in which channel length is of same order of magnitude as the depletion region thickness of source and drain junction), the potential barrier in the channel reduces causing Drain Induced Barrier Lowering (DIBL) [2]. This DIBL generates sub-threshold current even at the voltage that is lower than threshold voltage. Sub-threshold leakage current or weak inversion current

is thus most important contributor of static power consumption in CMOS. To avoid this, different techniques are used and are described in [3-9]. However, recently propose Multi Threshold CMOS (MTCMOS) and Lector techniques are expecting to deliver better results than any other techniques [8-10] and hence the authors propose here the new techniques developed by them in MTCMOS and Lector to reduce the leakage current.

In this paper, we discuss about MTCMOS and LECTOR techniques that are used to reduce sub-threshold and leakage currents. We make circuits using CMOS, MTCMOS, Lector techniques and analyze comparatively. Different techniques and its drawback with justification of use such kinds of techniques are described in section II to IV. A D Flip Flop is designed as a case study and all these techniques are compared for low power low noise applications in section V and VI and concluded in section VII. It is seen that MTCMOS consumes less power and have less output noise compare to other two.

2. COMPLEMENTARY METAL OXIDE SEMICONDUCTOR [CMOS]

A CMOS design style uses complimentary and symmetrical pairs of p-type and n-type metal oxide field effect transistors for logic functions as shown in Figure 1[2]. All the PMOS devices together called as pull-up network and their substrate terminals are connected to VDD power supply, all the NMOS devices connected together are called as pull-down network and their substrate terminals are connected to VSS. Since one transistor of pair is always off, the series combination draws significant power only momentarily during switching between on and off states. CMOS also allows high density so that many circuits can be fabricated on a single chip [2].

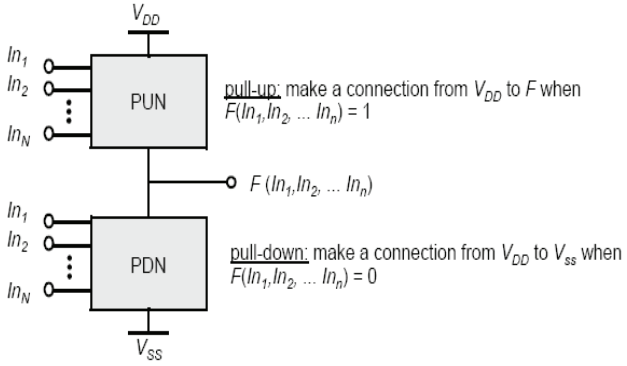

Figure 1: CMOS basic structure

However, mismatch in CMOS Devices is relatively high. The threshold voltage mismatch of static CMOS cells is negligible. But this mismatch has two-sided effect on off-set current. Hence total cell's current value may vary depending upon the direction of threshold voltage mismatch shift [2]. Further, when MOSFET's input gate voltage switches from one state to another state, it produces a spike which becomes a serious issue at high frequencies. These are highly static sensitive and can be easily damaged by static electricity. These are the few causes for which alternate techniques like MTCMOS and Lector are discussed in section III and IV.

3. MULTI-THRESHOLD CMOS

MTCMOS is a power gating technique. This technique uses different threshold voltage transistors in designing a CMOS circuit. The circuit is operated in two modes i.e. active and sleep modes. When a logic circuit is active, the sleep signals are de-asserted which turn on high threshold transistors and create virtual ground and virtual supply around the logic. In inactive mode, the sleep signals are asserted which separate the logic from the power/ ground, there by lowers the leakage current.

Sleep transistor sizing is a very important design aspect. The performance degradation of sleep transistor depends on its size and the amount of current that flows through it [10]. The voltage drop across the sleep transistor decreases the effective value of supply voltage and increases threshold value of pull-down network because of body effect. This increases the transition delay time of the circuit. We can overcome this problem by placing a large transistor which leads to large area overhead and dynamic power consumption. Hence we cannot save the power for a short duration of time. So the time for which we cannot save the power, is dependent on the transistor sizing [11]. A PMOS transistor is placed down the pull-down network so that the circuit is put in intermediate node and data retention is also realized as shown in Figure 2.

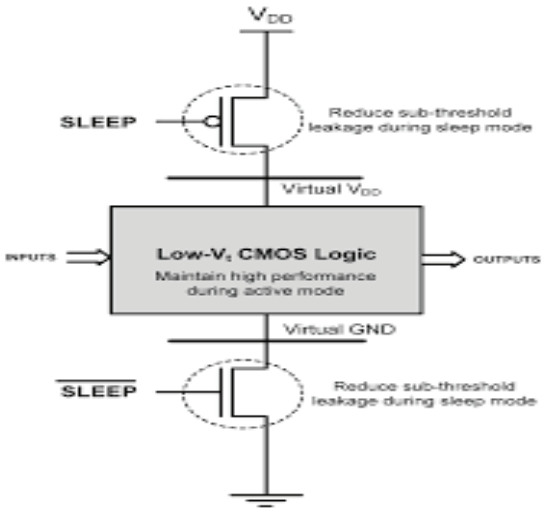

Figure 2: MTCMOS basic structure.

In this case, however, Sleep transistor sizing and placing should be taken care in such a way that it supplies sufficient current to the circuit. Also, even if the circuit is working in sleep mode then also an active power management circuit must be added and that has been taken care in this paper.

4. LECTOR CMOS

Lector CMOS is a drain gating technique [12] that involves two more transistors called Leakage Controlled Transistors (LCTs), a PMOS and an NMOS transistor that are placed between pull-up and pull-down networks. Lectors are introduced to obtain leakage controlled circuit. In this case, leakage power reduced by assembling the transistors from power supply to ground and is the notion behind Lector technique. One of the two LCTs always operates in its near cut off region.

The significant feature of LECTOR is that it works effectively in both active and idle states of the circuit; result in a better leakage reduction.

A state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with one OFF transistor in the path [12-14]. This can implemented by placing lector network in three different positions (i) placing LCTs only for the output gate (ii) placing LCTs in the main circuit (iii) placing LCTs in both main circuit and output gate. According to our analysis out of the three, (ii) gives least power consumption.

Figure 3 shows a lector CMOS gate circuit. Between the two nodes N1, N2, LCTs are introduced. The gates of both LCTs are controlled by the source nodes of each other. It means that two LCTs are controlled by each other and there is no need of external signals as shown in the Figure 3. These two LCTs create a high resistance path between VDD power supply and ground, and there by reduces leakage current.

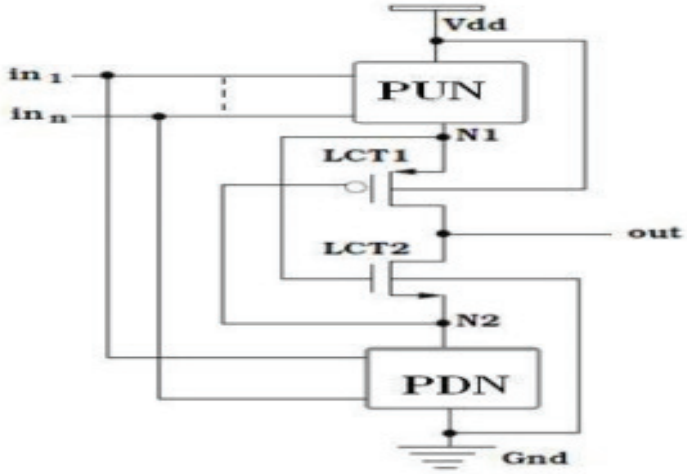

Figure 3: Lector CMOS gate.

Drawbacks of LECTOR Technique are (a) Placing the LECTOR network in any design increases the complexity of the circuit; (b) Though the leakage current decreases, the total power consumption may increase due to other effects in some cases.

In summary, in all these cases each has its own advantages and disadvantages. Therefore, a comparative study among these three will give a clear cut understanding regarding the power consumption and leakage current. The authors have considered a positive edge triggered D-Flip Flop as the case study and have analyzed in the next section.

5. APPLYING CMOS, MTCMOS AND LECTOR CMOS TECHNIQUES ON POSITIVE EDGE TRIGGERED D-FLIP FLOP.

It is seen that each of the techniques described above has its own advantages and disadvantages. Therefore, a comparative study will be useful for the prediction of low power and low noise for a circuit. The authors have decided to study the same in a delay Flip Flop as a case study. Delay Flip-flop is the most common element used in the design of memory elements [1, 14]. So, we have considered Delay Flip-flop which is designed using NAND gates as shown in Figure 4.

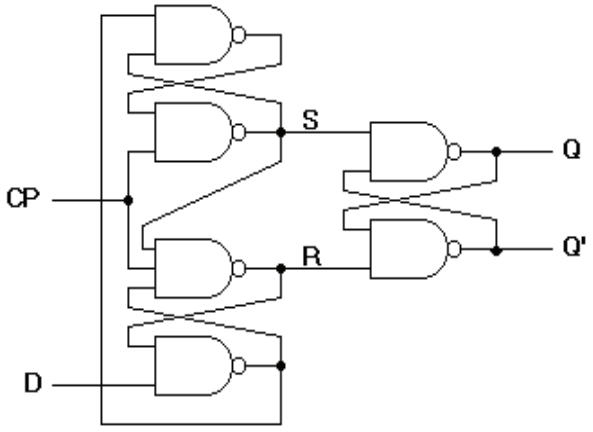

Figure 4: Positive Edge Triggered D Flip-flop

A) CMOS Positive Edge Triggered D-Flipflop

Taking D as data input, 'CP' as clock input, Q as output, CMOS positive edge triggered D-flip flop is designed by replacing each NAND gate with equivalent CMOS.

The output waveform of CMOS positive edge triggered D-flip flop shown in the Figure 5 indicates that the output follows clock input at the positive edges of 'CP' input.

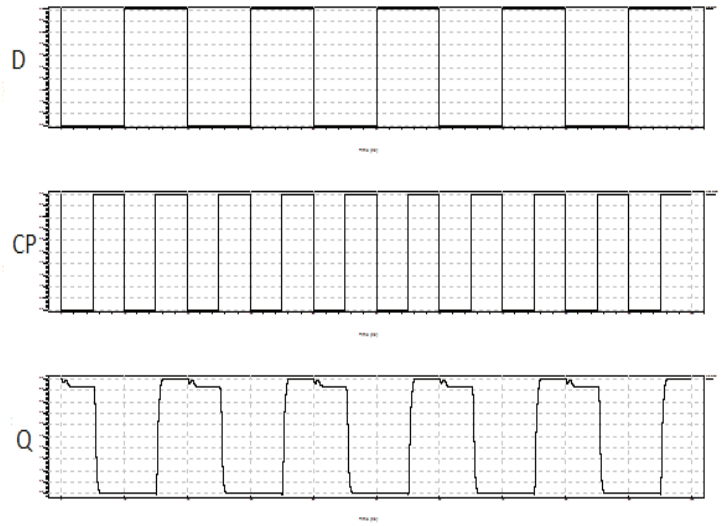

Figure 7: Output waveform of LECTOR based positive edge triggered D-flip flop.

B) MTCMOS Positive Edge Triggered D-Flipflop

A CMOS D-flip flop is designed and added PMOS and NMOS transistors at the top and bottom creating virtual power supply and ground. Sleep signal is applied to PMOS and its inverse to NMOS in such a way that both PMOS and NMOS should be in ON state. The output of MTCMOS positive edge triggered D Flip-flop is shown in Figure 6.

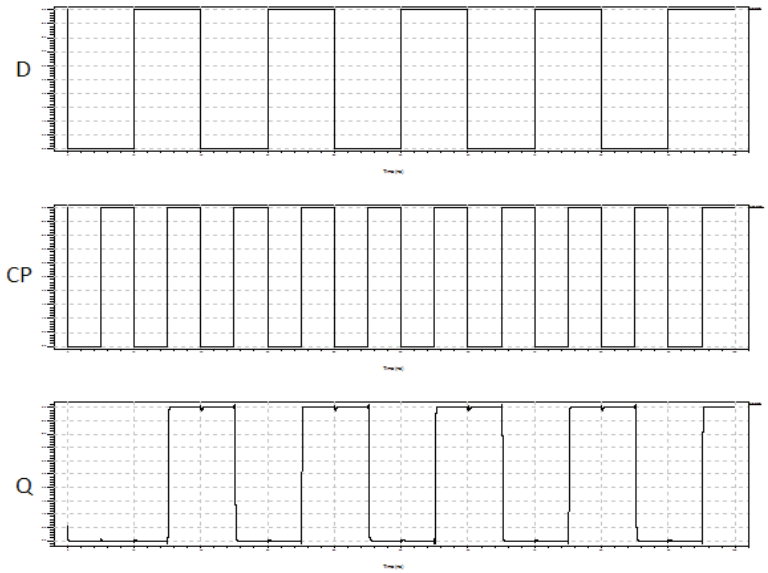

Figure 6: Output waveform of positive edge triggered D-flip flop using MTCMOS.

C) LECTOR based Positive Edge Triggered D-Flip flop.

For all the NAND gates, placing one NMOS and one PMOS between the pull-up and pull-down networks and connecting their inputs to each other source terminals, we constructed the LECTOR based positive edge triggered D-Flip flop and the corresponding results are shown in Figure 7.

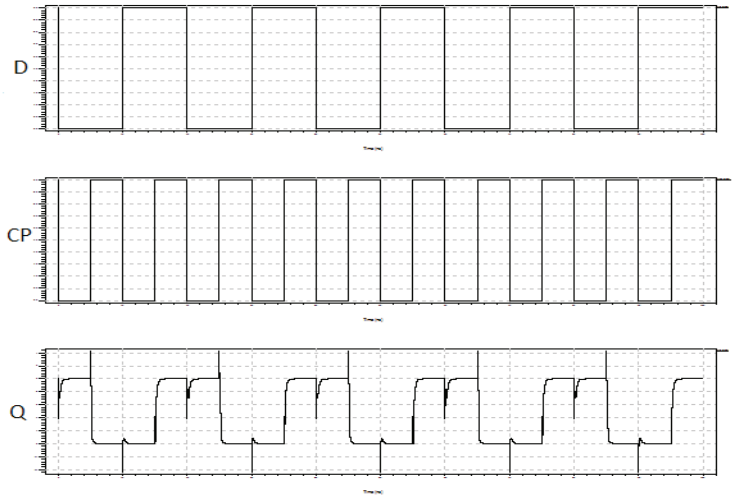

Figure 7: Output waveform of LECTOR based positive edge triggered D-flip flop.

6. COMPARATIVE ANALYSIS

The three technique CMOS, MTCMOS and LECTOR results are compared in Table 1. From table 1, it is seen that MTCMOS devices have low static power consumption, which is mainly due to low leakage current. So reduction in its leakage current results in better performance and low power dissipation. Leakage power mainly depends on sub-threshold leakage current which increases with increase in threshold voltage. Multi threshold voltages consideration reduces the threshold voltage and thus the static power. Multi Threshold Complementary Metal Oxide Semiconductor (MTCMOS) and LECTOR CMOS techniques are meant to reduce the leakage current as well as leakage power to achieve better results. It is seen that MTCMOS is very effective circuit level technique that improves performance in terms of power by utilizing low and high threshold voltage transistors and seen that MTCMOS have less power dissipation as well as less noise (as shown in Table 1). However, the LECTOR CMOS technique dissipates more power and generates more noise also as additional transistors are used in this circuit. Thus power reduction and noise in MTCMOS is better among the three mentioned techniques.

Table 1: POWER AND NOISE MEASURES

Circuit Name	Positive Edge Triggered D Flip-flop		
	CMOS	MTCMOS	L E C T O R CMOS
Average Power (micro wtts)	407.1802	376.5287	1568.081
Output noise (nano volts	45.96973	32.85069	87.55068

We collected the data of average power and output noise of positive edge triggered D-flip flop using all three techniques and plotted a graph as shown in Figure 8. It is seen from Figure 8 also that MTCMOS is the best method for low power applications as it consumes less power.

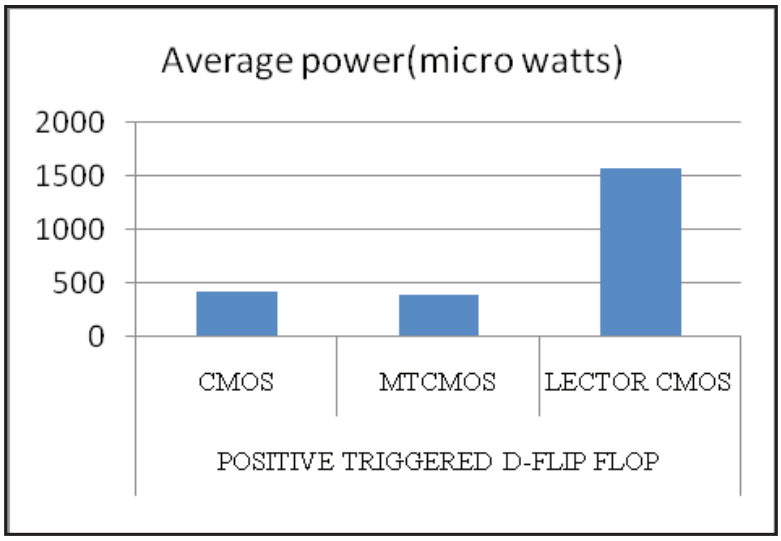

Figure 8: Average power comparison graph

Figure 9 represent the output noise in nano volts. Here also it is clearly depicts about low noise in MTCMOS showing that MTCMOS is the best method for low noise application also. This is because consideration of multi threshold voltages reduces the leakage current drastically. However, in Lector case, though we could able to reduce the leakage current, addition of few external circuit makes it complicated and increases the static power consumption. The use of more circuits also naturally increases the noise generation. Therefore, it is suggested that MTCMOS circuit is best suitable to obtain low power and low noise.

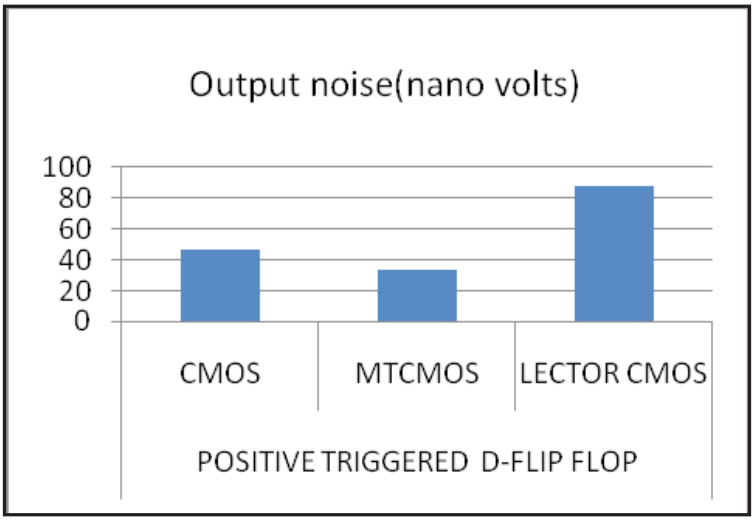

Figure 9: Output noise comparison graph.

7. CONCLUSION

In this work, a comparative study of different low power designs techniques is implemented using CMOS, MTCMOS and LECTOR CMOS techniques on positive edge triggered D-Flip flop as case study. It is noticed that all the three techniques have their own merits and demerits. According to our analysis, MTCMOS is good in terms of average power and output noise. According to our analysis, the D-flip flop designed using MTCMOS technique is good for low power and low noise applications.

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