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Design of Low Power & High Performance Dual- V_{dd} Multi -V_{th} Level Converter

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ABSTRACT

Clock distribution networks consume a major portion of the power of a chip . Continuous Scaling of VLSI Technology i.e Channel length ,Supply has lead to integration of millions of transistors on a single chip operating at very high clock frequencies. Besides area and performance, the modern VLSI designs aim at low-power consumption due to limited battery lifetime. Most voltage scaling techniques require that the Integrated Circuit operates at a single supply voltage The design utilizing Dual Vdd and Single Vth provide effective reduction of power.

The use of multiple supply voltages (multi- Vdd) is an effective technique for reducing the power consumption without degrading the speed in an integrated circuit (IC). To transfer signals among the circuits operating at different supply voltages such as Dual Vdd , level converters are required. Three new multi supply voltages (multi-Vdd) level converters are proposed in this paper. The proposed level converters are compared with the level converter. For high performance and Low power design, different types of level converters are analyzed.

Keywords: CDN, single threshold voltages ,Level Converters, multi-Vdd,etc.,

1. INTRODUCTION

The clock distribution network (CDN) delivers the clock signal to all the sub system of an Integrated Circuit. The clock distribution network consumes a considerable amount of power in synchronous digital systems. The major component of the total power dissipation is the power that is used for charging and discharging the load capacitance in the circuits.

$$P = f_r C_{Load} V_{dd} V_{os}$$

where fr is the clock frequency, C_{Load} is the total load capacitance, V_{dd} is the supply voltage, and Vos, the output swing of the buffer. For the case where the output of the buffer swings from 0 to Vdd, Vos = Vdd and the formula reduces to

$$P = f_r C_{Load} V_{dd}^2.$$

Where f_r is a fundamental parameter for the circuit.

2. LOW POWER CLOCK SCHEME

In this Low power clock tree, a HL Converter is a buffer that converts the incoming clock signal to the chip from a high voltage swing to a low voltage swing. Alternatively, the input clock could be generated so that it has a low voltage swing. The clock signal is then transmitted on the chip as a low voltage signal, thereby ensuring a low power clock distribution network. At the points of utilization at the sink flip-flops, it is converted using the LH Converter (Low-to-High converter) block to the higher voltage swing, which is the voltage at which it is used by the logic network. Intermediate buffers are used in the clock tree to regenerate

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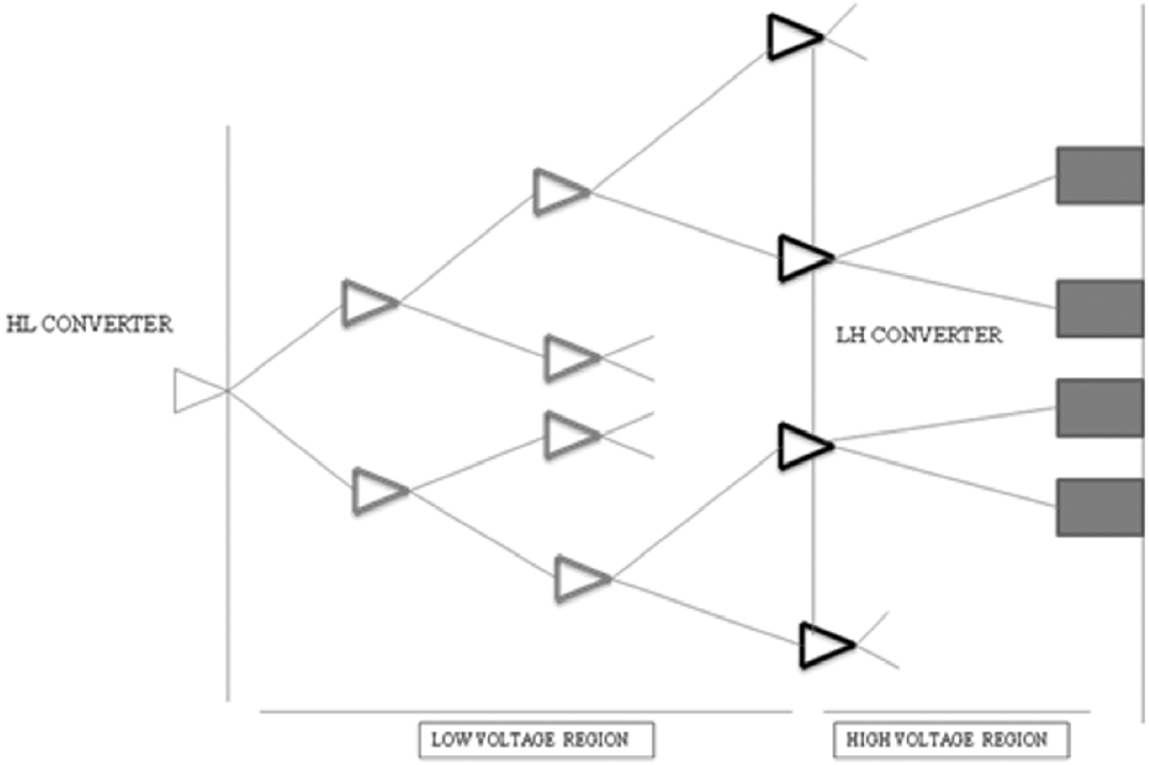

Figure 1: Low Power Clock Scheme

the signal and maintain a sharp slew rate as the signal passes through the network. An HL Converter is inserted at the root of the clock tree, and LH Converters are inserted at the clock sinks, thereby placing the entire clock tree in the low voltage region.

3. LEVEL CONVERTER CIRCUITS

The structure of the LH Converter is relatively straightforward. To convert the clock swing from a Lower voltage range of gnd to VddL to a Higher voltage range of gnd to VddH, a conventional buffer driven by a supply voltage of VddL will be adequate. We note that the use of feedback in the part driven by VddH serves to speed up the transition and therefore ensures that the transient current is not significant. The Level converters are discussed as below:

3.1. Standard Level Converter

The Existing Standard Level Converter is the feedback based ,in which outputs are cross coupled. When a Low Voltage swing signal directly drives a gate that is connected to a higher supply voltage, the pull-up network of the cannot be fully turned off, therefore it produces static dc current. In order to suppress this static dc current, specialized voltage interface circuits are employed between a low voltage driver and a full voltage swing receiver [2].

In the standard Level Converters which are feedback-based, the pull-up network transistors are not directly driven by the low voltage swing signal provided by the driver. The pull-up network operation is controlled by an internal feedback technique [4]. Isolated from the low voltage swing input signal, thereby avoiding the formation of static dc current paths within the Circuit.

The traditional level converters suffer from high short-circuit power and long propagation delay due to the slow response of the internal feedback circuitry mechanism which controls the operation of the pull-up transistors. The pull-up network transistors that receive higher gate overdrive voltages from the full-voltage

swing feedback paths. But at low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to Balance the strength of the pull-up and the pull-down networks. This causes further degradation in the speed and the power efficiency of the conventional level converters when utilized with very low input voltages [3].

The input Voltage applied is a Low voltage range (gnd to VddL). The supply Voltage used for VddH and VddL. It can be any voltage ranging from (1.2V to 3.3V to 5V). If a Logic '0' is applied at input i.e at n1(node 1) it becomes Logic '1'(VddL). This Voltage turns on nmos(M1), this makes pmos(M4) on thus a Voltage (VddH) drives output inverter, output attains Logic '0'. The VddH at the input of output inverter makes pmos (M3) off. This output is connected to cross coupled pmos devices as such Logic '1' is applied to M3 ,which turns off and M4 gets turned on. Thus output remains stable at Logic '0'.

Now if a Logic '1' (VddL) at input turns on M2 and the inverter output which is Logic '0' at node (n1) turns off M1. The M1 drain voltage is at Logic '1' which turns off M4 thus output is driven to VddH. The output Voltage then turns on M3 and thus maintains the output voltage at Logic '1'(VddH).

Similarly a standard Level Converter (HL) can be analysed by changing the Voltages as VddL to VddH and viceversa. It converts the clock swing from a Higher voltage range of gnd to VddH to a Lower voltage range of gnd to VddL,The lower values of VDDL, the sizes of M1 and M2 need to be increased in order compensate for the gate overdrive degradation. The load seen by the previous stage (driver circuit) is therefore increased, thereby further degrading the speed and increasing the power consumption. Tapered buffers are required to drive M1 and M2 at very low voltages. These tapered buffers further increase the power consumption of LC1.

3.2. Pass Transistor Based Level Converter

Another Existing level converter (LC2) is used for enhanced speed as compared to LC1. LC2 is shown in Fig. 3.M6 maintains the voltage of gate of M1 between VddL and VddL + Vthn to enhance the current produced by M1. The capacitor (C= 7 Ff) is used to stabilize the voltage of gate of M1 against the noise induced by the nearby switching events.

In the Fig.3, the second Level (LH) converter is shown. If input is at Logic '0' ,as nmos(M1) turns on due to the voltage from nmos(M6) which varies between VddL and VddL + Vthn . Thus a Logic '0' is applied to M3 and M2,thus pmos(M3)gets turn on and nmos(M2) turns off. This Voltage of VddH at the output of inverter drives the output inverter as such a Logic '0' appears at the Level Converter output.

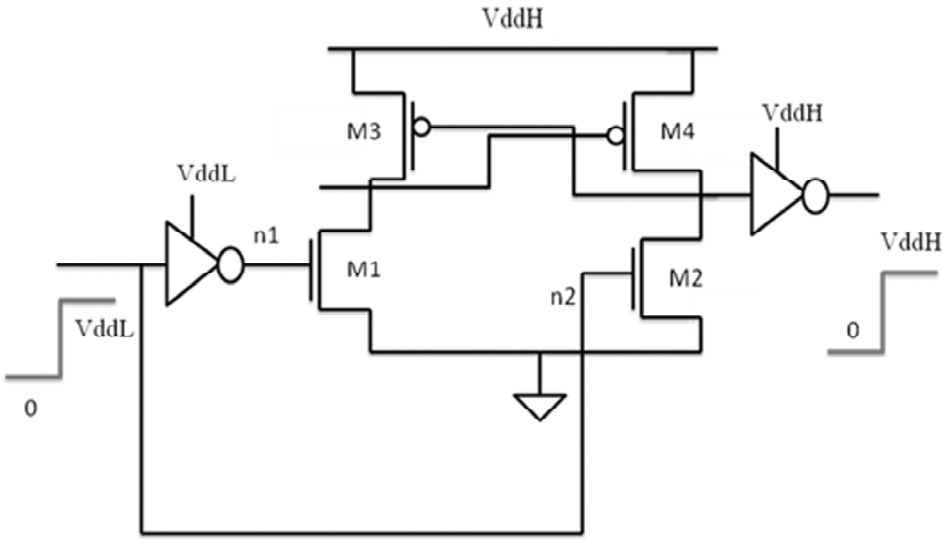

Figure 2: Standard Level Converter(LC1)

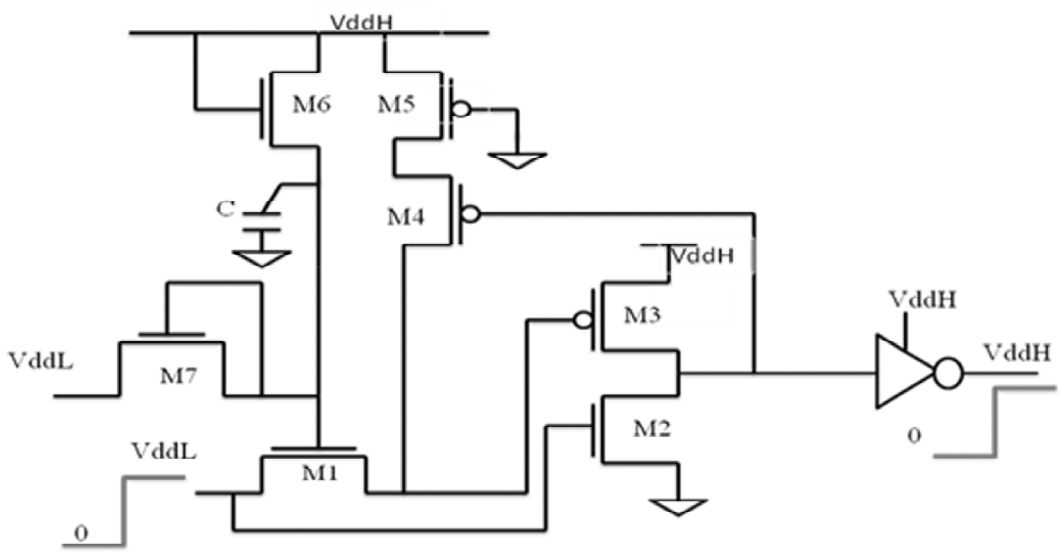

Figure 3: Pass Transistor based Level Converter(LC2)

If input to the Level Converter is at Logic '1'(VddL),as nmos(M1) turns on due to the voltage from nmos(M6) which varies between VddL and VddL + Vthn. Now this Logic '1'(VddL) is applied to M2 and M3. This voltage makes nmos(M2) on and pmos(M3) off. the output of first inverter is driven to Logic '0' which driven the second inverter driven by supply voltage of VddH. Thus the output of the second inverter attains the value of Logic'1'(VddH).

When the input changes from gnd to VDDL there is a direct current path from VddH to gnd through the M2 & M3 path. This direct current path exists until output of nmos(M1) is charged to VddH through M4 and M5. Similarly, when the input changes from VddL to gnd, there is a direct current path from VddL to gnd through the M5–M4 –M1 path. This direct current path exists until input of second inverter is driven up to VddH and M4 is turned off. Level Converter consumes significant short-circuit power, similar to Standard Level Converter_1, during both transitions of the output. Furthermore, when VddL is reduced, a significant increase in the size of M2 is required for maintaining functionality. The load seen by the driver circuit therefore increases at Lower VddL. Tapered buffers are required for driving LC2 at very low voltages. These tapered input drivers further increase the power consumption of LC2.Similarly a Level Converter (HL) can be analysed by changing the Voltages as VddL to VddH and viceversa. It converts the clock swing from a Higher voltage range of gnd to VddH to a Lower voltage range of gnd to VddL.

3.3. Multi-vth Level Converters

Multi - Vth level converters are described in this section. These level converters employ a multi-Vth CMOS technology in order to eliminate the static dc current. The high threshold voltage pull-up network transistors in the new level converters are directly driven by the low-swing signals without producing a static dc current problem.

The Multi-Vth level converter (LC3) is shown in Fig.4 LC3 is composed of two cascaded inverters with dual -Vth transistors. The threshold voltage of pmos(M2) is higher Vth for avoiding static dc current in the first inverter when the input is at VddL .The threshold voltage of pmos(M2) is required to be higher than VddH-VddL for eliminating the static dc current. When the input is at Logic '0', pmos(M2) is turned on. nmos(M1) is off. The Output of the first Inverter is driven to VddH. The output of the second inverter is discharged to Logic '0'. When the input is at VddL, nmos(M1) is turned on. pmos(M2) is turned off since Vgs, M2>Vth, The output of the first inverter is to Logic '0'. The output is of the second inverter is charged to VddH [11].

LC3 consumes lower power, occupies significantly smaller area, and imposes a much smaller load capacitance on the input driver as compared to LC1 and LC2. The circuit configurations of the level Converter LC4 is shown in fig.5In the Level Converter LC4 ,M1 needs to be cutoff after a "1" is successfully propagated to the output (the input is at VddL and the output is at VddH) in order to avoid the formation of a static dc current path. The Logic circuitry composed of M5, M6 , and C, shown in Fig. 5

When input is at Logic '0', pmos(M4) turns on and nmos(M3) turns off , thus pmos(M2) is turned off which drives the output to Logic'0'. If Logic'1 i.e VddL is applied as input, pmos(M4) turns off and nmos(M3) turns on ,thus pmos(M2) is turned on which drives the output to Logic'1'i.e VddH. The circuit configurations of the another level Converter LC5 is shown in fig.6

The problem of static current arises for extremely low VddL. In general LC5 can be used for which When input is at Logic '0', pmos(M4) turns on and nmos(M3) turns off , thus pmos(M2) is turned off which drives the output to Logic'0'. If Logic'1 i.e VddL is applied as input, pmos(M4) turns off and nmos(M3) turns on , thus pmos(M2) is turned on which drives the output to Logic'1'i.e VddH.

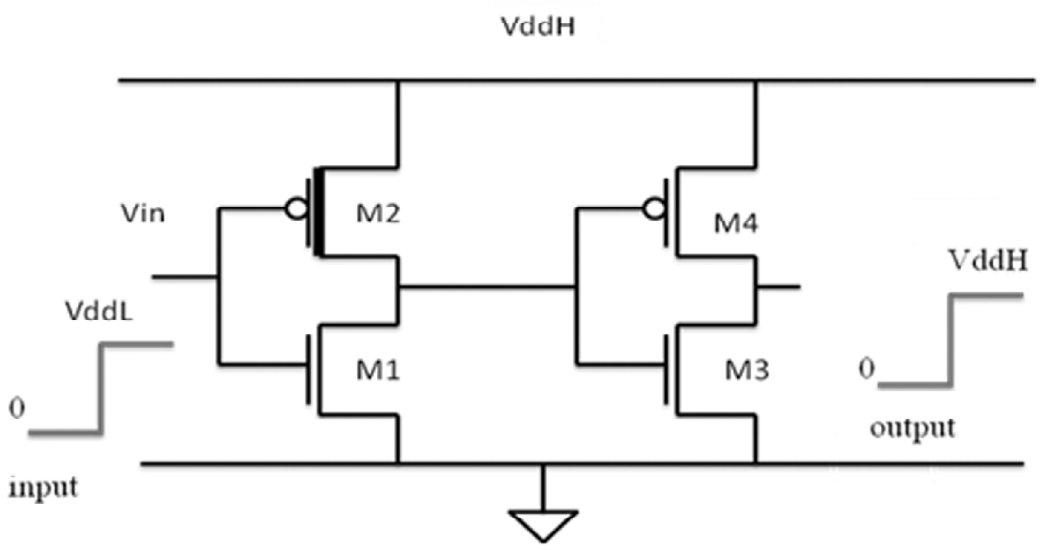

Figure 4: Multi Vth Level Converter(LC3)

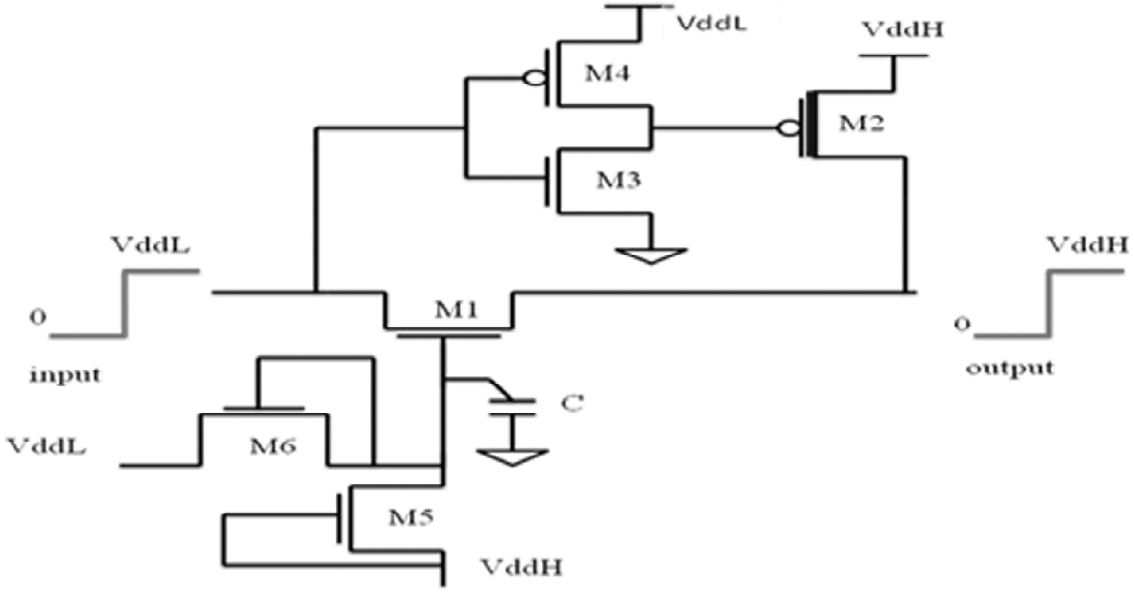

Figure 5: Multi Vth Level Converter(LC4)

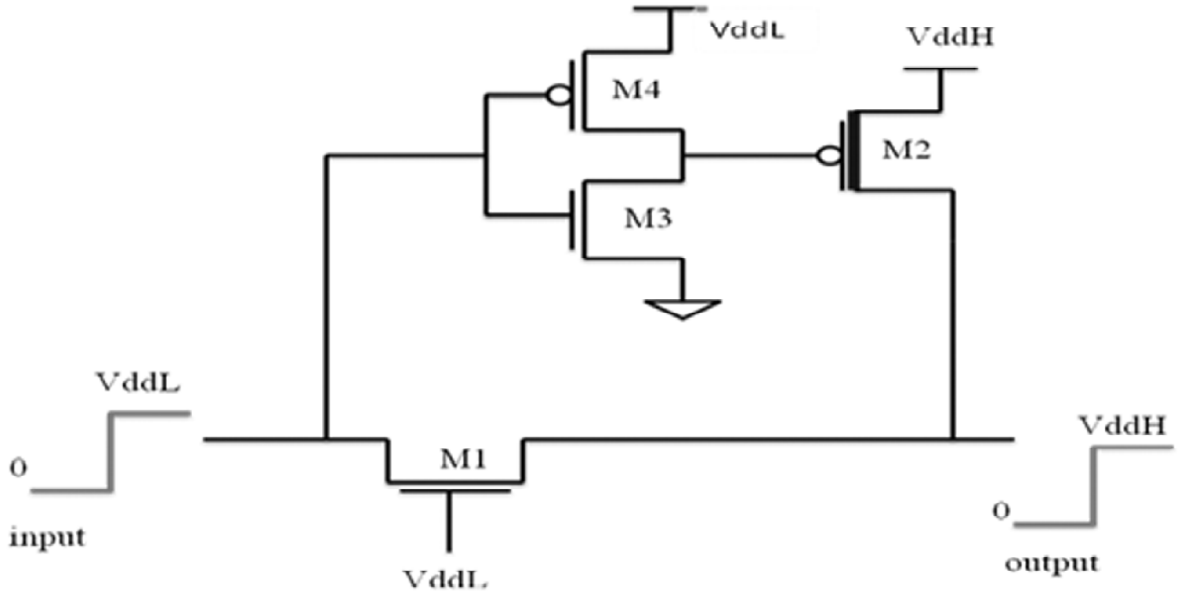

Figure 6: Multi Vth Level Converter(LC5)

3.4. Proposed Level Converter Using Transmission Gate

The operation of Transmission gate based Level Converter is same as pass transistor based LC. The need for using very Low voltages for which a pass transistor is used, it is replaced by a transmission gate**.** The power consumption is also reduced by 11.6%

3.5. Proposed Level Converter Using Dual Vdd & Multi Vth Voltage

The proposed design is the conventional Circuit where two inverters are cascaded which acts as LH Converter. For the input Logic '0' the PMOS(p2) is on and NMOS(n2) is off thus the output of first inverter is Logic '1' which makes nmos(n3) on and PMOS(p3) off . Thus output remains at Logic '0' . When the input is at Logic '1' (VddL),nmos (n2) is on, PMOS(p2) is off thus output of first inverter is at Logic '0' which makes

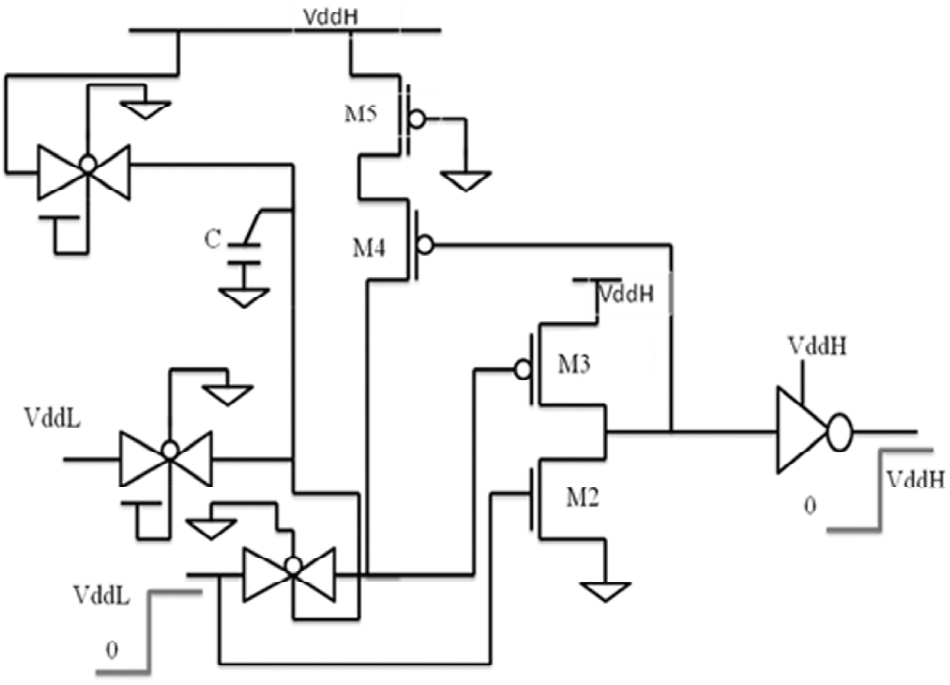

Figure 7: Proposed Transmission gate based Level Converter(LC6)

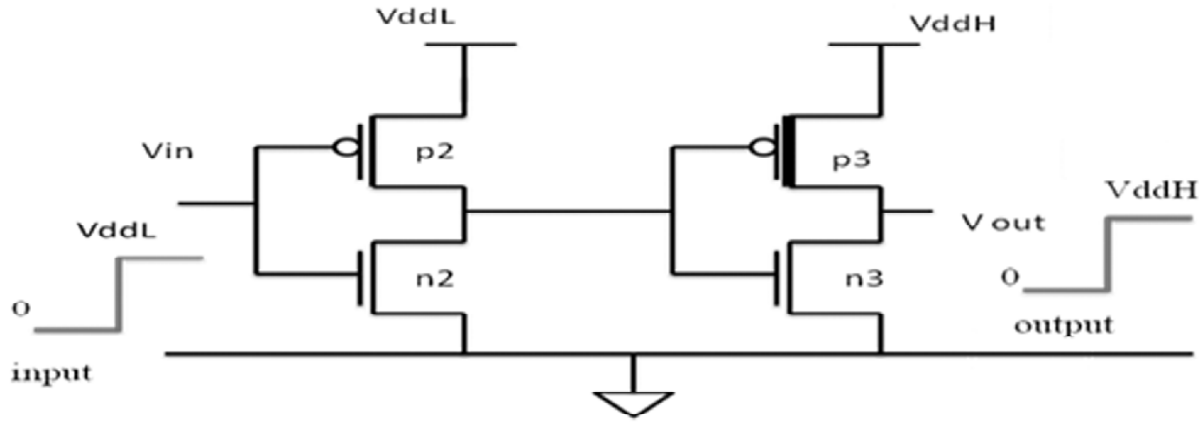

Figure 8: Proposed Dual Vdd & Multi Vth Level Converter(LC7)

PMOS(p3) on and NMOS(n3) off. Thus output goes to Logic 1(VddH).Thus output of the proposed Level converter is an LH i.e. VddL. to VddH.

3.6. Proposed Level Converter Using Dual Vdd & Single Vth Voltage

The proposed design is the conventional Circuit where two inverters are cascaded which acts as LH Converter. For the input Logic '0' the PMOS(p2) is on and NMOS(n2) is off thus the output of first inverter is Logic '1' which makes nmos(n3) on and PMOS(p3) off . Thus output remains at Logic '0' . When the input is at Logic '1' (VddL),nmos (n2) is on, PMOS(p2) is off thus output of first inverter is at Logic '0' which makes PMOS(p3) on and NMOS(n3) off. Thus output goes to Logic 1(VddH).Thus output of the proposed Level converter is an LH i.e. VddL. to VddH.

3.7. Proposed Level Converter Using Dual Vdd & Multi Vth Voltage Using Transmission Gate.

When input is at Logic '0', pmos(M4) turns on and nmos(M3) turns off , thus pmos(M2) is turned off which drives the output to Logic'0'. If Logic'1 i.e VddL is applied as input, pmos(M4) turns off and nmos(M3) turns on , thus pmos(M2) is turned on which drives the output to Logic'1'i.e VddH. The proposed LC8 can be used for very Low supply Voltages and threshold loss due to mosfet is replaced by a transmission gate. Similarly a Level Converter (HL) can be analysed by changing the Voltages as VddL to VddH and viceversa. It converts the clock swing from a Higher voltage range of gnd to VddH to a Lower voltage range of gnd to VddL range of gnd to VddH to a Lower voltage range of gnd to VddL

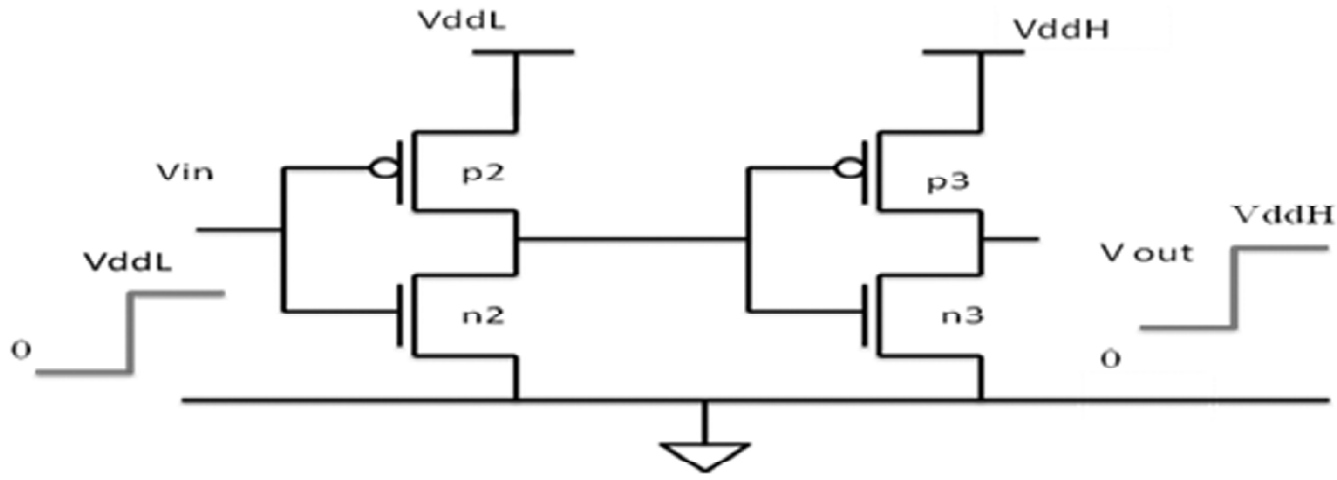

Figure 9: Proposed Dual Vdd & Multi Vth Level Converter(LC8)

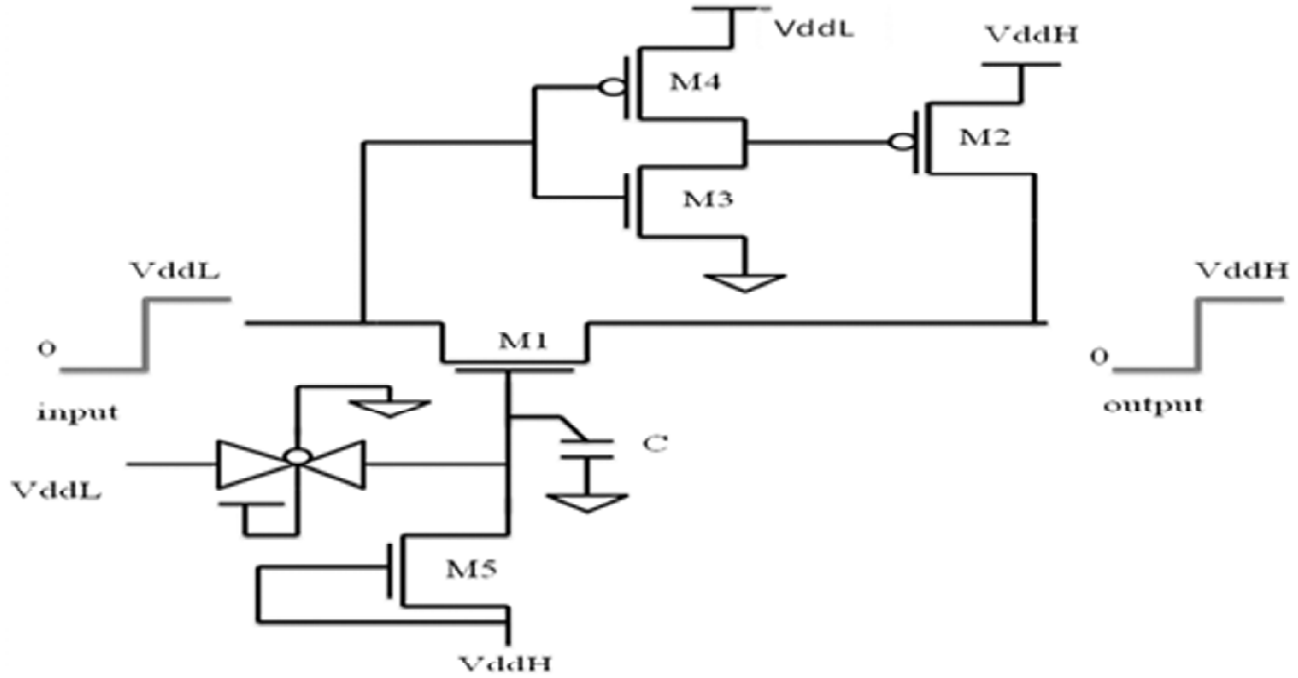

Figure 10: Proposed Dual Vdd & Multi Vth Level Converter(LC8)

4. CONCLUSION

In this paper, Various Low Power Scheme Level Converters are proposed from the existing Multi Vth Level Converter. Each Level Converter proposed has advantageous of power consumption or Supply voltage used, number of transistors utilized. Also one drawback of short circuit path is eliminated in proposed Level converters.

The Power Dissipation of Level Controllers can be minimized by redesigning the circuit to act as Low to High Level Converter(VddL=3V to VddH=5V) or High to Low Converter(VddH=5v to VddL=3V). The simulations are done using supply voltages of VddL: 1 and 1.2 V. The standard maximum supply voltage (VddH) is 5V.

Figure 11: Simulation Results of LH Converter

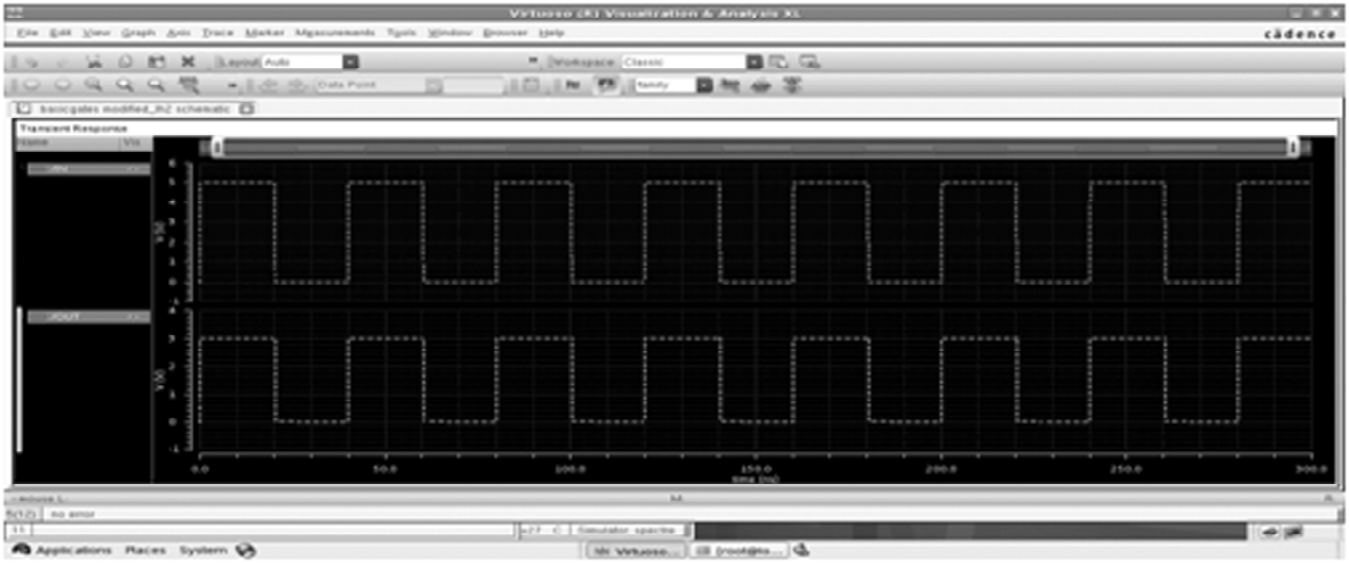

Figure 12: Simulation Results of HL Converter

Therefore, the power dissipation of the Level Converters can only be reduced by reducing the total load capacitance, reducing Vdd, reducing Vs without reducing Vdd, which corresponds to a linear reduction in the power dissipation. The **VddL** used is 3V and **VddH** used is 5V and Load capacitance is varied from 10 f F to 1pF.The Frequency of oscillations produced is 10 Mhz. The Comparison of Power Consumption of Various Level Converters proposed is

Table 1
Comparison of Power consumption of Various Level Converters.

S.No.	Level Converter	Transistor Sizes	N	Power Consumption
1	LC1	W_n=1.0u,L_n=0.12u,W_p=2.0u,L_p=0.12u	08	0.559mW
2	LC2	W_n=1.0u,L_n=0.12u,W_p=2.0u,L_p=0.12u	09	0.258mW
3	LC3	W_n=1.0u,L_n=0.12u,W_{p2}=2.0u,L_{p2}=0.12uW_{p3}=8.0u, L_{p2}=0.06u	04	15.070uW
4	LC4	W_n=1.0u,L_n=0.12u,W_{p4}=2.0u,L_{p4}=0.12uW_{p2}=8.0u, L_{p2}=0.06u	06	23.546uW
5	LC5	W_n=1.0u,L_n=0.12u,W_{p4}=2.0u,L_{p4}=0.12uW_{p2}=8.0u, L_{p2}=0.06u	04	29.071uW
6	Proposed LC6	W_n=1.0u,L_n=0.12u,W_{p2}=2.0u,L_{p2}=0.12u	10	0.228mW
7	Proposed LC7	W_n=1.0u,L_n=0.12u,W_p=2.0u,L_p=0.12u	04	9.983uW
8.	Proposed LC8	W_n=1.0u,L_n=0.12u,W_{p4}=2.0u,L_{p4}=0.12uW_{p2}=8.0u, L_{p2}=0.06u	07	24.150uW

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