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Oscillation Ring Test Using Modified State Register Cell For Synchronous Sequential Circuit

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ABSTRACT

Nowadays increase in speed and decrease in chip size leads to increase in delay faults in the circuit. The detection of these delay defects requires at speed testing methodology. At-speed method testing creates signal transitions which will be captured in normal speed. In this paper, an oscillation ring test for synchronous sequential circuit is implemented and a modified state register cell, which is used to modify the states of finite state machine, is developed. The test response obtained from the circuit is directly observed at primary output, which results in reducing the communication between automatic test equipment and the circuit under test. The expected output of this work is high fault coverage with less number of test vectors.

Keywords: Oscillation Ring test, MSR cell, synchronous sequential circuit, At-speed test.

1. INTRODUCTION

An oscillation ring test is a closed loop test with odd number of signal inversions in it. Once the ring is constructed, oscillation signal appears on the ring. The ring can be constructed by connecting output to the input. For a circuit with stuck at and stuck open fault, oscillation will not occur or stops and while the oscillation frequency will be different for circuit with gate delay or path delay fault from fault free circuit. The circuit under test can be tested, by observing the oscillation signal output of the circuit, one can decide whether the circuit under test is faulty or not. Oscillation test is a useful and efficient method to detect faults in functional circuits and devices. The test was used to evaluate the speed of integrated circuits, to generate control voltage, to extract circuit trans-conductance, and phase noise.

We propose an oscillation ring test method for sequential circuit testing. The proposed method involves modification of storage elements so that oscillation signal can be generated on the circuit based on the functional and timing specifications of the circuit under test. Fig.1 shows the oscillation ring test methodology.

Delay Faults are mainly caused by the gate delay, transition delay of any input or output signals. Interconnection delay also plays a vital role in total delay faults. The main difference between gate delay and interconnection delay or path delay is individual component delay. The gate delay involves the assumption of individual component delay while in path delay there is no need to assume the individual component delay. The critical path determines the working speed of the circuit. Critical path is nothing but the any longest path between primary input and the primary output. If circuit or devices is fault free, then the circuit will perform at the same speed as like critical path. If any delay in the circuit then the device or circuit might have delay fault as well as some other faults.

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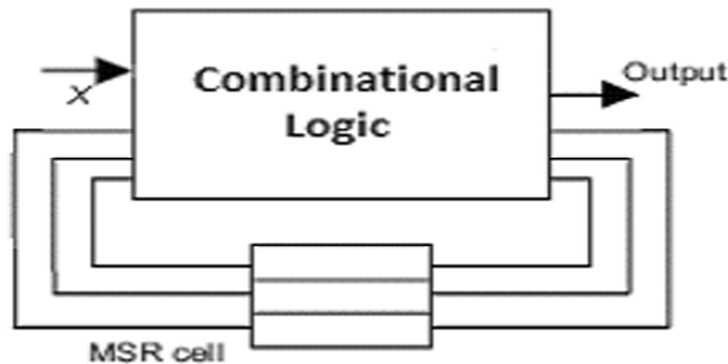

Figure 1: Oscillation Ring Test

2. OSCILLATION RING TEST FOR SYNCHRONOUS SEQUENTIAL CIRUITS

Oscillation ring test for sequential circuits has been proposed. The proposed method was very useful in detecting faults in the circuit. As from the name oscillation ring test, we have to form a ring in the circuit and make circuit to produce oscillation. The produced oscillation signal was observed at output, with the obtained oscillation signal one can able to decide whether the circuit is faulty or fault free.

The ring in the circuit was formed by providing the feedback path between the output and the input. Now the circuit looks like a closed ring. Whenever the odd inversions present in the circuit, the oscillation can be formed in the circuit. It is very difficult to produce oscillation in the asynchronous circuit. The clock signal was used in order to make production oscillation easily. The circuit was controlled by the clock signal, the applied clock signal makes the circuit as synchronous circuit. This method involves addition of some components but it has advantage of no usage of tester and also the test cannot produce any delay. The Modified scan register was used, which helps to modify the state holding elements or storage elements. The MSR cell decides the next state of finite state machine.

2.1. Forming Oscillation in the circuit

Fig.2 shows the transition table and output of the FSM. Fig. 3 shows the state diagram of the FSM as an example to explain the oscillation ring test. The oscillation was formed by when the primary input is fixed at either 1 or 0 and the FSM is in any one of the state then the FSM moves to the another state. The output corresponding to those both states should be different. For example if first state has output as 1 then next state should have output as 0 or vice versa. From the second state FSM should have move back to first state

Present State (PS)	Next State (NS)		Output (Z)	
	X=0	X=1	X=0	X=1
A 000	C 010	F 111	1	0
B 001	D 011	E 100	1	0
C 010	F 111	D 011	1	1
D 011	C 010	A 000	0	1
E 100	E 100	B 001	0	0
F 111	A 000	B 001	1	1

Figure 2: State Transition Table of FSM

only not to any other state. Again FSM goes to same state. Thus for fixed input if FSM moves forth and back between any two states whose output are different then oscillation signal was obtained at the output.

In the above mentioned example only two states B and E for fixed input 1 will produce oscillation for remaining other states there is no possibility of producing oscillation.

2.2. Modified Scan Register Cell

In order to produce oscillation in remaining states we use modified scan register cell, which changes the next state so that oscillation can be formed in all the states. The MSR cell modifies the state transition table

Figure 3: State diagram of the FSM

PRESENT STATE	NEXT STATE	OUTPUT STATE	OUTPUT
0	0	LOW	0
0	1	RISING	1
1	0	FALLING	0
1	1	HIGH	1

Figure 4: State transition bit truth table

OP Value		2nd Operand			
		L	H	R	F
1st Operand	L	Bypass	INV	Hold 0	Fail
	H	INV	Bypass	Fail	Hold 1
	R	Hold 0	Fail	INV	Bypass
	F	Fail	Hold 1	Bypass	INV

Figure 5: MSR Operational Table

of the FSM in order to produce oscillation. MSR cell uses state bit transition truth table and MSR cell operational table. Fig.4 shows the state transition bit truth table. Fig.5 shows the MSR operational table.

The state transition bit truth table explains the change in bits between any two states for the same position. The LOW state indicates that both present state and next state was 0. The RISING state indicates that present state it is 0 while next state bit is 1, for the FALLING state is just opposite of rising state that present state is at 1 and the next state is at 0. Similarly for HIGH state both present and next state bit is at 1.

The relationship between normal mode next state and test mode next state was explained with the help of MSR operational table. It performs five operations. The operand 1 in the table indicates the normal mode next state while the operand 2 indicates the test mode next state. If both the operands are in low state or in high state then MSR is in BYPASS state. Similarly if any one operand is in rising and another is in falling state or vice versa then also he MSR will be in BYPASS State. In BYPASS state the output is same as the input. If MSR state is INV then output is inversion of input. In HOLD0 state the output of MSR will be 0 irrespective of any input. Similarly for HOLD1 state the output will be in 1irrespective of its input. In some cases, there is conflict between two operand arrives while at the time FAIL operation was executed.

2.3. Modifying the circuirt to create oscillation

As said early the oscillation was produced only for B and E states. So only these two states can be tested. In order to test the other states, we have to make some changes in the FSM with the help of MSR cell so that oscillation will be produced in all other states, which means all other states also can be tested. The MSR cell will force the next state whose output was differ from present state. Fig.6 shows the state transition and output table of modified FSM. Fig.7 shows the state diagram of the modified FSM.

In the modified FSM all the six states can be tested. Oscillation was formed in all six states with three pairs. For Example for the fixed input x=0, when FSM is in state A whose output was 0, then FSM moves to the next state D whose output will be 1. Again move back to A and continues. Thus outputs of two states differ with fixed input and also FSM moves forth and back between these two states. So these states can able to produce oscillation and also A and D states can be tested. Similarly for fixed input X=1, if FSM is in either B or F state whose output was 0 and 1 respectively. The FSM moves back and forth between these two states. Hence oscillation can be produced in these states. These two states are also tested. Similarly all the other states are changed in order to produce oscillation so that every state in the FSM was tested.

Present State (PS)	Next State (NS)		Output (Z)	
	X=0	X=1	X=0	X=1
A 000	D 011	F 111	1	0
B 001	D 011	F 111	1	0
C 010	F 111	E 100	1	1
D 011	A 000	C 010	0	1
E 100	E 100	B 001	0	0
F 111	A 000	B 001	1	1

Figure 6: State transition table of Modified FSM

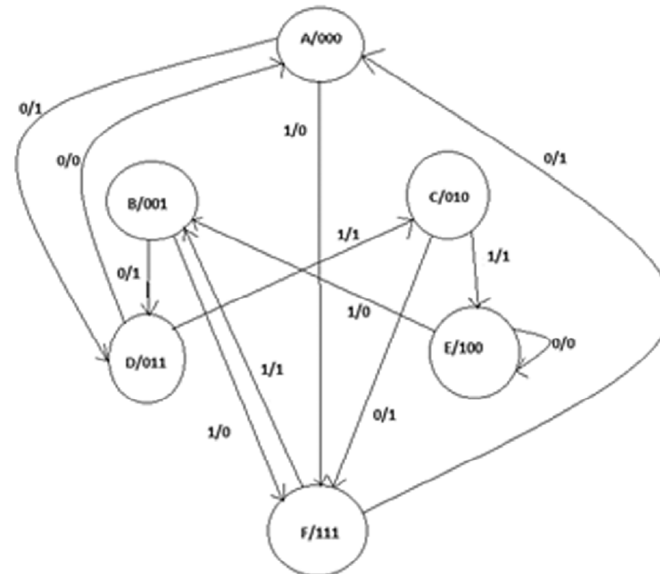

Figure 7: State diagram of Modified FSM

3. RESULTS

The proposed oscillation ring test was demonstrated on some MCNC circuits. The maximum number of state transition function was given by (2^p)*s. P is number of primary inputs while S is number of states.

Table 1 Result of Oscillation Ring Test on MCNC Circuits

Circuit	Proposed					#stv (ATPG)
	Transition		Stuck-At			
	#t(osc)	FC(%)	#t(osc)	FC(%)	#t(scan)	
bbsse	130	88.75	52	98.28	2	52
cse	231	90.78	80	99.43	2	76
dk14	107	93.45	22	97.35	4	36
dk15	98	92.06	19	100.00	0	24
dk16	237	96.20	62	99.23	3	65
dk17	67	97.00	17	100.00	0	21
dk27	19	84.04	7	100.00	0	11
dk512	56	95.46	19	100.00	0	24
lion	20	96.00	7	100.00	3	8
mc	21	97.67	7	100.00	0	10
planet	391	95.31	121	97.51	19	128
s1	338	86.16	93	93.69	26	105
sand	589	98.74	155	99.60	2	140
sse	130	88.75	52	98.28	2	52
styr	576	96.78	157	98.78	6	157
tbk	661	83.24	214	100.00	0	189
s27	28	98.28	6	97.50	1	11
s298	143	97.67	48	99.07	2	30
s386	138	87.70	44	95.56	6	42
s1488	476	96.93	131	98.25	10	135
s1494	511	96.34	143	98.18	10	154
Average		**93.21**		**98.61**		

This method was very effective for circuit which produces more number of oscillations in the circuit. Hence circuit with more output was very suite for this test.

Table.1 shows the results of proposed oscillation ring test on benchmark circuits. The proposed test method almost detects all faults in the circuit. In average around 93% of transition delay fault was detected while around 98% of stuck-at faults were detected. The Proposed test method does not require any complex clock signal which is usually required for transition delay fault. The proposed test method has complexity of O (n^2), where n denotes number of state transition function. With higher value of n, the proposed methodology achieves high accuracy.

4. CONCLUSION

In this work, the oscillation ring test for synchronous sequential circuit was proposed, in which at-speed testing is possible. Most of the delay faults in the circuit were detectable while performing the proposed test method. MSR cells are developed in order to make oscillation in the circuit, so that circuit can be tested. However the proposed method has few disadvantages like gate level fault coverage was not guaranteed. It also does not guarantee about detection of physical faults. Experimental result shows that delay fault coverage by this proposed method was very good.

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