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# Design of Nine Level Inverter with Added DC Source using Level Module Technique

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**ABSTRACT**

A two stage conversion is required to convert high voltage dc to high voltage ac. This process requires very bulky equipment and more complex to control, and becomes less efficient. In Power Distribution System (PDS), DC is replaced by High Frequency AC (HFAC) for better cost and equipment. High Frequency inverter acts as source side inverterin High Frequency AC system. This paper proposes a new level module topology, and it simplifies multilevel inverter circuit. It replaces H-bridge configuration with level module topology. This topology has reduced switches, and also improves efficiency. The topology has an added dc source which allows for an asymmetrical configuration, making it suitable for implementing renewable energy resources. The proposed topology is simulated using MATLAB/ SIMULINK environment. The results are presented to validate the proposed idea.

***Keywords:*** Cascaded H-Bridge, Power Distribution System (PDS), High Frequency AC (HFAC). Multi-levelinverter (MLI). Fuel Cells (FC). Diode Clamped Multi level Inverter (DCMLI). Capacitor Clamped Multi level inverter (CCMLI)

## I. INTRODUCTION

Multilevel inverters play an important role in interfacing the local system with the grid.The use of cascade multi-level inverters will help in connecting renewable energy resources with the grid. Asymmetrical MLI has multiple inputs, single output configuration. This helps interface renewable energy with grid.

Most prominent renewable resources such as solar, fuel cells, wind and batteries are available in different voltage levels. Also it is quite important to be grid interactive and for further developments into smart grid.

The conversion process from high voltage dc to ac amplification requires two or more stages, but multi–level inverters make it easy by converting high amplitude dc to ac. But amplification requires more levels. Multi-level inverters make it easy by converting high voltage dc to ac without stepping up and down of voltage levels.

Multi-level Inverter eliminates the use of transformer, and henceforth reducing the losses caused by it. The selection of inverter in dc to ac power conversion is very crucial. Multilevel inverters are used to achieve proper ac output and eliminating harmonics. In high frequency ac power distribution, dc power is being replaced by ac for reduction in cost and bulk equipment [1]. High frequency switching methods are implemented in power distribution systems. Research in hybrid multi-stage inverters with unequal input voltages is being carried out. The switched capacitor network model has been implemented in recent literature [1]. The switched capacitor network uses series and parallel combinations with inverter to achieve a nine level output [2]. Switched capacitor based boost converter is implemented. The multi-level inverter aims to increase voltage of output with switched capacitor and H-bridge inverter at the end [3]. A number of single stage switched capacitor and inductor networks are used in power conversion. The inductors limit peak current in the circuit [4].

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A multi-level inverter with reduced switches is considered. The design is improved byreducing switches. The switching losses are decreased by decreasing number of switches [5]. Various inverter topologies such as Diode Clamped Multi Level Inerter and Capacitor Clamped Multi Level Inerter are studied in [6]-[7]. High frequency power distribution systems require switching at high speeds. The switching speed should support high power for application like hybrid vehicles. The hybrid vehicle with fast switching technique is implemented [8]. Resonant inverters are able to achieve nine level output with phase shifted modulation [9]-[10]. Two stage conversions from dc to ac are done with resonant inverter [11]. Multiple PWM technique is used to reduce harmonic content. The control of the system is also improved by using multiple pwm technique.Some multilevel inverter concepts are discussed in [12]–[16].

Voltage step up converter employs switched capacitor with h-bridge inverter, to obtain ac voltages with varying ratios[17].Neutral point clamped inverter configuration is used for voltage balancing. Different types of neutral point clamped topologies are studied in [18]–[21]. Active filtering techniques are implemented in multi-level inverter for eliminating harmonics [22].High frequency ac power is fed to motor loads in vehicles [23].

Bidirectional power conversion helps save energy and feed energy back to battery [24]. Five level inverter pwm structuresarestudied with various pwm techniques [25]. Switchedcapacitor fed multi-level inverter is advantageous in contrast with other multi-level inverter due to multiple input configurations [26]. Series and parallel combination operations reduce switches and eliminate theuse of inductor [27]-[28]. Boost converter fed multi-levelinverter has added advantage, such as high amplitude output and also eliminates the use of transformer [29]. Asymmetric configuration is currently researched, since interfacing renewable energy is easily achieved.Thisis available in the recent literature [30]-[33]. A wide range ofmulti-level inverters and their modulation are discussed in [34]-[39]. Harmonic elimination is done byusing various algorithms.The use of filter is also considered in this method, as a way to eliminate harmonics [40]-[41].

## II. PROPOSED TOPOLOGY

Components of multi-level inverters include semiconductor switches, voltage supplies and pwm control. Output voltage and current of MLI are stepped waveforms. Multi-level inverter can be implemented from basic three-level and is continued up to ‘n’ level multi-level inverter. Mostly used multi-level inverters in recent years are the Neutral Point Clamped multi-level inverter(NPC), Flying Capacitor multi-level inverter (FC) and Cascaded H-Bridge multi-level inverter (CHB). The neutral point in NPC balances the voltage in the dc link and provides balanced voltage to the inverter.

The flying capacitor technique uses capacitor and diodes to balance and split the voltage equally across the circuit to provide balanced voltage to inverter and reduce damage on switches. The usage of many inputs makes cascaded H-bridge more preferable than other inverters. The H-bridge has multiple inputs and still produces the same output as other topologies.

It combines inputs with varying voltage levels together. Single stepped wave output is achieved. The need to incorporate multiple inputs into a single output is increasing. So hybrid asymmetric multi-stage topologies are becoming more prevalent area in research. In the asymmetric configurations, the voltage inputs vary in number and magnitude of dc voltage supplies are unequal.

Cost reducing topologies are considered in improving inverter without compromising on reliability and efficiency. Reducing switches by changing the design of the inverter seems plausible. Incorporating multiplevoltage inputs is important. Such hybrid multi-stage topology is designed.This topology has multi-level configuration and an added dc voltage supply.

## III. LEVEL MODULE TOPOLOGY

A new level module topology is proposed for reducing the number of semiconductor switches and still obtains the same nine level output. This is done by an added dc source. The topology is designed in such a

way that we can obtain the required voltage by switching on devices. Two switches operate to produce output level using single source at one instant and two sources at other instant. This helps us to replace switched capacitor network which is complex and difficult to control.

## IV. BLOCK DIAGRAM OF LEVEL MODULE TOPOLOGY

The block diagram shows an added dc source with respect to symmetrical configuration. The level module consists of 5 switches. The level module connects the three dc sources with h-bridge.

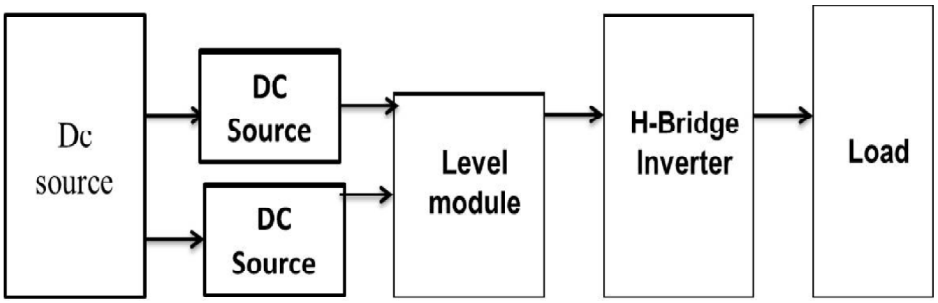


**Figure 1: Block diagram of level module topology**

The added dc source is an advantage in this configuration. The input voltage levels are having the ratioof 1:2:4. The level module utilizes these sources by proper switching pattern. The h-bridge connects level module to the load.

## V. CIRCUIT DIAGRAM

The level module circuit has 5 switches. These switches are operated by pulse generator circuit. The h-bridge has four switches; first diagonal switches operate to give positive half of output while the other pair operates during negative half. The sources are switched on at frequent intervals.

The conventional system has 12 switches and 2 dc sources with complex control circuit.But this design reduces the switches to 9. It also has an added source. The 5 switches reduces switching loss and total power loss. The complex control is also simplified from phase shifted modulation to a pulse generator

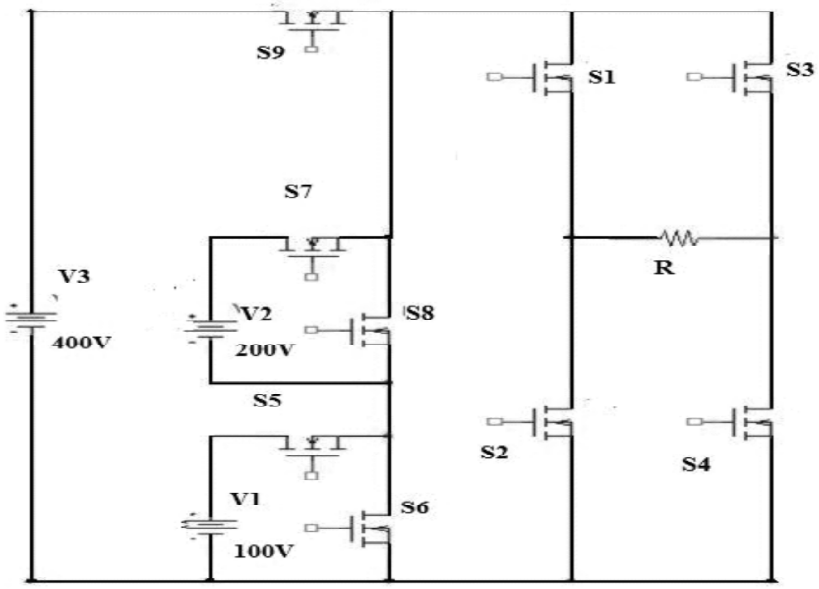


**Figure 2: Circuit diagram of level module topology**

circuit. The asymmetrical configuration will be very useful in interfacing unequal inputs with single load and the system is also effective against voltage unbalancing.

## VI. FOURIER ANALYSIS

The harmonic content in the output voltage can be determinedby using Fourier series.

It is the method of defining a periodic waveform in terms of trigonometric function.

$$V_{O=a_0+\Sigma_{n=1}^{\infty}(a_n\cos(n\omega t)+b_n\sin(n\omega t))} \tag{1}$$

Since is $V_0(t)$ an odd function, $a_n=0$ and $b_n$ is given by

$$b_n = \int_0^T V_0(t)\,\sin(n\omega t) \tag{2}$$

The total harmonic distortion is a measure of harmonic distortion present in inverter output.

The total harmonic distortion is given by

$$THD = \sqrt{\frac{\Sigma_{n=2}^{\infty} V_n^2}{V_1^2}} \tag{3}$$

Where Vn is the nth harmonic voltage and $V_1$ is the fundamental voltage.

## VII. MODES OF OPERATION

There are five modes of operation. During zero state, no switch conducts also the absence of capacitor and inductor means no free-wheeling mode.

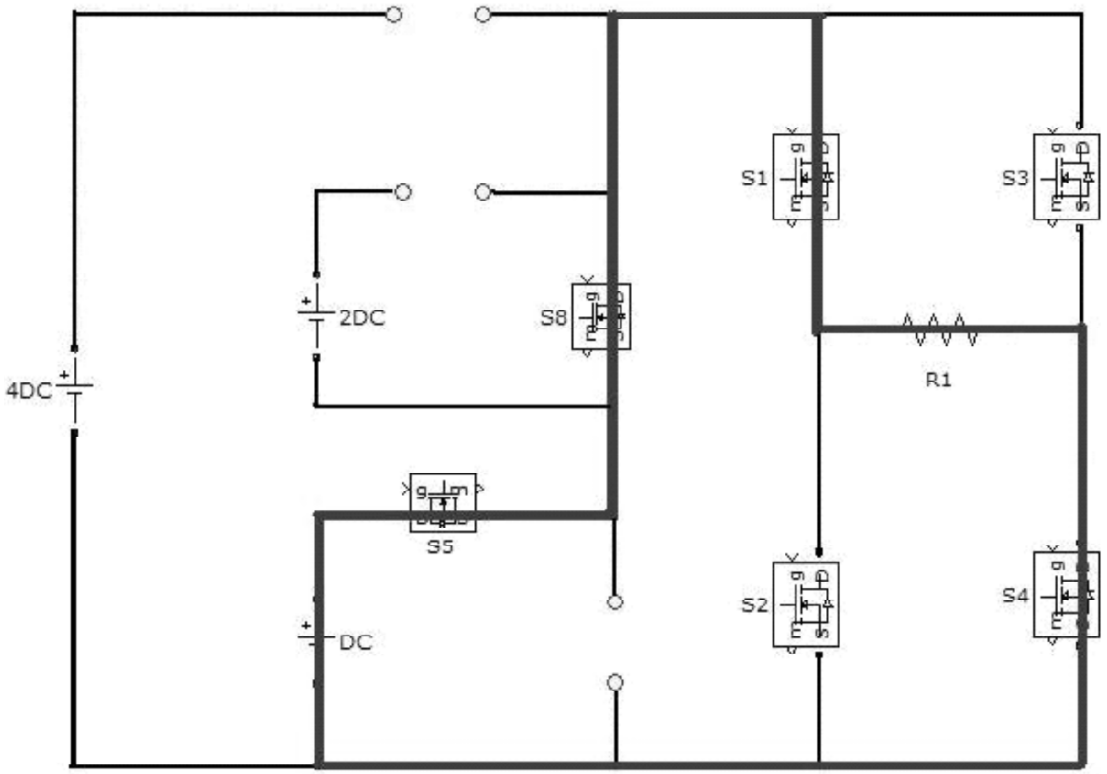


**Figure 3(a): Mode 1 equivalent circuit**

The switches S5 and S8 are ON to produce $1V_{dc}$ at output. The other source side switches S6, S7 and S9 are in OFF state condition. The switches S1 and S4 are ON state and produce positive half of H-bridge. During mode 2 switches S6 and S7 conduct with S1 and S4 for positive mode. S2 and S3 switches conduct during negative mode of operation.

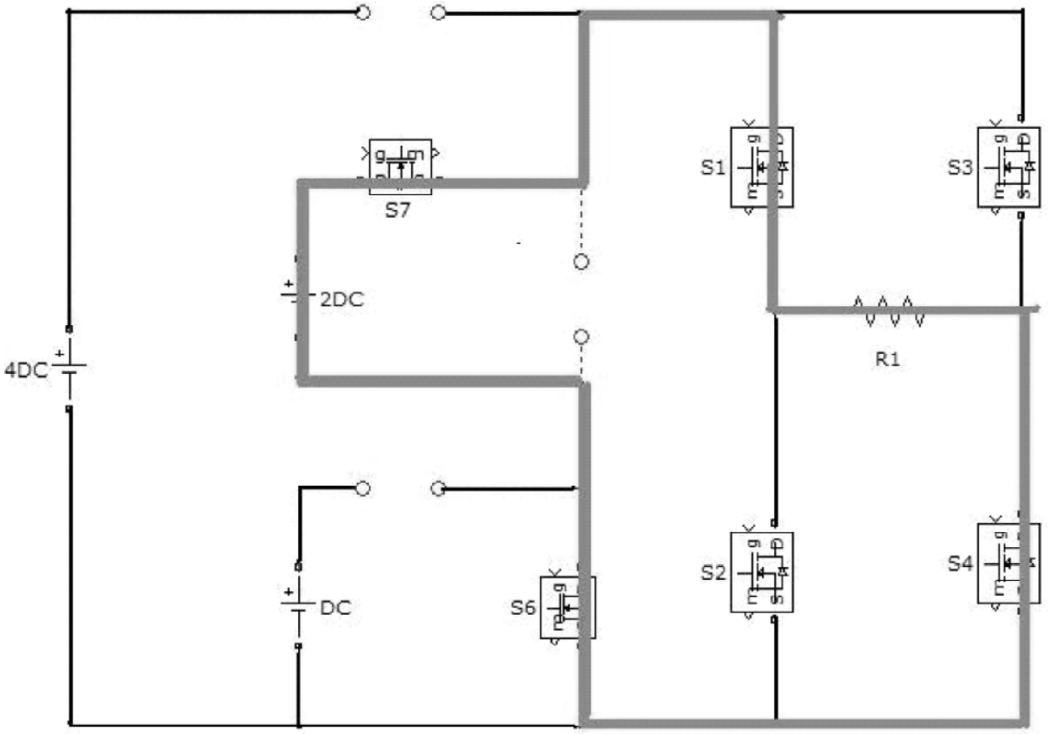


**Figure 3(b): Mode 2 equivalent circuit**

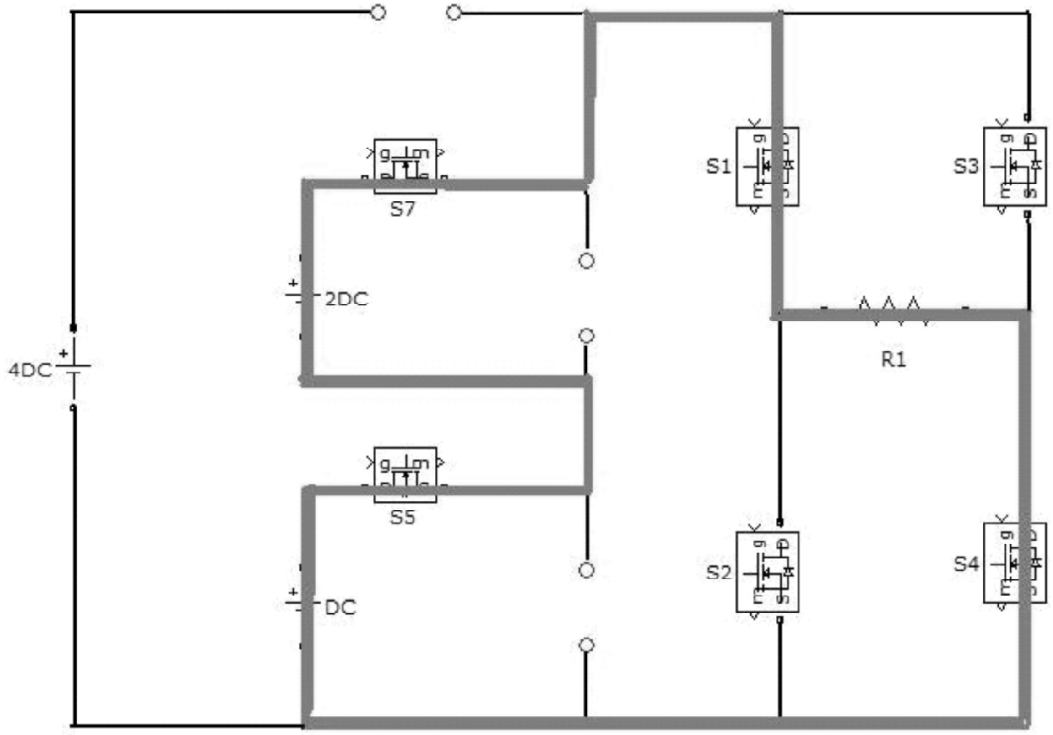


**Figure 3(c): Mode 3 equivalent circuit**

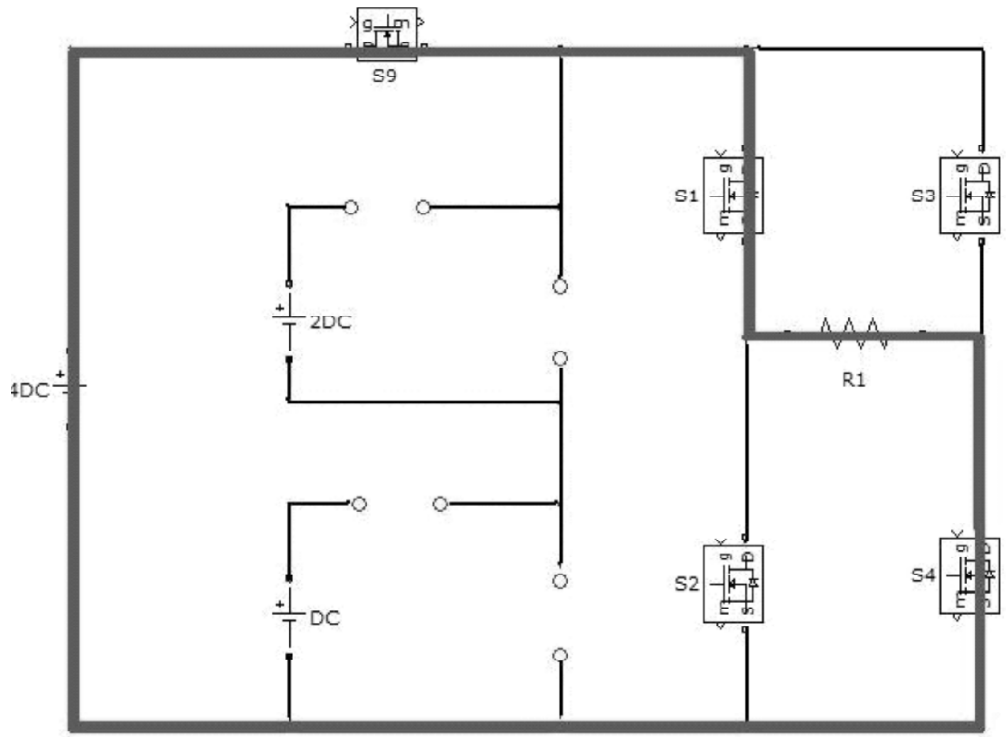


**Figure 3(d): Mode 4 equivalent circuit**

During Mode 3, the voltage sources V1 and V2 are switched ON by S5 and S7. The other switches are turned off. During the fourth mode of conduction the switch S9 conducts and all other switches are off. The output obtainedacross RL load is $4V_{dc}$.

## VIII. SIMULATIONAND RESULTS

The circuit model is implemented in Matlab environment and simulated. The input voltages are having the ratio of 1:2:4 are 100V, 200V and 400V. The output is taken across the RL load.

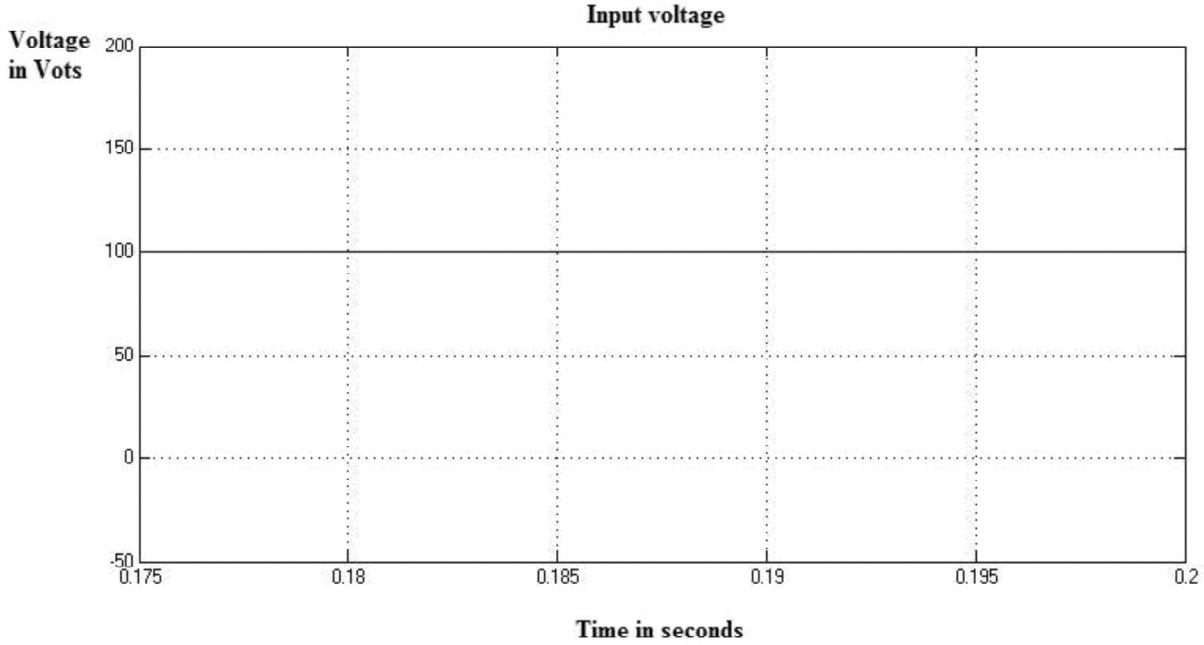


**Figure 4(a): Asymmetrical input 100V**

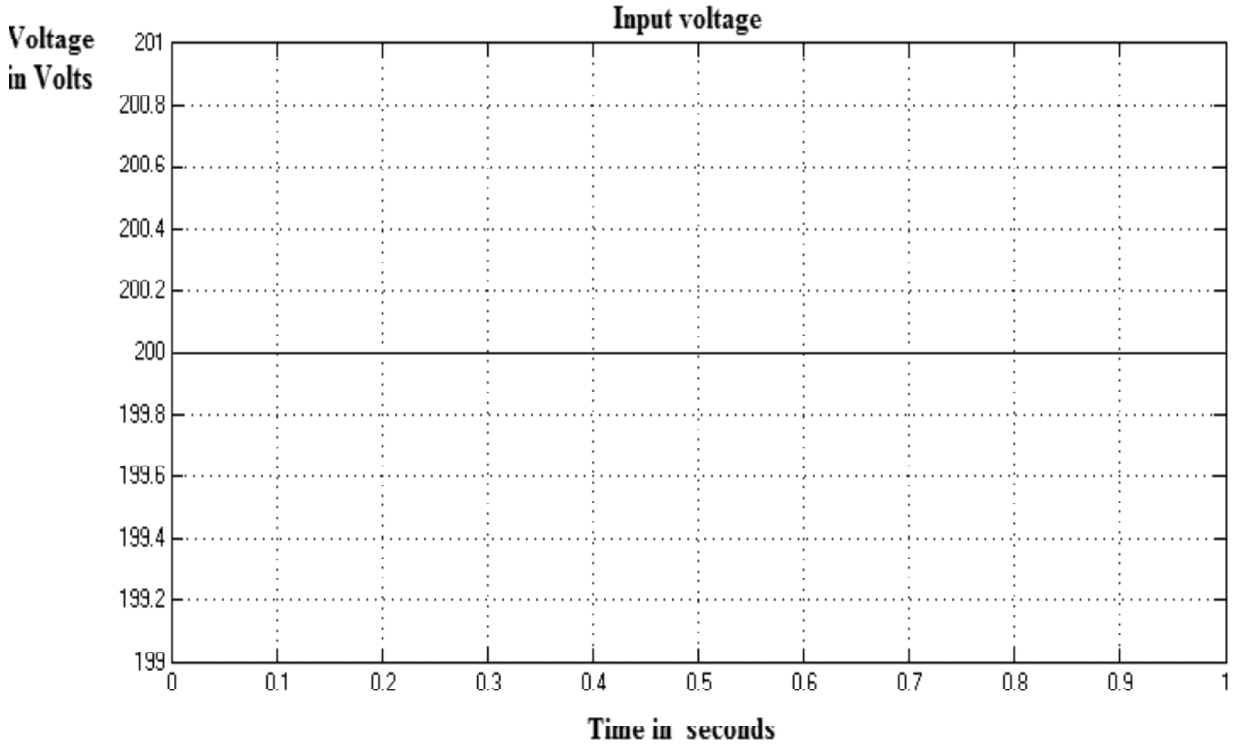


**Figure 4(b): Asymmetrical input 200V**

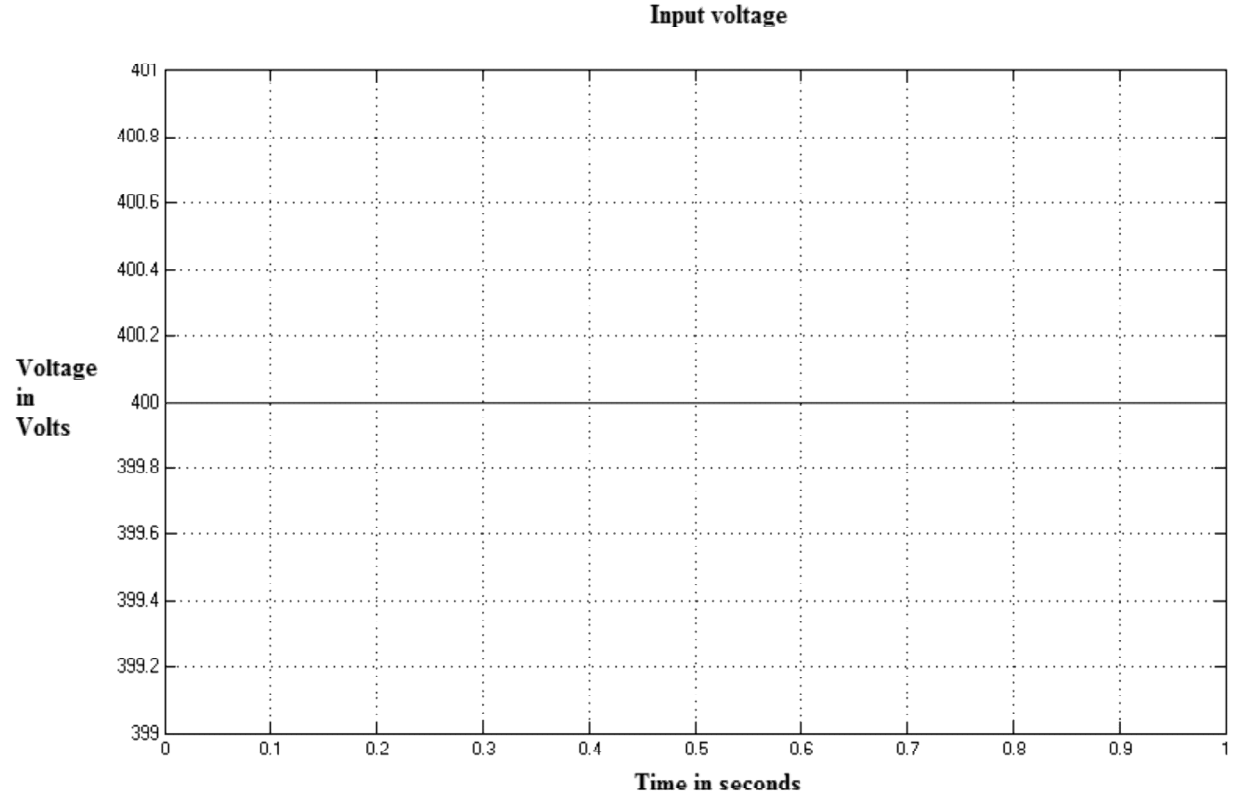


**Figure 4(c): Asymmetrical input 400V**

The asymmetrical configuration allows input voltages in the ratio of 1: 2: 4. To obtain output voltage as 250V, the input voltages can be given as 25V, 50V, 100V.

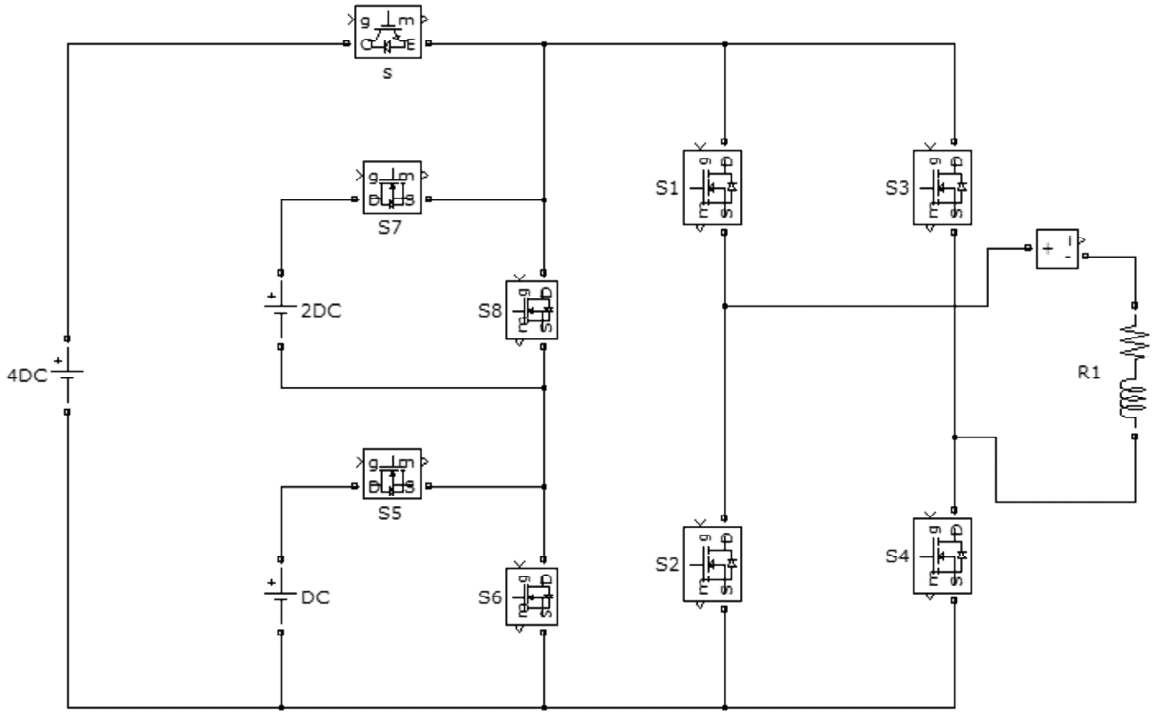


**Figure 5: Simulation of inverter with RL load**

The output taken across RL load is nine level stepped wave output.

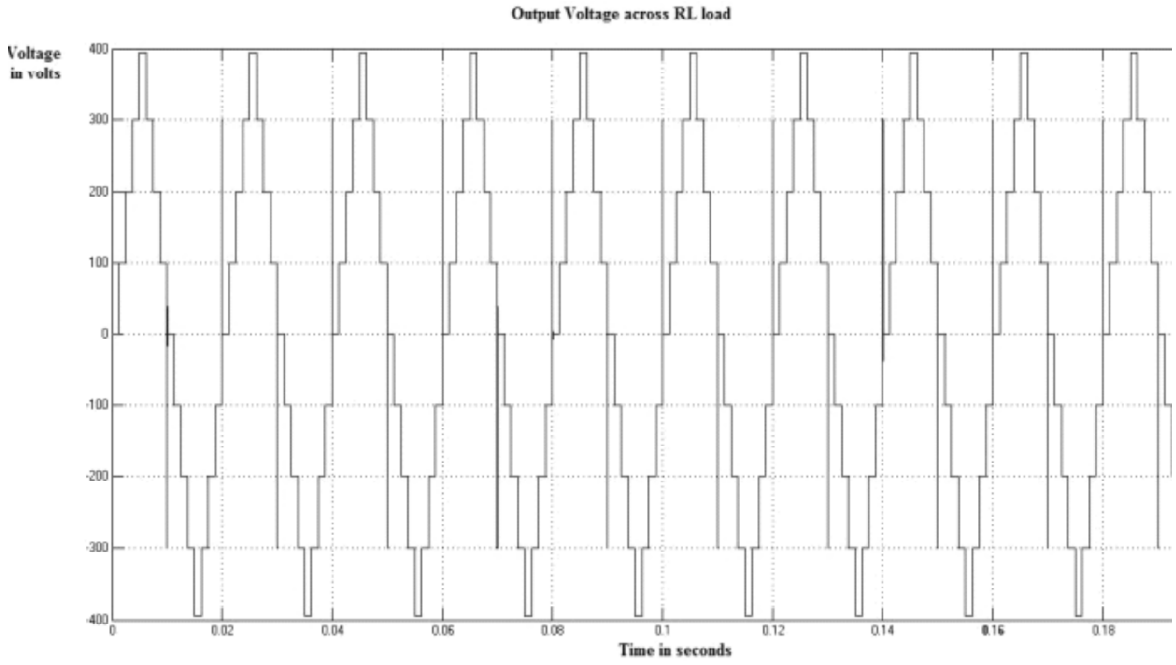


**Figure 6: Output voltage across RL load**

Thee voltage spikes occur whenever voltage rises 0 to $1V_{dc}$. The output can be obtained as 230V which can be obtained by flexible input 50V, 100V and 200V. The nine level output obtained across the motor has peak to peak voltage of 800V.

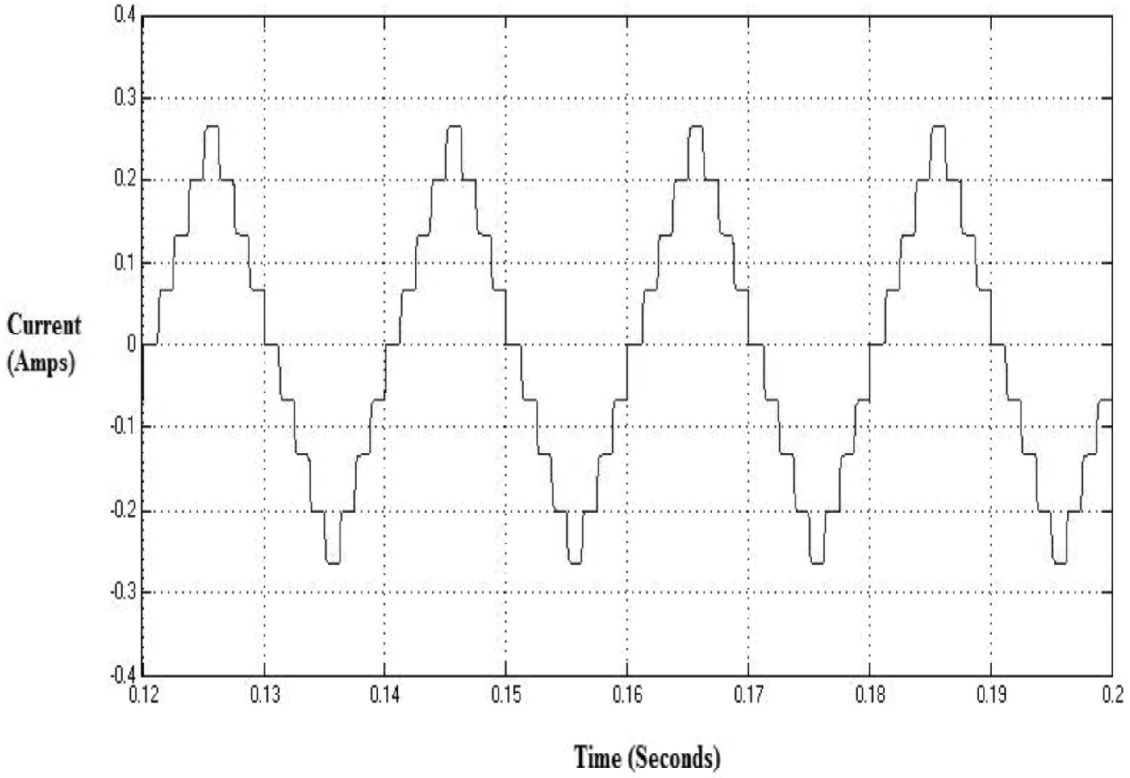


**Figure 7: Output current across RL load**

The current output is a stepped waveform obtained across RL load. The peak to peak current is 5Amps.

A single phase asynchronous motor (capacitor start) is used. The output is taken across the motor.

The motor starts slowly and quickly picks up speed. The motor reaches 1500RPM and continues at same speed. The motor speed can't be controlled as that being a disadvantage. But this drive is excellent choice for constant speed and torque applications.

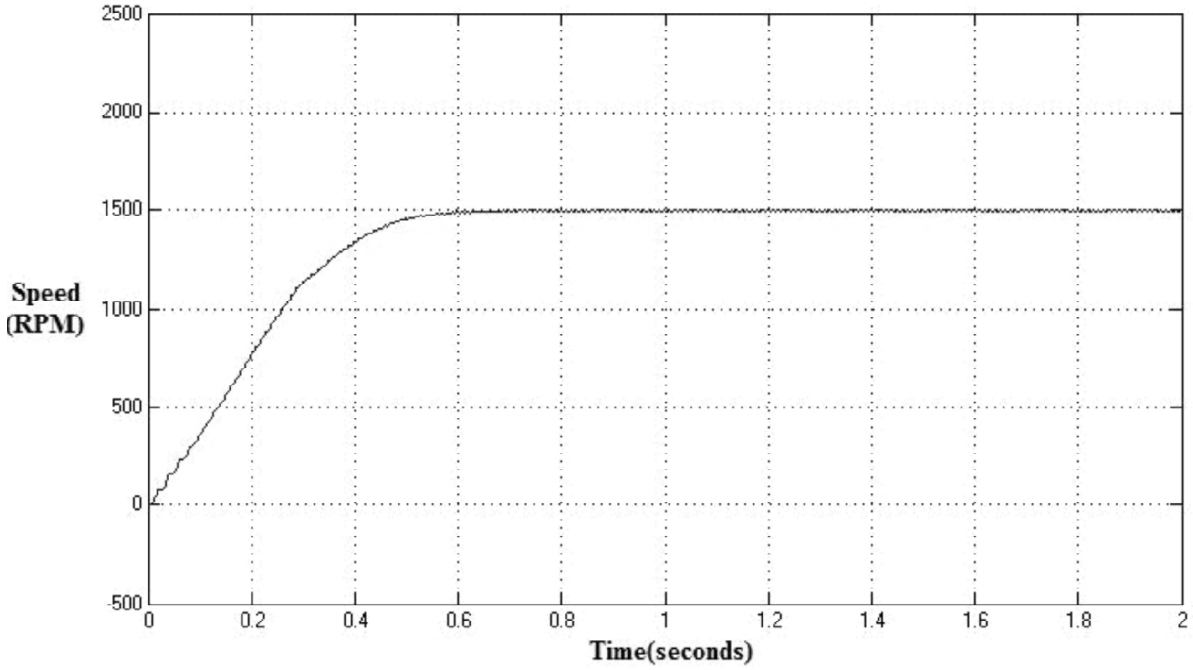


**Figure 8: Speed characteristics of the single phase asynchronous motor**

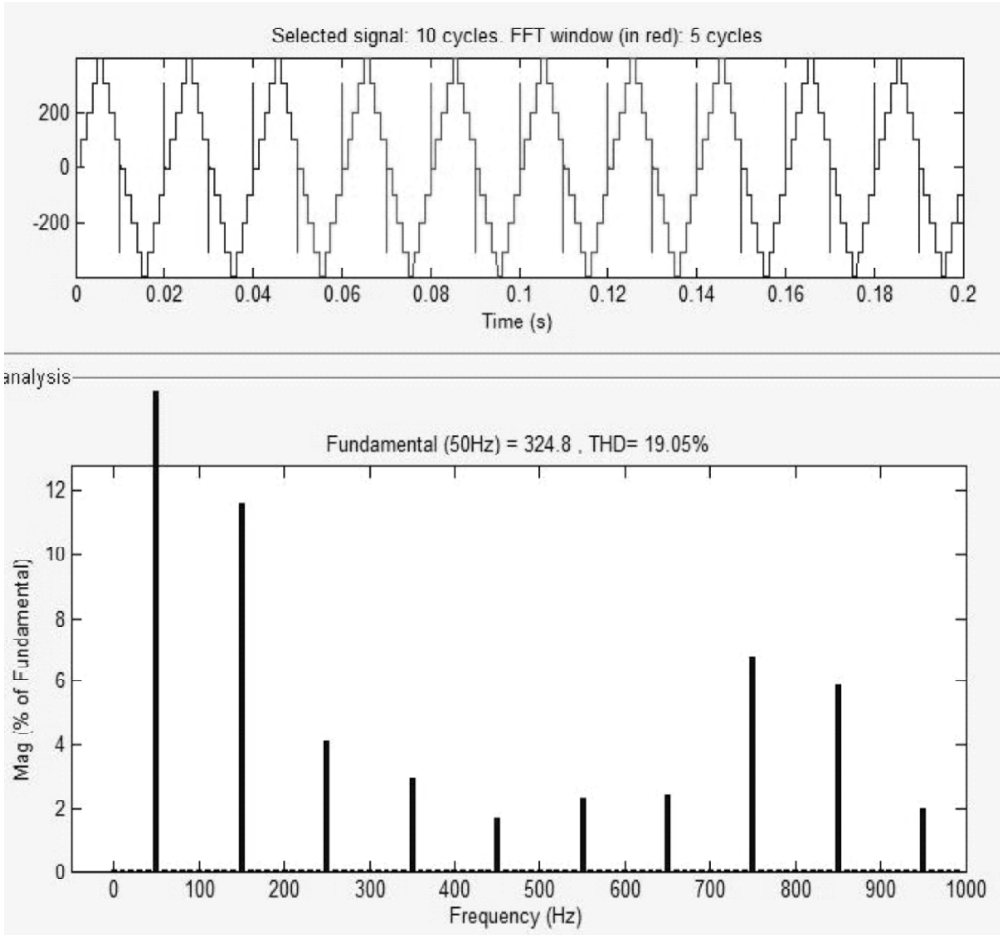


**Figure 9: FFT analysis for total harmonic distortion**

The total harmonic distortion analysis is obtained by Fast Fourier transform tool in Matlab software. The THD is measured to be 19.05%. The cascaded multi-level inverter can be used as a comparison with this inverter.

A comparison ofsymmetrical nine level mli and improved level module technique is done.The parameters such as number of switches, THD, Fundamental component and third harmonic are used to compare both the inverters. The switches are reduced and the harmonic levels remain the same for both topologies. The result obtained is nearer to previous topology. The $5^{th}$ and $7^{th}$ harmonic content are also similar. This topology incorporates more voltages and reduces the switches to achieve the similar output. The FFT shown in figure. 8 shows the selected waveform, fundamental component.

**Table I**
**Comparison of symmetrical 9-level MLI and level module topology**

| *S.No.* | | *Comparison of symmetrical 9 level and level module topology* | |
|---|---|---|---|
| | *Parameters* | *Symmetrical 9 level mli* | *Level moduletopology* |
| 1. | No. of Switches | 12 | 9 |
| 2. | Fundamental | 323.7 | 324.8 |
| 3. | Thd | 18.18% | 19.05% |
| 4. | $3^{rd}$ harmonic | 11.71 | 11.59 |

## IX. CONCLUSION

In this paper, a new level module topology is proposed for an application where dc to ac power conversion takes place with asymmetrical source such as batteries, fuel cells, and renewable energy sources. The new level module topology is designed with lesser switches and added dc source. The voltage and current waveforms are obtained, and show stepped wave peak to peak output.

The proposed inverter with modes of operation, simulation, THD analysis and comparison with conventional system is done. The pwm pulses are generated based on the requirement of the inverter switches. The results obtained show similar performance even by changing design and reducing switches.

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