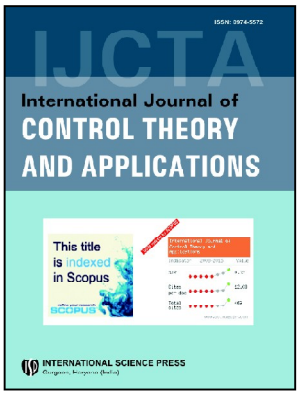

International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 10 • Number 28 • 2017

Design of Low Power Latched Comparator in 45nm for Cardiac Signal Monitoring

N. Bala Dastagiri and K. Hari Kishore

KL University, Vadeeswaram, Guntur

Abstract: This work proposes a new architecture for latched regenerative comparator that is suitable for implementation in cardiac Implantable Medical Device applications. In the proposed circuit of the latched comparator, the low transistor count is used to reduce power consumption. Moreover the proposed comparator uses the positive feedback mechanism to overcome the non idealities like offset voltage and kickback noise. The work presented in this paper is simulated using Tanner EDA tools in 45nm technology. The proposed work is designed well to operate with the frequencies between 50 to 250 KHz and with supply voltages from450mV to 1V. The non-idealities of the proposed comparator are considerably and power dissipation is also reduced.

Keywords: Cardiac Implantable Medical Device applications, low transistor count, Kickback noise, comparator.

1. INTRODUCTION

Comparators are one of the crucial components in the design of analog to digital converters (ADCs) which are very necessary in most of the applications related to signal processing. One important application is Cardiac Implantable Medical Device for monitoring cardiac Signals. Such applications are implemented in CMOS nanometer technology with a lot of digital signal processing circuits as well as analog circuits. The overall performance of the device depends on the analog to digital converter circuits. Hence, there is a need to improve comparators. These are usually energy constrained and they are battery operated. Therefore it is very essential to design the low power circuits for increasing battery life of the device [1], [2].

Cardiac Implanted Medical Device is installed with a physical contact between the tissue and the electrodes. However, it is less immune to noise sources which are outside the body when compared with the wearable cardiac medical devices. The major drawback of these systems is a risky surgery and it is very expensive. Also the lifetime of the device is very crucial and it is needed to work for several years. To address this issue, our interest is on the design of a low power comparator. The vital cardiac signals are of medium speed, therefore the device doesn't need high speed but power dissipation is the major issue. A 7-bit Successive Approximation Register ADC with clock frequency as 100 KHz is used in our circuit design which is acceptable in the intended design [3, 4].

In this brief, we tried to optimize the conventional latched comparator in terms of power dissipation and kickback noise. Moreover we tried to optimize the comparator for frequencies between 50 to 250 KHz and between the voltages from 400mV to IV. However, the designed latched comparator is not only used in Cardiac applications but also it can be used in other applications by simply varying the operating point.

Regenerative latched comparators or latch based sense amplifiers are used generally used in low power applications. Due to the existence of positive feedback mechanism, the response of the latched comparator is very fast and accurate. Moreover, low power consumption of latched comparators is due to the reduction static leakage currents [5, 6, 7, 8].

In this work, a new architecture of dynamic latched comparator is presented with high resolution and accuracy. The proposed architecture of latched comparator dissipates a few nano watts of power at medium frequency of operation. The proposed latched comparator fits into the applications where limited source energy is available. This work is organized as follows. The preceding section establishes the various architectures of latched comparators. In section III, the proposed comparator architecture is demonstrated. In Section IV, the simulation results are presented and analyzed including the comparison performance of key parameters between the existing and proposed architectures of the latched comparators for cardiac IMDs. Finally in section V, conclusions are drawn.

2. EXISTING LATCHED COMPARATOR IN CARDIAC IMDS

Due to the existence of numerous latched regenerative comparator architectures, it is difficult to initiate the details of all the available architectures. Therefore, in this brief a few basic architectures of latched comparators are compared.

In general all the latched comparators operate in two modes of operation, initiated by the clock input signal. During the first phase known as reset phase, clock input is 0V and the input signal is given to the comparator and the positive feedback of the latch is disabled, thus both the outputs are charged to VDD. In the second phase of the comparator known as regeneration phase, the clock input is VDD v and whenever the input signal is applied, the outputs reaches their final values depending on positive feedback mechanism of the latch.

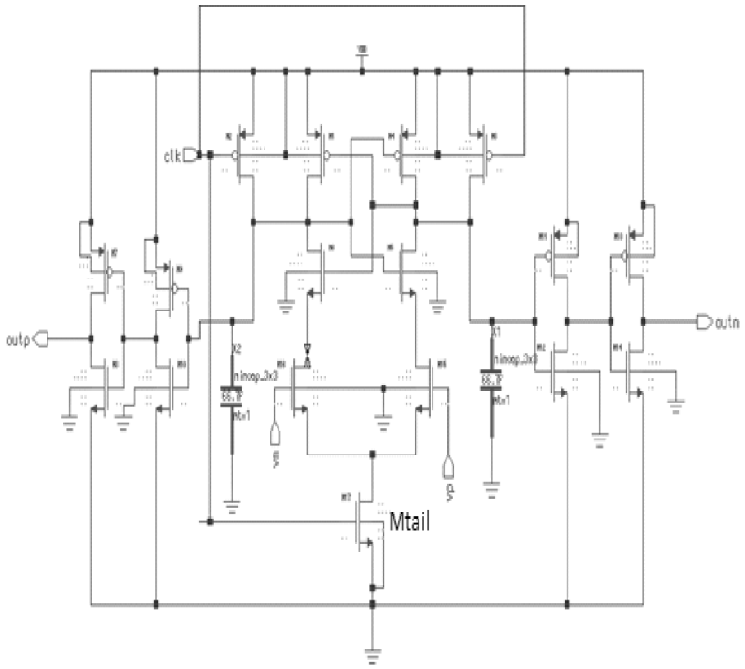

Figure 1: Schematic Diagram of Balance Latched Regenerative comparator

The schematic of regenerative balanced latched compararto is depicted in figure 1[9]. In this architecture of the latched comparator , the capacitors are placed in parallel form to reduce the thermal noise. Infact reducing thermal noise alone generates a noise called kickback noise.In this circuit almost all the transistors work in the weak inversion region.

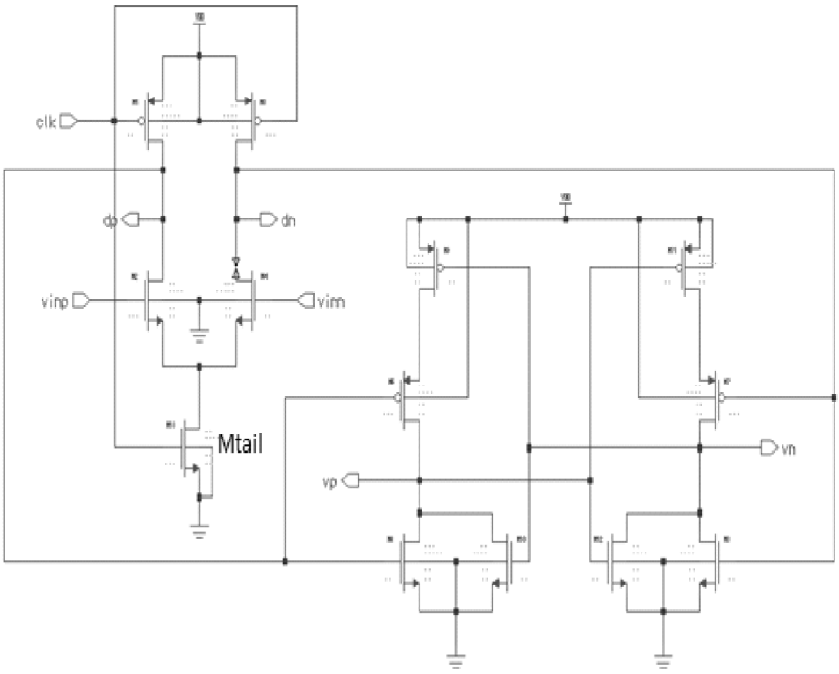

Figure 2: Schematic diagram of Single clock Dual rail dynamic comparator

The architectural circuit of the Single Clock Phase dual rail dynamic comparator is depicted in figure 2[10].Dual rail dynamic comparator dissipates more power when compared with the architectures of single rail dynamic comparator. In constrast,dual rail latched compared is choosen as it generates less kickback noise.

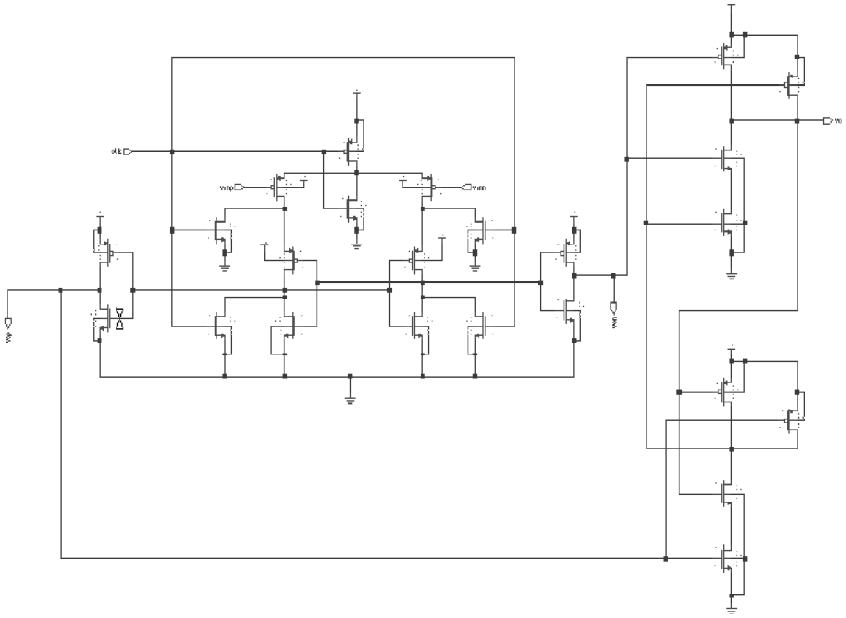

Figure 3: Schematic Diagram of SR latched Dynamic Comparator

The architecture of SR latched regenerative comparator is shown in figure 3[11]. The SR latch implemented in the comparator circuit is used to store the final value of comparison during the comparison mode for the total clock cycle. In this circuit, the output is loaded with unique values by the use of inverters. For the reduction of thermal noise and kickback noise the common mode input voltage is taken in mid rail voltages.

3. PROPOSED LATCHED COMPARATOR

The architecture of proposed latched comparator are depicted in figure 4.

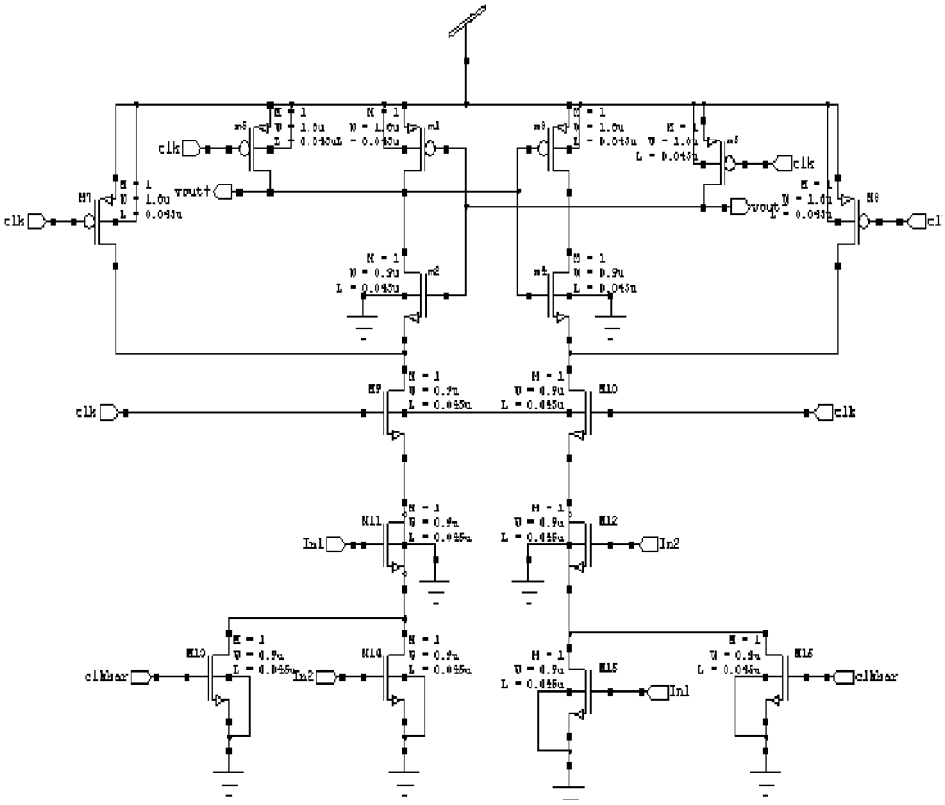

Figure 4: Proposed architecture of latched comparator

In SAR ADC, the accuracy is degraded due to the effect of the thermal noise. The effect of thermal noise can be drastically reduced by the increasing the size of the input transistors which intact increases kickback noise. The proposed comparator is mainly designed to overcome the impact of the non-idealities of the comparator namely thermal noise, Kickback noise and offset voltage. Moreover in order to achieve the low power dissipation single stage clocked comparator is chosen. To overcome the non-idealities of the comparator, the proposed design uses a splitter footer comparator. Also proposed latched comparator uses cross coupled compensation technique for addressing this issue. In figure 4 architecture of proposed comparator is depicted. Normally kickback noise occurs due to the fast change of source and drain voltages present at the input transistors. In the proposed design the compensation transistors M9 and M10 are used to reduce the residual kickback noise.

The proposed latched comparator operates in two modes of operation. During the reset mode of operation the clock input is given as 0V, the transistors M5-8 will be on ON state leading both the outputs to VDD. During the comparison mode of operation, the transistors M15-16 will be on state and the transistors M5-M8 will be in OFF state. Depending on the input values applied one of the output goes to VDD and the other output will be at 0V. The splitter footer structure and the compensation transistors reduce the non-idealities of the comparator.

In this proposed lathed comparator circuit, kickback noise is cancelled out by using the compensation transistors M9-10 and these transistors are used to provide isolation at the transistors where the inputs are given. This will be offering shielding between input and output nodes of the comparator, thus reducing the kickback noise. For the latched comparators, the input referred offset voltage is the performance metric that alters the performance of the system.In the proposed architecture of latched comparator, the offset voltage will be the static offset voltage as the common mode input voltage is kept at mid rail voltages.The proposed comparator has the offset voltage based on Gaussian distribution whose deviation is $\sigma os = \Delta VIN_{\min} / \sqrt{2} erf^{-1}(2Y-1)$.

4. SIMULATION RESULTS AND DISCUSSIONS

In this part of the brief, the simulated results of the proposed lacthed dynamic comparator are analyzed and presented graphically. Also the comparison of proposed dynamic latched comparator with the existing architectures is tabulated. The Simulation is carried out in CMOS 45nm technology using Tanner EDA tool.

In figure 5 the transient response of the proposed latched comparator is demonstrated for the inputs with the specifications of Vinp=1V amplitude sinusoidal wave, Vinn=0.6V which is a constant reference voltage. The input is Clk=1V with a frequency of 100KHZ.

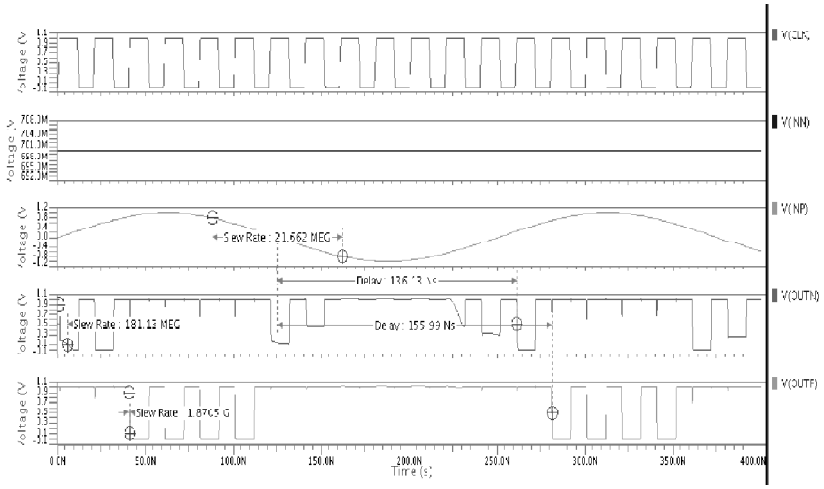

Figure 5: Transient response of proposed latched regenerative latched comparator

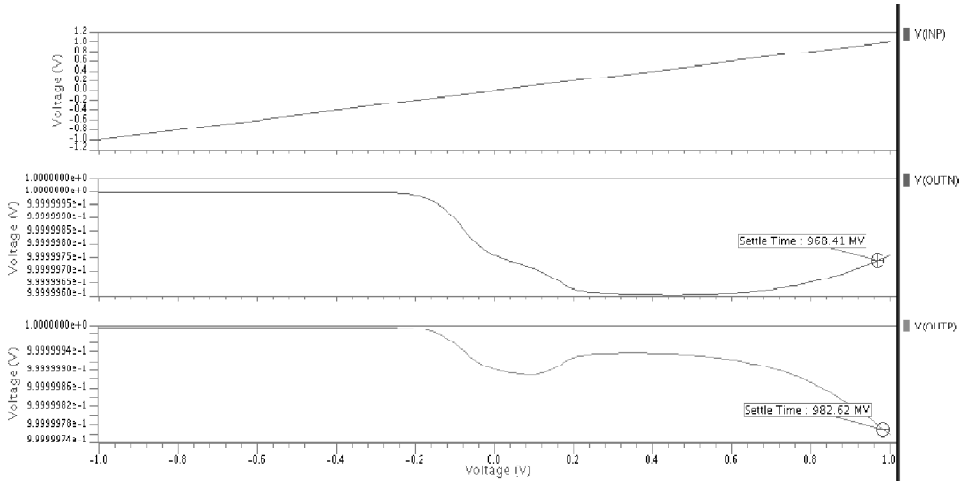

Figure 6: DC response of proposed latched comparator

The figure 6 shows the DC characteristics of the proposed latched comparator with the following specifications. For this inputs are supplied with constant 0V and one of the input is set to sweep from -1V to +1V with step division of 0.01V. DC response provides the offset voltage of comparator.

A Monte-carlo simulation with 100 runs is carried out to check the influence of mismatches in transistors. The transistor mismatches have insignificant effect on the reduction of kickback noise achieved by the proposed solution.

Table I
Comparison of Comparator Properties

Comparator Properties	*[9]*	*[10]*	*[11]*	*Proposed Comparator*
Power dissipation (nW)	2.6319	1.1370	6.04	2.5
Kickback noise (mV)	13	6.2	5.9	4.5
Offset voltage	7.8	7.9	8.1	6.2

From the Comparison table I, it is shown that the proposed comparator dissipates low power and produces less kickback back when compared with the existing architectures .

5. CONCLUSION

This brief studied the various architectures of dynamic latched comparators for cardiac IMD and proposed a new architecture of latched comparator to overcome the non–idealities of the comparator. The new proposed circuit achieves good considerable results and it is shown with the simulation results using Tanner EDA tools in CMOS 45nm Technology. The simulation results of the proposed circuit of dynamic comparator generates low kickback noise, yields low offset and also dissipates low power when compared with other works used in cardiac IMDs.

ACKNOWLEDGMENT

This work is sponsored and assisted by Annamacharya Institute of Technology and Sciences, Rajampet, India and we are thankful to the organization. We thank Prof. Abdul Rahim and Mr.S.Fahimuddin for their valuable suggestions and mind stimulating discussions.

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