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Design of Intelligent Controller for Temperature Process on FPGA

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Abstract: This paper investigates about the execution of fuzzy logic controller (FLC) on reconfigurable device. The reconfigurable device programmed was Field Programmable Gate Array (FPGA). The synthesis and simulations were carried out using Altera Quartus II software tool. The coding for the logic cells configuration was carried out with Very High Speed Hardware Description Language (VHDL). The effective implementation of FPGA was noted with less logical elements (LEs) count, the modules were configured with FLC algorithm using Mamdani's function. This paper projects the complete synthesis of VHDL program for fuzzy logic control algorithm with the mathematical model for heat exchanger process under different input conditions. The functionality of the fuzzy controller was verified on the FPGA chip.

Keywords*:* VHDL, FPGA, Shell and Tube Heat Exchanger (STHE), Digital FLC.

1. INTRODUCTION

The main aim of this paper was to implement a digital fuzzy logic controller on an FPGA for a heat exchanger temperature process. The controller was tracking and maintaining the temperature of the heat exchanger outlet. MATLAB/Simulink was used to develop to formulate the mathematical model of the process plant. Various cores of the FPGA were partitioned and independent functional modules. The Altera Cyclone II FPGA hardware device has been chosen and for synthesis of the VHDL code Quartus II software development tool has been used. This paper projects the complete synthesis and simulation of VHDL program for fuzzy logic control algorithm with the simulation model for heat exchanger process. In the literature survey although various control methods are mentioned for the control of STHE. But fuzzy logic has been preferred over the conventional methods because of fuzzy inference system which creates an associative memory with linguistic rules. Fuzzy controllers are better suited to handle the nonlinear plants. The mathematical model of the STHE process was obtained using FOPDT modeling technique and converted into digital representation for FPGA implementation. FPGA has been preferred over other digital programmable devices like DSPs or microcontrollers because of its low cost and higher performance index. Low cost microcontrollers can edge over the FPGA but they can't be used for complex operations in real time.Therefore, intelligent and complex controllers have been implemented using logical elements of reconfigurable devices and these chips run significantly faster.

In the last decade many researchers tried to explore more on the intelligent controller implementation on FPGA [1]-[4]. Nian Zhang et al. [5] explained about the hybrid fuzzy model design for a navigation system. The proposed algorithm was evaluated with VHDL coding for FPGA implementation. Saber Krim et al.[6] discussed about the limitations of conventional PI controller over the fuzzy controller. It

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projected the improvement of the Conventional Direct Torque Control (CDTC) of an induction motor by designing Fuzzy controller on FPGA. The simulation and implementation of the controller was done by Xilinx System Generator (XSG). K.M. Deliparaschos et al.[7] in their paper proposed about the exclusive active fuzzy rules operation at high frequency with less complexities in hardware. In their work zero-order Takagi-Sugeno method has been used for Fuzzy Logic implementation.

For more complex algorithms, implementation schemes based on multiple DSP cards have known limitations such as the design complexity, cost, and compatibility problems. Heat exchangers are devices in which heat is transferred between two fluids without any mixing of the fluids. The shell and tube heat exchanger model is used to implement the controller mechanism. The nonlinearity involved in the process makes the behavior quite uncertain. Hence fuzzy logic based controller has been chosen.

The paper has been organized as follows: Second section describes about the Process dynamics and mathematical model obtained. Third section outlines about the FPGA architecture, fourth and fifth section discusses about the Fuzzy logic implementation methodology and synthesis results obtained. Finally we analyzed the inferences obtained with the controller implementation on FPGA.

2. HEAT EXCHANGER- PLANT DESCRIPTION AND MODELING

Shell and Tube Heat Exchanger (STHE) are most commonly used in process industries for heating or cooling process fluids and gases etc. They deliver reliable heat transfer performance by utilizing a high turbulence as well as counter flow, making one or more passes. The STHE system is constructed using 37 copper tubes and a carbon steel shell. A heat exchanger has two flowing fluids partitioned by a solid wall. Heat is transferred:

- By convection from the hot fluid to the wall
- Conduction happens through the wall, and
- By Convection from the wall to the cold fluid

Heat exchanger was classically controlled using conventional controller but the intelligent controller performance ascertained that it produces remarkable results. From the set of experiments performed, it has been found that the data supplied for the training are having interaction effect. After conducting the open loop system test, the model has been identified as First order plus time delay (FOPDT). Using 2-point method proposed by Zeigler-Nichols the time delay has been estimated. In the following equation, k_p is the ratio of change in output steady states value and change introduced in the manipulated variable. After substituting the values obtained from Figure 4 the final FOPDT model can be written as:

$$G(s) = \frac{k_p}{\tau s+1} e^{-t_d s} = \frac{.495}{376s+1} e^{-62.73s} \quad (1)$$

After the identification of the FOPDT model conducting the experiments. Then the discrete digital form of the model was used for the VHDL code synthesis. The Fuzzy based controller was tuned. In the following section FPGA architecture has been described with the implementation scope of the fuzzy logic controller.

3. FPGA ARCHITECTURE DESCRIPTION AND SOFTWARE TOOL FLOW

For the resilient clock management in Cyclone II device is carried out by four phase-locked loops (PLLs) as shown in Figure1. It carries out the synthesis for device clock, manages the external system clock and the I/O interfaces. With proper configuration PLLs provide the zero delay buffer, to attenuate jitter or to

synthesize the frequencies. The device memory blocks can access dual port memory in the input/output clock mode [8]. The FLC has been designed using Altera's QuartusII tool and the VHDL coding has been chosen for the process description. In the Figure2 the software tool flow has been clearly outlined. Each elements of the FLC is designed and carefully optimized for synthesis. In the top level design file - *controller.vhd*, the components behavior and process functionalities has been declared for the synthesis. The components described are interlinked with the architectural modeling of the control system.

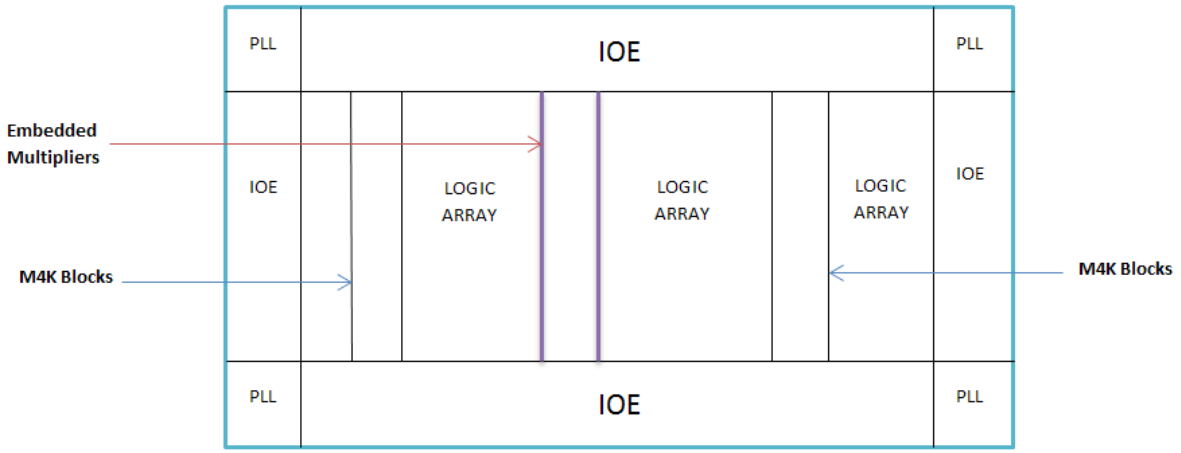

Figure 1: Altera Cyclone II device architecture with logical elements

The fuzzy logic controller was designed to control the temperature of the heat exchanger model. Here the simulations were carried out the first order time delay model obtained from the mathematical modeling of the shell and tube heat exchanger. The controller model was designed with fuzzy rules and the synthesis of the fuzzy rules in Quartus II software has been carried out successfully. The fuzzy controller rules has been coded with VHDL presented in this paper.

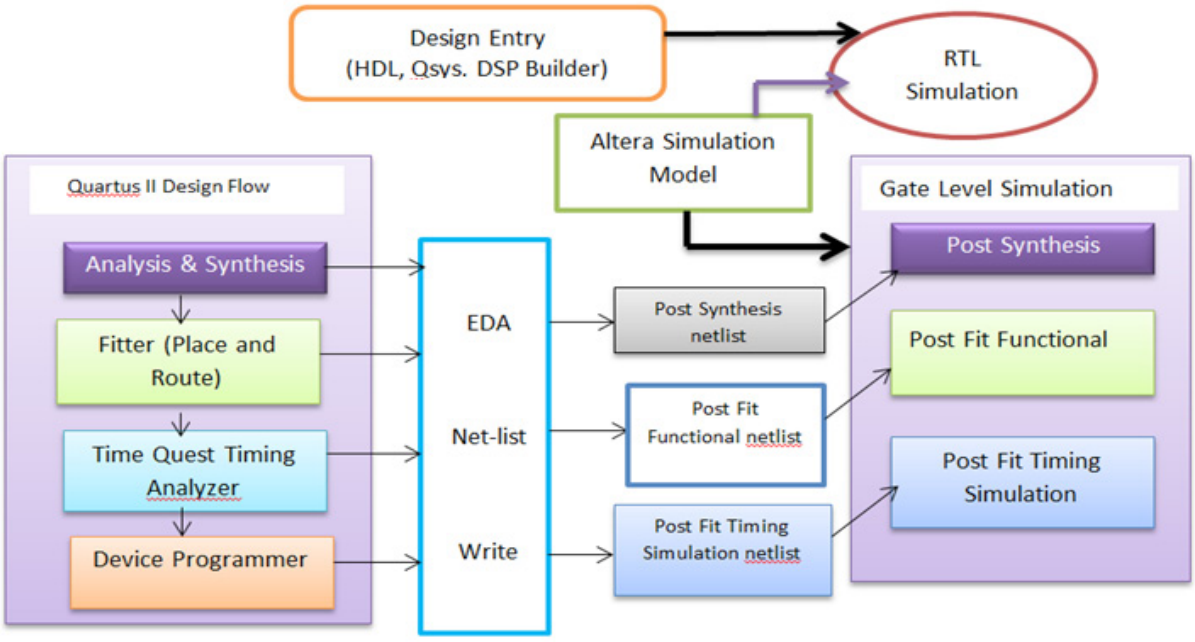

Figure 2: FPGA logical synthesis with Altera Quartus II design tool

4. FUZZY LOGIC IMPLEMENTATION ON FPGA

The fuzzy control algorithm has been identified as one of the method for controller design on FPGA. The controller design logic has been with the high level design blocks in the Figure 3.The simulation results obtained will be discussed in this section.

The control system logic was written in the form of linguistic rules which was stored in the knowledge base. To evaluate the relevance control rules at certain time and to embed the decision for the plant input

- In order to modify the inputs to be interpreted and compared with the fuzzy rules, the fuzzification interface has been created with *fuzzification.vhd* file and a test bench has been created to validate the fuzzification process which was simulated by using ModelSim tool (*fuzzification_tb.vhd* file)

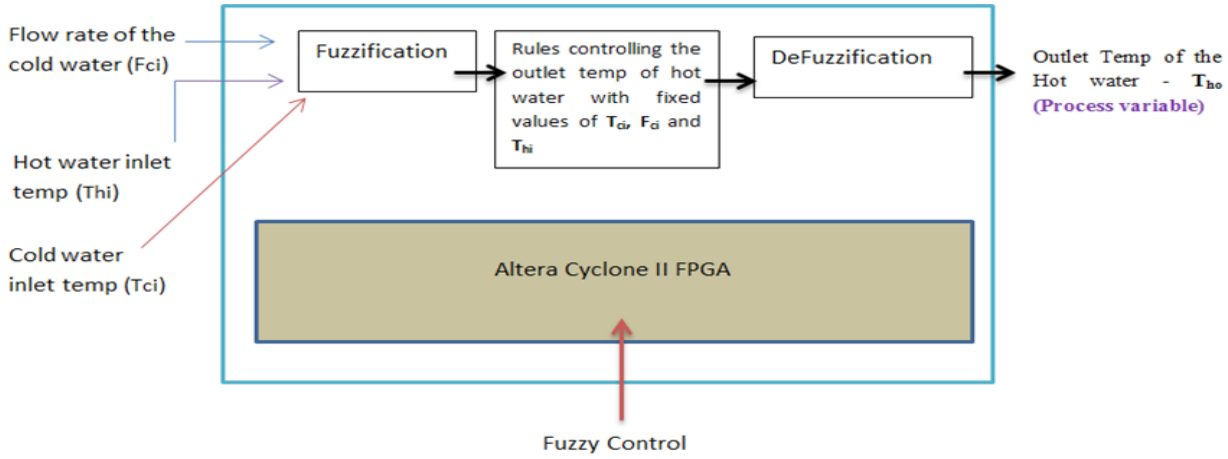

Figure 3: Fuzzy logic controller implementation in FPGA

Alongwith the four major files in the top level design. Figure 4 below shows the flow analysis with all the design files for the controller design. The design description also contains the following two files for the flow analysis and proper synthesis of the controller.

- *Config.vhd* file which holds the package description of the top level design files.
- *Synchronous.vhd* file contains the underlying libraries of the IEEE and standard logic functions from the Intellectual properties to access the math-functions and simulate the top level controller design file.

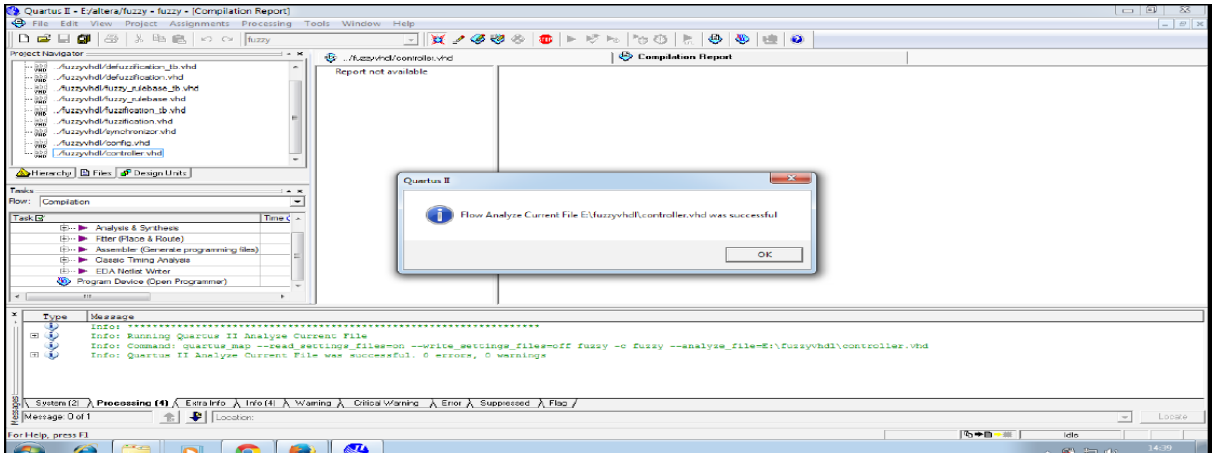

Figure 4: Flow Analyser integrating all the HDL files with the top level design

The fuzzy rules have been designed for the control of STHE. The 2 inputs range membership function has been kept as follows: error = [-30 30], change in error = [0 0.1] while the controller output is in the range of 4-20mA for real time communication with the plant. Figure 5 shows the fuzzy rules with the surface viewer.

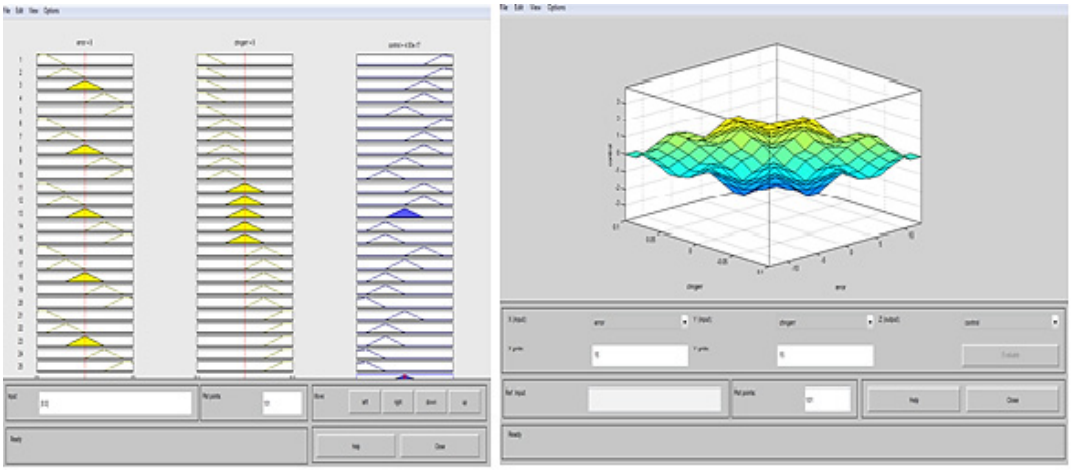

Figure 5: Fuzzy Rules on the surface viewer

5. ANALYSIS AND SYNTHESIS OF VHDL CODE

Analysis and synthesis is one of the phases of VHDL code compilation. In this step the top level design file is integrated with other files of the entity and a proper hierarchy has been created. The software simulator checks the syntax of design and logical error of the program. The technology mapping of the logical representation has also been done in this step. Figure 6 shows the real time working status of the Cyclone II FPGA board with the bit files transferred for FLC algorithm.

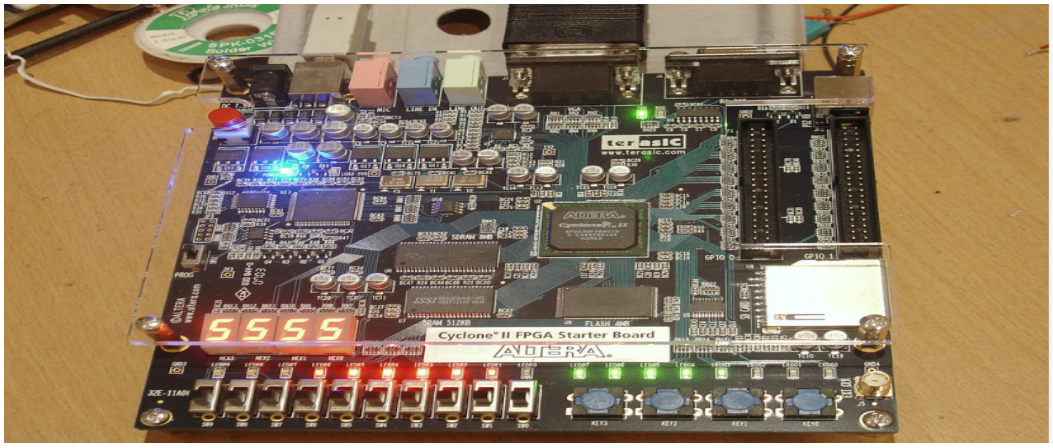

Figure 6: Altera Cyclone II FPGA real time screenshot in functional mode with FLC design

The Quartus II RTL Viewer provide graphical representations of the design. The analysis of the VHDL design and the detail registers allocation was done in RTL (register transfer logic) synthesis, Figure 7. This step also generates *.bdf* and *.gdf* files for exploring the schematics of the design. In the Technology Mapping as shown in Figure 8, the minute level representation of design schematics has been depicted. It has been noticed in the following Figure 9 that the VHDL code for fuzzy logic has been successfully compiled.

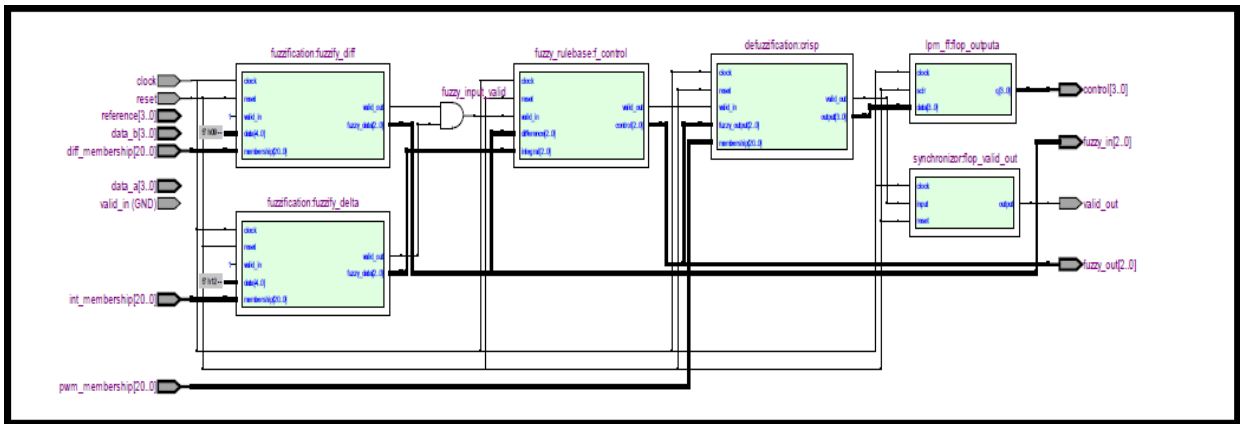

Figure 7: Fine Grained RTL Schematics generated for the Fuzzy Controller design in FPGA

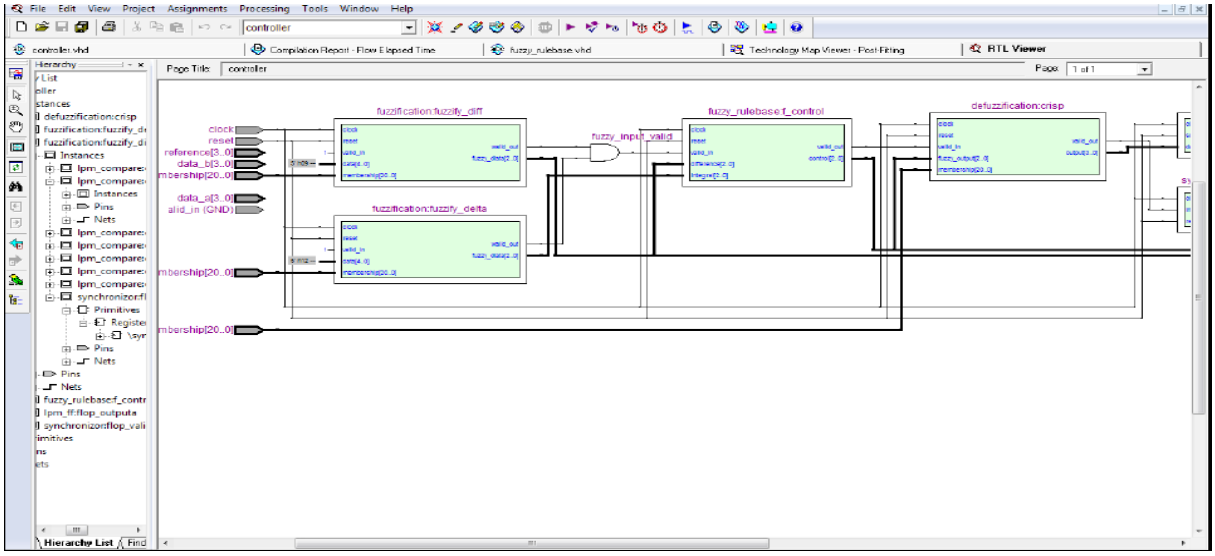

Figure 8: Technology map Viewer for fuzzy control algorithm targeted for Altera's FPGA

In the following Table 1 the detailed summary of the project has been outlined with all the necessary hardware utilized. The table projects the logical elements count, timing model status with total registers count. In our design the Altera Cyclone II family device EP2C20F484C7 has been chosen. The control algorithm shows the optimized result with minimal gate count and less resource utilization.

Table 1

Device Utilization lists for logical implementation of FLC

FPGA Architecture Specifications	*Consumption*
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Functional Successful
Total Logical Elements	18/18752 (< 1%)
Total Combinatorial functions	1/18
Total Registers	18
Total Pins	89/315 (28%)
Total memory Bits	0/239,616
Total PLLs	0/4

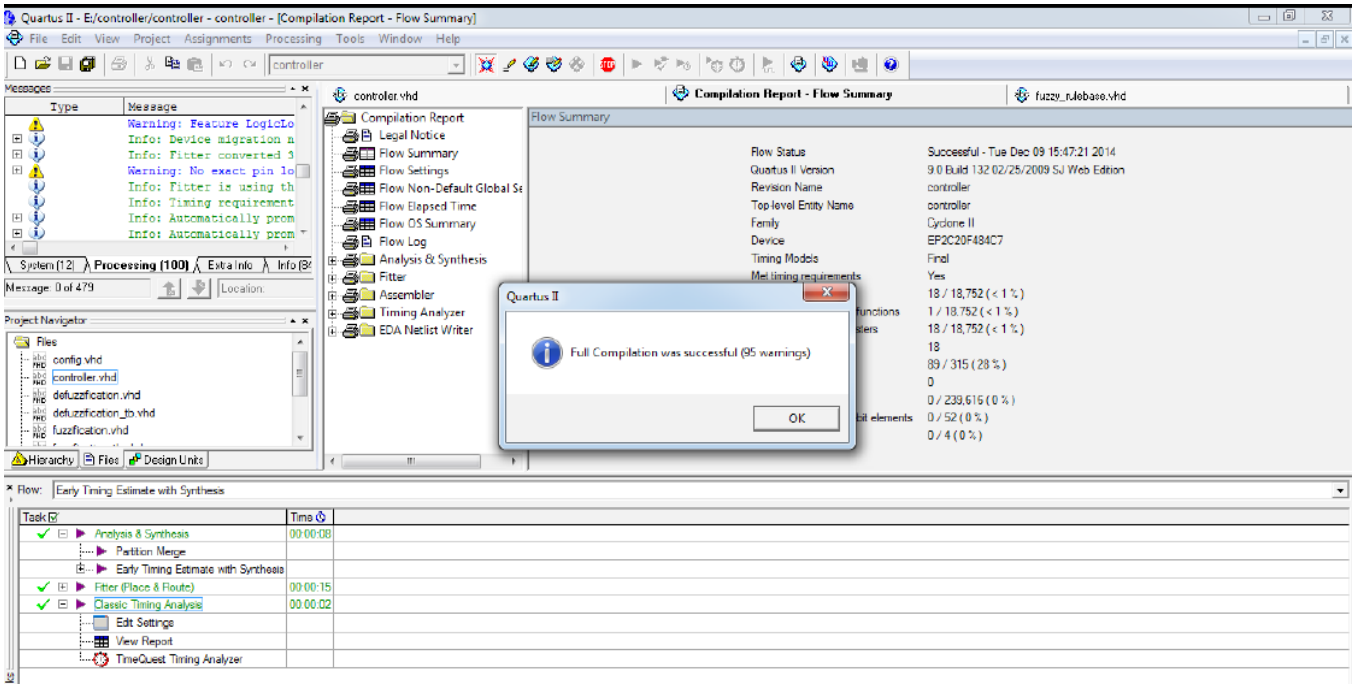

Figure 9: VHDL code compilation in Altera's QuartusII with project summary

6. CONCLUSION

In this paper we presented the design of fuzzy logic controller (FLC) in FPGA that reduces the clock cycles for overall execution of the VHDL code. Hence it can be inferred that the optimized execution increases the overall input data processing rate of the system. For FPGA implementation Altera Cyclone II family device EP2C20 has been chosen and synthesis was carried out with Quartus II tool. The FLC provides a formal methodology for representing, and implementing a human's heuristic knowledge about how to control a system, which may provide a new paradigm for nonlinear systems like heat exchanger. Hence with the reconfigurable devices like FPGA, FLC proves to be competent and well optimized with the above synthesis results.

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