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AN EFFICIENT IMPLEMENTATION OF DWT FOR IMAGE COMPRESSION ON RECONFIGURABLE PLATFORM

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Abstract: Image compression is a significant technique in storage and transmission of digital images as it requires huge data. This paper presents an efficient implementation of Discrete Wavelet Transform (DWT) for image compression on reconfigurable platform. This implementation can be applied for lossy as well as lossless compression. The system is implemented using VHDL and simulated using MATLAB. The experimental result shows that this implementation occupies only 144 slice registers at an operating frequency of 43.630 MHz.

Key Words: *DWT, FPGA, VHDL, image compression, JPEG*

I. INTRODUCTION

Now-a-days, demand and development of multimedia information is growing rapidly which further contributes to insufficient network bandwidth and memory storage. Due to this, data compression becomes more significant for reducing the data redundancy to save memory storage and transmission bandwidth. DWT based image compression such as JPEG 2000 offers major features such as high compression efficiency, lossless color transformation, region-of-Interest Coding, lossless and lossy compression, random code stream access and processing error resilience. DWT is an application of sub-band coding. In sub-band coding, input spectrum is decomposed into set of band limited components called sub-bands. These sub-bands can be assembled to reconstruct the original spectrum without an error.

DWT has become one of the most commonly used techniques for signal analysis and image processing applications. DWT performs multiresolution signal analysis that holds both time and frequency information. Due to its time and frequency domain characteristics, DWT has been widely used for image compression such as in JPEG 2000. Generally, (5/3) and (9/7) wavelet filters are used as default filters for lossless and lossy compression respectively. Since convolution method is based on filter bank structures in implementation of DWT, large number of arithmetic computations and large storage area is required. It also requires features that are not desirable for either high speed or low power hardware applications. Many VLSI based 1-D and 2-D DWT architectures have been developed and implemented to reduce number of slices, internal memory requirements, hardware complexity and increase the design performance.

DWT has been widely used in applications of digital signal processing due to its efficient computation and sufficient characteristics for non-stationary signal analysis. Generally, the structure used for wavelet analysis is as shown in the figure 1.

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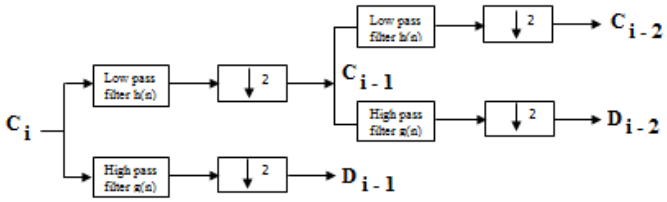

where Cx = Approximation coefficients
Dx = Detail coefficients

Figure 1. One-dimensional DWT decomposition

DWT decomposes a signal into different sub-bands in order to get the lower frequency sub-bands that have finer frequency resolution and higher frequency sub-bands for coarser time resolution. Decomposition of an image can be single level, two level or three level as shown in figure 2.

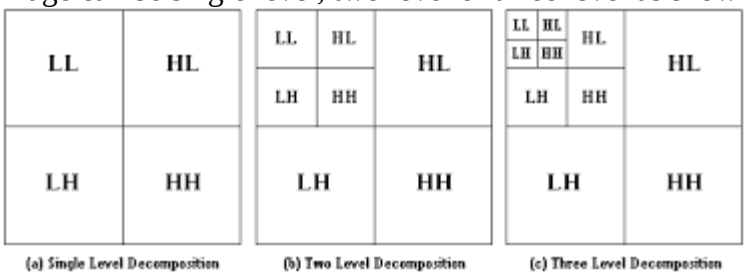

Figure 2. DWT Decomposition

DWT evaluates the signal at dissimilar frequency bands with different resolutions by disintegrating the signal into an approximation and detail information. Decomposition of a signal into diverse frequency bands obtained by successive high pass filtering g[n] and low pass filtering h[n] of the time domain signal. The combination of high pass g[n] and low pass filter h[n] encompass a pair of analyzing filters. Output of each filter comprises half the frequency content, but an equal amount of samples as the input signal. Two outputs together comprise the same frequency content as that of input signal; however, the amount of data is doubled. Hence, in the analysis bank, down sampling by two is applied to the outputs of the filters.

DWT is widely used for image compression as it supports features like easy manipulation of compressed image, progressive image transmission, region of interest coding, etc.

1.1. One-Dimensional DWT:

Initially, the signal is applied to low-pass (LP) and high-pass (HP) filters respectively. Then, the output of these filters (i.e. filtered coefficients) are down sampled to neglect the alternate coefficients. When the output of low-pass filter is down sampled, it contains low frequency components of the signal which are known as approximate portion of the original signal whereas when the output of high-pass filter is down sampled, it contains high frequency components which are known as detailed portion of the original signal. The filter pair low-pass filter h(n) and high-pass filter g(n) used for decomposition of the signal is known as analysis filter-bank whereas filter pair used for reconstruction of the signal is known as synthesis filter bank.

The output of low-pass filter h(n) represents the approximate coefficients and is represented as:

$$y_h(n) = \sum_k x(k)h(2n-k)$$

The output of high-pass filter g(n) represents the detailed coefficients and is represented as:

$$y_g(n) = \sum_k x(k)g(2n-k)$$

II. LITERATURE SURVEY:

This section provides the overview about some of FPGA and MATLAB oriented implementations of DWT algorithm:

Altaf O. Mulani el at [1] presented a combined watermarking and cryptography approach for image authentication. This implementation occupies 2117 slices at maximum operating frequency of 228.064 MHz. This scheme provides improved security without compromising its speed and area.

Venkata Anjaneyulu el at [2] focused their interest on memory efficient FPGA for SPIHT (Set Partitioning in Hierarchical Trees) image compression technique.

P.R.Kulkarni el at [3] suggested robust invisible watermarking for image authentication which is better to retain the original image.

M. Nagabushanam el at [4] proposed a modified lifting scheme based 1D and 2D DWT FPGA architectures for computing the approximation and detailed coefficients of DWT. The system is implemented on Virtex-5 and it requires 1152 slices at 180 MHz.

P.R.Kulkarni el at [6] proposed DWT based robust invisible digital image watermarking which does not affect the quality of original image. This method first combines information of low frequency DWT coefficients and watermark image and then the combination of this is used to extract the watermark.

M. Puttaraju el at [7] proposed FPGA oriented (5/3) integer DWT for image compression. This architecture is based on lifting scheme and can be applied to 2D spatial images from payload instruments.

Durga Sowjanya el at [8] proposed an area efficient and high speed VLSI architecture that utilizes 158 slices at 120 MHz. This implementation requires least computing time and also less area. It is applicable for fixed point 1-D DWT.

M. Nagabushanam el at [9] suggested DWT architecture based on modified BZFAD multiplier that occupies 1152 slices at 256 MHz. According to the author, this implementation is 65 % faster and occupies 44 % less area. It also achieves 35 % power saving.

Abdullah Al Muhit el at [13] proposed a DWT algorithm for image compression which supports JPEG 2000 standards.

III. PROPOSED ALGORITHM

The flow graph of proposed algorithm is as shown in figure 3.

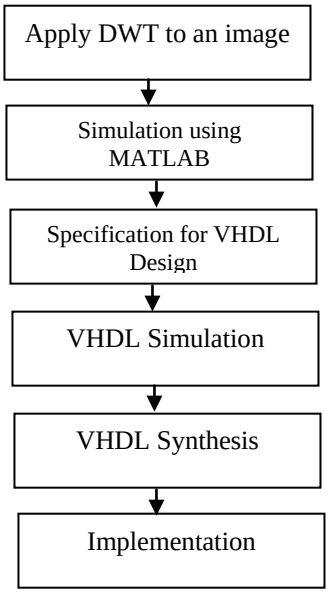

Fig. 3. Proposed Algorithm

Initially the code of the algorithm was written using MATLAB because it provides powerful numerical computation and advanced visualization with easy to write syntax. DWT algorithm has been tested on the “lena” image file with satisfactory result. After achieving proper result, we move to HDL coding using Xilinx_ISE_Design Suite_13.1. Here, initially specification of the algorithm at the behavioral level is carried out using the HDL. After compilation, algorithm was simulated using Questasim to get the satisfactory results for real time implementation. Next, the HDL codes are synthesized using the Xilinx XST synthesis tool which will produce gate-level architecture for FPGA implementation. Finally, the design codes of DWT will be downloaded into FPGA board for verifying its functionality. However, in this paper we only present the simulation results for the DWT.

IV. Experiment and Result

4.1. Tools Used in the Design

Software tools:

Xilinx ISE_Design Suite_13.1 and MATLAB 2014 are used for this implementation. Xilinx ISE_Design Suite_13.1 is used for simulation as well as synthesis purpose. Additionally, Questasim is used for simulation and MATLAB 2014 is used to read the output.

Hardware tools:

Xilinx Virtex series FPGA XCV400 is used which has following characteristics as shown in table 1:

Characteristics	Value
LUTs	9600
Slices	4800
IOBs	170

Table 1: Characteristics of XCV400

4.2. RTL Schematic:

Figure 4. shows the RTL schematic of our proposed design.

Fig. 4. RTL Schematic

4.3. Comparative Analysis:

It is very important to compare the performance of proposed design with existing implementations to evaluate its performance or efficiency. The comparison can be done based on area utilized and its operating frequency. There are various FPGA based implementations some of which requires less area and some achieves optimum speed.

Table 3 shows the comparison of the result obtained in this proposed design with previously obtained results.

Parameters	Our Work	Reference [2]	Reference [6]	Reference [5]
Slice registers	144	1152	1152	158
Frequency of Operation	43.630 MHz	180 MHz	256 MHz	120 MHz
FPGA used	Virtex	Virtex-V	Virtex-V	Virtex-II

Table 3: Comparison of result

4.4. Simulation Results:

Figure 5. shows simulation result for lena image.

a. Input image

b. Single level decomposed image

c. Reconstructed Image

Fig. 5. Simulation Result

V.CONCLUSION

In this paper, area efficient and high speed DWT algorithm for image compression is suggested. This implementation requires only 144 slices at an operating frequency of 43.630 MHz. And from the comparison with previous work done, it is clear that proposed algorithm is better from area as well speed point of view.

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