IJCTA, 9(36), 2016, pp. 543-549

An integrated Frequency Synthesizer for Wireless Communication Applications for Improving the Performance

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Abstract : One of the leading importance's in wireless communications is to transmit multimedia data comprises of audio, video and images. The main objective is to provide a communication transceiver with low cost with smaller factor and lower power dissipation. An integrated RF functionality in low-cost CMOS technology together with the baseband transceiver function is the proposed approach for the above problem. It requires integration of the frequency synthesizer with enough isolation from supply noise to allow the synthesizer to coexist with other on-chip transceiver circuitry and still meet the phase noise performance requirements of the application. This paper suggests a differential synthesizer for block-down-convert receivers that achieve improved levels of phase noise and supply rejection performance through the use of fully differential architecture and a wide-bandwidth PLL.

Keywords : CMOS, Frequency Synthesizer, Phase Locked Loop, Signal Processing, Wireless Communication Application.

1. INTRODUCTION

Accurate synthesization on the output waveforms is necessary for all kind of communication systems. The result of the frequency synthesization should generate a waveform in a required frequency with low phase noise, low spur and tuning resolution based frequency. Also the application should be a cost effective and is the main objective of the research work. There are several disadvantages in traditional ROM based DDFS based frequency synthesization like hardware complexity, high power consumption. Methods like quarter wave symmetry, trigonometric approximations are utilized to reduce the size of ROM. But the quantization noise is familiarized and restricts the usage of these systems [9, 10].

Frequency synthesization is necessary to generate periodic signals with user required or system required frequencies and it is used as a portion of RF transceivers [1]. Fast settling time, sub-hertz based frequency solution, increased bandwidth, continuous phase switching response and low noise are done by direct digital frequency synthesizers [2]. A low power ROM-less based DDFS is proposed for frequency synthesization in terms of accumulator. Output of the phase accumulator is eliminated and a widespread phase accumulator is used to improve the resolution of the frequency. Due to various power consumption reasons, bottle neck problems ROM-less architecture [3-5] and ROM compression methods [6-8] are used in the existing studies for low-power and increased clock based frequencies.

Existing Approach

In the existing study [11] due to the need of ROM in look up table is little complex, it proposed a novel ROM-less architecture based on the approximation of Euler's Infinite series. The advantages of

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low complexity, low computational delay and increased purity. The proposed direct digital frequency synthesization method has a higher spurious free dynamic range during comparison with [1] and the value is 72.3 dBc. This approach is used as the basic building block of a communication system. During the input size increases then the necessity of ROM is increased. To overcome this issue, in this paper, a novel Integrated RF synthesizer is proposed.

Proposed Work

Analytical relationships for such a system relating output phase noise to system design parameters and internal noise sources are developed. A prototype systems embodying the design principles, and also embodying new differential circuit configurations which minimize supply coupling is designed, lay out and fabricated. The performance of the prototype synthesizer as a standalone device is evaluated. The synthesizer is embodied in a complete integrated radio system and the performance of the synthesizer in the complete radio system is also evaluated. A wide PLL bandwidth requires a comparison frequency in high level which is cooperative to the synthesis of frequencies at a wide range. Thus a wideband IF double conversion receiver which is compatible with the block down-convert receiver is included in the proposed architecture.

In the earlier methods of receiver architecture, the baseband is mixed with the received signal spectrum in two ways. Initially, the high frequency signal is mixed with the radio frequency signal which shifts the signal to a fixed intermediate frequency (IF). In order to do this, there is a need for RF synthesizer to be tuned which is smaller or equal to the standard spacing channel. The IF is mixed with the processed received signal and gets shifted to the baseband. So a good spectral purity with VCO is possible. When the reference frequency is larger than the loop bandwidth with the integer frequency division a stable loop is obtained. For eg., applications such as cellular phones, it has small value of frequency (200KHZ) as in GSM. Due to the loop bandwidth in MHz and the reference frequency which is in tens of MHz, It could not be produced by the wideband PLL based frequency synthesizer. To overcome this, our architecture is proposed with a Wideband IF Double Conversion receiver. In this method, the RF signal is mixed with the fixed RF synthesizer of intermediate frequency. Then the desired channel from the IF is tuned to the baseband by the variable frequency synthesizer at IF. By this low phase noise is achieved.

In the design technique of our proposed, integrated VCO with low noise is considered as the main block. Since the integrated VCO is too noisy and the random loop bandwidth the suppression of this noise by the wideband loop is not enough.

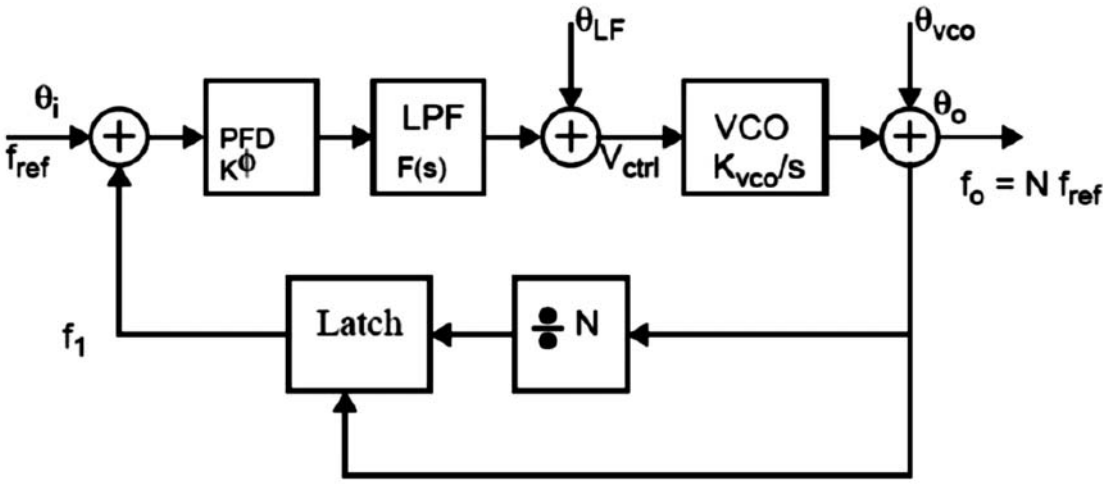

Figure 1: Linear Model of the Second Order PLL

From the above block diagram, the PFD noise and the frequency divider gets multiplied at the PLL output by the divider ratio. This divider ratio may get reduced when wideband PLL is used. There is no suppression of noise due to the wide bandwidth loop. This occurs only when the frequency over cross the

loop bandwidth limit. The divider output has the low noise latch which is clocked by the VCO such that the PLL output has no contribution from the divider noise. The noise obtained from the loop filter has a peak gain which depends on the gain of the VCO.

Low-Noise Integrated VCO Design

The tuned and untuned VCO are the basic types of Low noise Integrated VCO design. Untuned oscillator has the disadvantage of having inferior spectral purity for the same power consumption when compared to the tuned oscillator. The performance of the latter depends on the Q, quality factor of the tuned element.

On-chip Inductors

Most commonly used on chip inductor is spiral inductor which is constructed using the metal layers. This layout depends on the inductance value and their frequency of operation. The preferred spiral inductors generate less noise when compared with active inductances. Hence high performance VCO is obtained.

On-chip Varactor

Here the *p* +/*n* well junction is used as the varactor. This is more preferred due to its high quality factor. Thus the optimization of the layout needs only less attention. The minimum series resistance is achieved so the distance between *p*+ and *n*+ regions is kept at a minimum value.

Fully-Integrated VCO with Tuned Element

The oscillator in the fully integrated VCO is obtained by connecting a gain stage which may be a transistor and a bandpass filter of tuned or resonator types together. Here the preferred oscillator is Colpitts oscillator. In the oscillator circuit the positive resistance in the tank is cancelled by providing negative resistance through capacitive positive feedback.

Differentially-Controlled VCO

If the Voltage controlled Oscillator is integrated, the noise could be coupled through the substrate. For differential output, the control voltage variation or the supply leads to the variation in the effective capacitance in the tank. Hence there is a fluctuation of the control supply or voltage by the oscillation frequency.

Low-Noise Loop Filter and Phase/Frequency Detector

The low noise loop filter and the phase detector are orderly connected to generate the control voltage. The VCO control voltage is acquired from the loop filter output. The output contains the information which checks whether the VCO phase leads or lags the reference.

Loop Filter Design

The loop filter design has the charge pump based on the concept of current steering. Differential up and differential down signals from the PFD are used in order to steer the current in the differential pair in the charge group. This result in non-zero static phase error and the spurious tones are created. It is created due to ripple in the control voltage at the comparison frequency. By this the VCO frequency is modulated. The difference between the control voltages is considered as the VCO control voltage by neglecting the ripple. The steady state charge pump should have the differential output as zero even if the control voltage need to drive the VCO is large. Thus an active loop filter is used.

Low-Noise Latch

The noise in the divider chain is bypassed at the frequency divider output by the low noise latch. At RF, VCO gives the clock signal which in turn takes the output of the divider as its input. For this process the divider output should be kept ready before the arrival of the VCO clock cycle.

Frequency Divider

The frequency divider block has the prescalar and two counters in its pulse swallow architecture. The divider noise performance constraint gets relieved by the low noise latch at its output. The current should be maintained constant in order to lower the noise coupling from the injection of the substrate. This is done by the differential logic which is better than the single ended case.

2. EXPERIMENTAL DESIGN

A wireless device implemented in the proposed work has the prototype based on the wideband PLL architecture. This has been fabricated into the CMOS process of 0.35 mm 2-poly 5-metal, intended as the RF synthesizer using a wideband IF double conversion architecture. Each block has differential input and output with a differentially controlled VCO. The low-noise buffer is also differentially clocked. The hardware and the power consumption determine the plan of frequency of the frequency synthesizer. This has the major impact on the performance such as phase noise, spurious tones and power.

In general the openly available crystal oscillator 1,(below 200 MHz) has a phase noise level of -160 dB/Hz at 50 kHz offset frequency. The reference frequency needs 0.2 MHz multiples which is the channel spacing of the wireless device. If the minimum value of the frequency is 43.2 MHz, then the RF synthesizer frequency step and the IF generation frequency is 43.2MHz. To improve the performance the IF should be at least 200MHz with 1.9GHz carrier. Then the divider ratio will be 36 (*ie*. 1.6GHz/43.2MHz)The crystal oscillator phase noise and divider are amplified by N. Therefore the crystal reference frequency is chosen as 86.4MHz.Then the divider ratio is reduced from 36 to 16 with 400 MHz IF. This leads to the reduction of noise amplification, phase detector and divider to 24dB.Thus wide band PLL is implemented. The spurious tones are suppressed when the IF synthesizer uses narrow band PLL approach. This is generated by the loop.

In the oscillator 2, narrow bandwidth loop is preferred such that the phase noise and divider is suppressed by the loop filter at its output. The VCO controls the overall phase noise of the oscillator 2. This phase noise is relaxed by 12dB as the output of the VCO is divided by 4 in order to obtain the IF frequency. The oscillator 2 required tuning ranges is approximated when the RF is divided by the IF. For eg, for 80 MHz crystal reference frequency the tuning range 20%.

Loop parameter design.

To achieve overall phase noise as minimum the loop bandwidth of the wide band PLL needs to be optimized especially for offset frequency that is difficult to meet. Here in this work for maximum suppression of the VCO noise the loop bandwidth is chosen as 8MHz by maintaining the low noise at 3MHz from the reference, PFD and loop filter. The RC parameters of the loop filter can be determined by obtaining the desired loop bandwidth. The determined RC parameter of the loop filter must have enough phase margins for the loop.

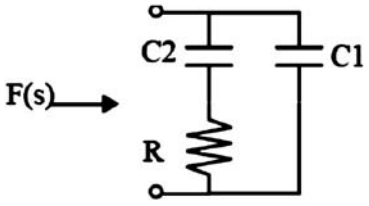

Fig. 2. Loop filter based on RC.

We know the loop gain is

$$G(s) = \frac{K_{\varphi} F(s) K_{vco}}{N_s}$$

Where F(s) is $$F(s) = \frac{1}{sC_1} + \frac{1}{\frac{1}{R} + sC_2} = \frac{1 + sR(C_1 + C_2)}{sC_1(1 + sR\,C_2)}$$

Let $$P_3 = \frac{1}{RC_2} \text{ and } Z_1 = \frac{1}{R(C_1 + C_2)}, \text{ then}$$

$$F(s) = \frac{1 + s/Z_1}{sC_1(1 + s/P_3)} \text{ and}$$

$$G(s) = K_{\varphi} \cdot \frac{1 + sZ_1}{sC_1(1 + s/P_3)} \frac{K_{vco}}{N_s}$$

The value of R, C_1, C_2 are selected in such a way that G(s) has enough phase margin. The value of oscillator 1 has the value of R is 20kw, and for C_1 and C_2 are given the value of 0.2pF and 8pF respectively. The phase margin is taken as 75 degree. Similarly for oscillator 2 the loop the value of R is 40kw, the value of C_1 is 10pF and the value of C_2 is 400pF with bandwidth chosen as 40 KHz.

VCO Design

The PLL will only be fully differential if the VCO is differentially controlled. The power supply rejection ratio is improved by using cascade current source. To reduce the 1/f noise PMOS device with 1μm channel length are used. To maximize the frequency control range, the output common mode level is set to the midpoint between the Vdd and GND. It is done by choosing the appropriate ratio of the current and the size of the cross coupled NMOS devices. In a common mode feedback circuit in the loop filter sets the control voltage to be the same as the level of the VCO outputs. Hence the differential-mode signal of the control voltage has the largest effective control range.

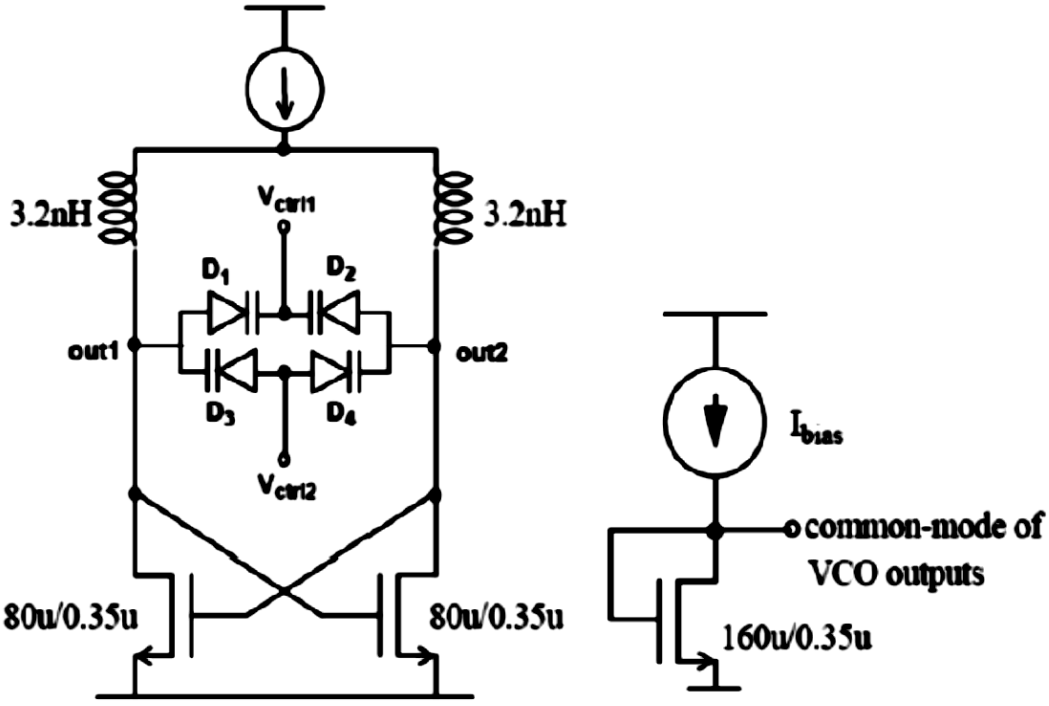

Figure 4: Circuit Diagram of a differentially controlled VCO with differential outputs

3. SIMULATION RESULTS

The entire PLL simulation results are obtained from HSPICE are shown in Figure-5. The initial spectrum indicates the spurious tone is -55dBc at multiples of 86.4MHz away from the carrier frequency. When a

200 mV peak to peak sine wave at 5.4 MHz is applied to the power supply of the PLL, a tom of -35 dBc appears at 5.4 MHz away from carrier, which is shown in the second spectrum. The third spectrum is the difference of the UP and down signals at the PFD results. This is the constant phase error of the proposed PLL. A -80dB tone at DC translates a constant phase error of 0.001 degree.

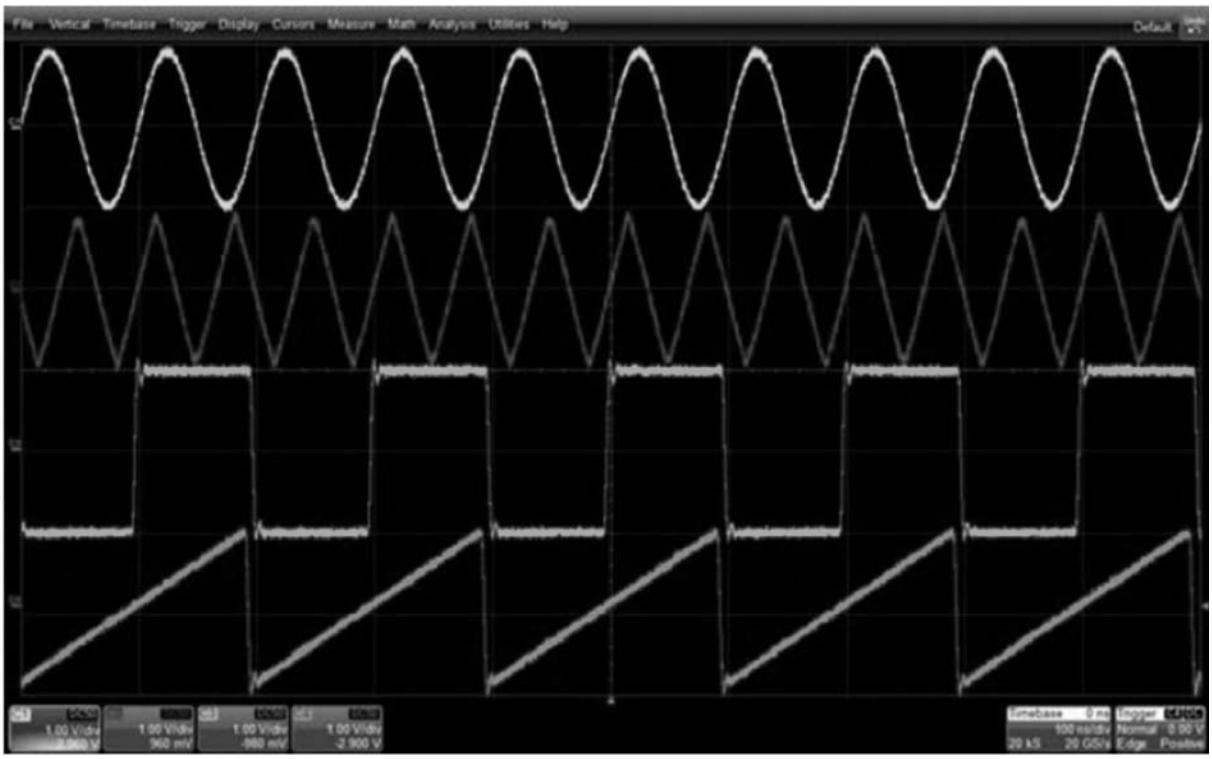

Figure 5: Frequency Synthesization using HSPICE

4. CONCLUSION

In this paper the basic restrictions on high-performance based frequency synthesization specifications are examined with a new wide bandwidth PLL based FS architecture is proposed. This paper concentrates on improving the performance, to do this it concentrates on the sub levels of the circuit design individually. They are, minimizing the phase noise are eliminated, spurious tones are explored, wide-bandwidth PLL is used, RF integrated based frequency synthesizer is selected and loop filter is amplified by the VCO gain. Since the entire design of the PLL circuit is selected as an integrated circuit the efficiency of the proposed design is high than the existing approaches.

5. REFERENCES

1. M. Kesoulis, D. Soudris, C. Koukourlis and A.Thanailakis, 'Systematic methodology for designing low power direct digital frequency synthesizers', lET Circuits Devices Syst., 4, p.293 (2007).
2. Estimation of Spectrum in Mobility based on Time Series Models “,International Conference on Recent Innovations in Engineering & Technology, ICRIET, BANGALORE.
3. J. Vankka and K. Halonen, Direct Digital Synthesizers: Theory, Design and Applications. Boston, MA: Kluwer, 2001.
4. Li Jincheng, Yang Huazhong “A New Architecture of Twiddle Factor Generator for Radix-2 1024-Point FFT” Chinese Journal of semiconductors vol. 25, Apr. 2004, pp.377-382.
5. Challenges and Surveys in Key Management and Authentication Scheme for Wireless Sensor Networks“ in Abstract of Emerging Trends in Scientific Research 2014– 2015. https://ideas.repec.org/s/pkp/abetsr.html
6. K.I.Palomaki and J.Niittylahti “A low-power, memory less direct digital frequency synthesizer architecture” ISCAS’03, ppII77-II80.

7. Cluster based Key Management Authentication in Wireless Bio Sensor Network “, ,International Journal of pharma and bio sciences.
8. J. M. P. Langlois, and D. Al-Khalili, “A low power direc digital frequency synthesizers in 0.18- μm CMOS”, IEEE CICC’03 pp283-286.
9. Security in Wireless Sensor Networks: Key Management Module in EECBKM”Presented in International Conference on World Congress on Computing and Communication Technologies on Feb 27- & 28 and 1st march 2014, on St.Joseph college,Trichy.
10. J.Vankka, ’Methods of mapping from phase to sine amplitude in direct digital frequency synthesis’, IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol 44,no.2,pp.526-534,(1997)March.
11. U.Dinesh, Aravind Ram.S, M.Hariharan, K.Hariharan, “A Novel Rom-less Direct Digital Frequency Synthesizer based on Euler Infinite Series”, IJSCE, Volume-3, Issue-2, May 2013.