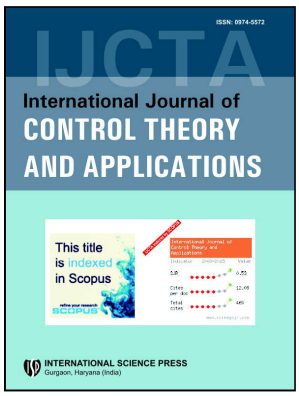

International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 10 • Number 6 • 2017

Comparative analysis of self checking and monotonic logic Techniques for combinational circuit testing

Namita Arya[1], Amit Prakash Singh[2] and Bhavika[3]

[1] University School of Information and Communication Technology Guru Gobind Singh Indrprastha University Dwarka, 16C, New Delhi, India, Email: aryanamita12@gmail.com
[2] University School of Information and Communication Technology Guru Gobind Singh Indrprastha University Dwarka, 16C ,New Delhi, India , Email: amit@ipu.ac.in
[3] University School of Information and Communication Technology Guru Gobind Singh Indrprastha University Dwarka, 16C, New Delhi, India, Email: amit@ipu.ac.in

Abstract: Today VLSI world permits the fabrication in huge integrated circuit area with empowerments of designs and attractive features. However, fabricating errors and failures take place due to inadequacy with the manufacturing steps. It is a major challenge to justify simultaneously both, the growth and the application of advanced techniques to fabricate integrated circuit at fabrication level. Strengthening methods are focused on building an error-free circuit and using different methods to manufacture a fault tolerant circuit. They are proposing several redundancy methods at fabrication level and enhancing the overall performance of the circuit. An efficient manufacturing has motivated the work present here with some methods of fault detection and avoidance techniques via monotonic logic and self-checking the logic of defect-detection.and self checking logic of defect-detection.

Keywords: Test circuits, Fault Detection Techniques, Monotonic logic, Self-checking circuits.

1. INTRODUCTION

The VLSI process has a very important feature to evaluate the fault failure cause in any chip. It is very difficult to decide the reason of its failure. The very initial process is to evaluate fault detection in between the fabrication of the circuit. Moreover error detection reduces the efficient area of the VLSI chip. Fault categorization defines the type of fault on the fault levels in the system. There are different methods introduced for the fault diagnosis in circuits.

Constantinescu C, Member S. surveyed that transient & intermittent errors have an efficient effect on dependability in [1].Dependability may be reduced by effect of burst of faults even when the circuit is fault tolerant. This paper introduced recovery techniques towards burst of faults. In [2], fault Simulation introduced a bridging error model using stuck-at fault logic. This paper proposed a unique technique for fault detection by fault sampling. Almukhaizim S, Drineas P, Makris Y. Introduces a non-intrusive concurrent error detection technique for whole digital circuit in [3].In [4], a fault diagnosis is proposed in stuck-at faults using Boolean logic gate in various types of circumstances. This paper also proposes a parallel bus lines concept for fault

tolerant circuit. In [5] a method is propounded as the output remains same after multiple measurements with the use of cascaded digital circuits to prepare a fault tolerant circuit. In this paper both stuck at fault and self checking technique is used with the help of the Modelsim simulator.

2. PROPOSED ALGORITHM

2.1. Defect Detection

The benchmark needs a circuit without any single type of error. Fault tolerance is all about redundancy, improvements and error diagnosis. The redundancy technique speaks about the reproduction of components by Fault detection.

There are many reasons for validation and verification of a circuit.

- Validation assured system correctness and development.
- Verification assured that the arrangement of the whole circuit fulfills its requirements.

The main object of both validation and verification is to determine faults. Error evaluation is one of the leading research topics of VLSI circuit theory. One of the major difficulties in this area is the evaluation of error-diagnosis tests for digital circuits.

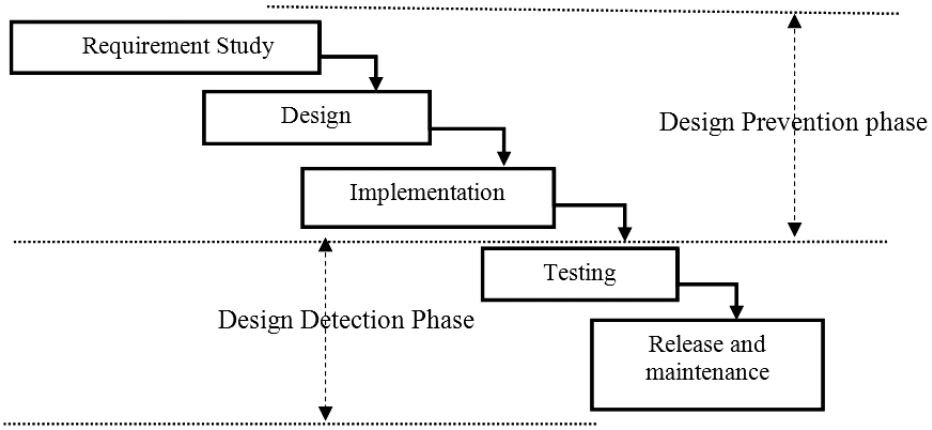

Figure 1: Circuit design process

2.2. Defect Detection Techniques

Here are four proposed techniques for detection and location of faults present in a circuit.

A. Self-checking circuit technique.
B. Monotonic logic technique

2.2.1. Self-Checking circuit technique

A circuit is called monotonic circuit if it executes a monotonic operation. A monotonic increment of a function remains the same when the input value rises.

Suppose we have a circuit which is implemented by the output of the circuit. It would be like Fig 2.

Suppose there is a single stuck at fault 0/1 error at the C, output of the circuit X .There may be chances of faults at the output f because the C is faulty input for circuit Y. Now z would propagate the fault from C to total circuit output f. This is also a fault detection technique by monotonic logic. The best part of this technique is that the fault can be avoided by re-implementing the circuit using another approach.

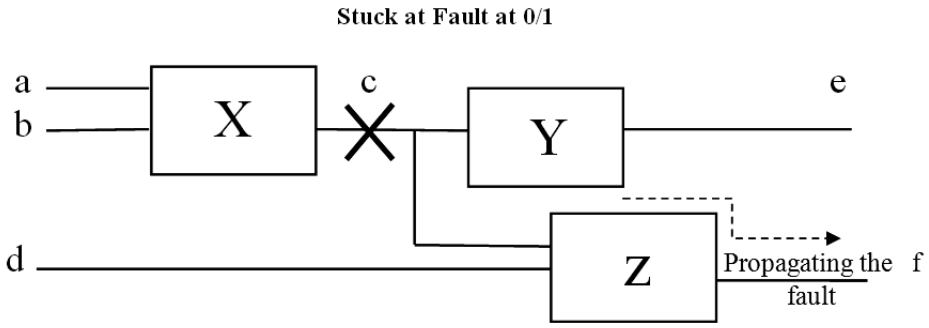

Figure 2: Monotonic logic circuit at stuck at fault

2.2.2. Re-implementation of monotonic logic circuit

Re-implementation of the circuit introduced a new circuit part H which is an extra circuit for inputs **a** and **b.** Therefore the signal **c** cannot propagate its error. That is the best way to avoid the fault by this technique. This technique is done in half adder circuit with stuck at fault error. There is the fault at the one output and fault is propagating through another circuit therefore other output also found faulty. In this case LEDs cannot blink due to the fault in the circuit.

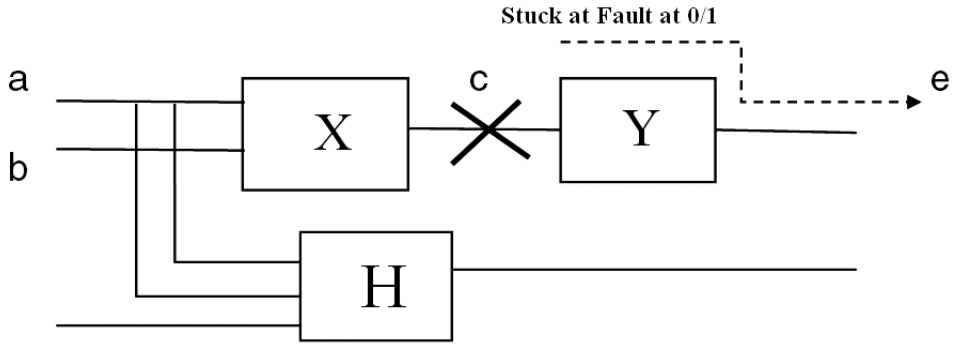

Figure 3: Re-implemented circuit without fault

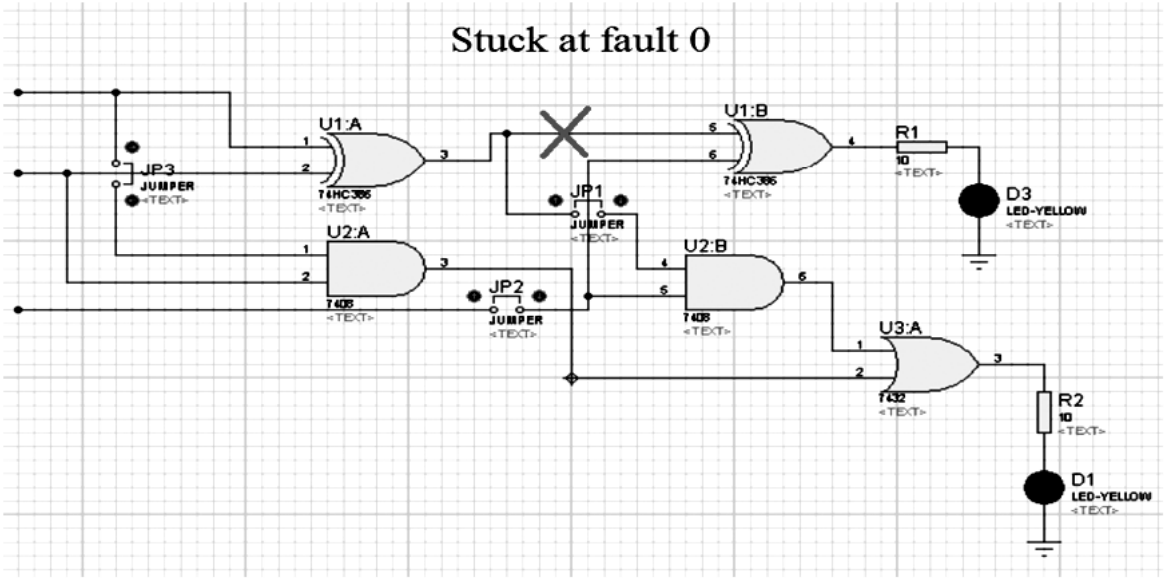

Figure 4: Monotonic logic half adder circuit at stuck at fault

LEDs blink because of fault free circuitry in figure 5

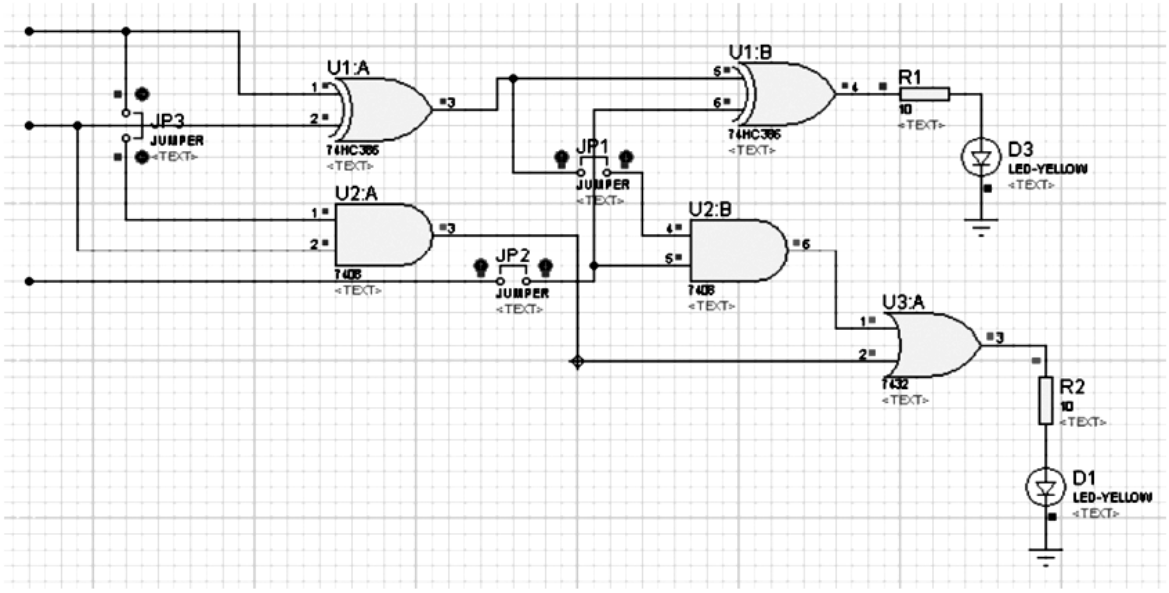

Figure 5: Monotonic logic half adder circuit without error

2.2.3. Re-implemented

Previous example can be re-implemented by adding a new component which is associated directly to original inputs. It will not propagate any fault even if fault is present in any other component.

This technique of fault avoidance can avoid at least one fault in the circuit and the remaining circuit can work properly.

In this figure 6 one LED D1 is not working due to fault present in the circuit but LED D2 is blinking because the fault is not propagating through the circuit.

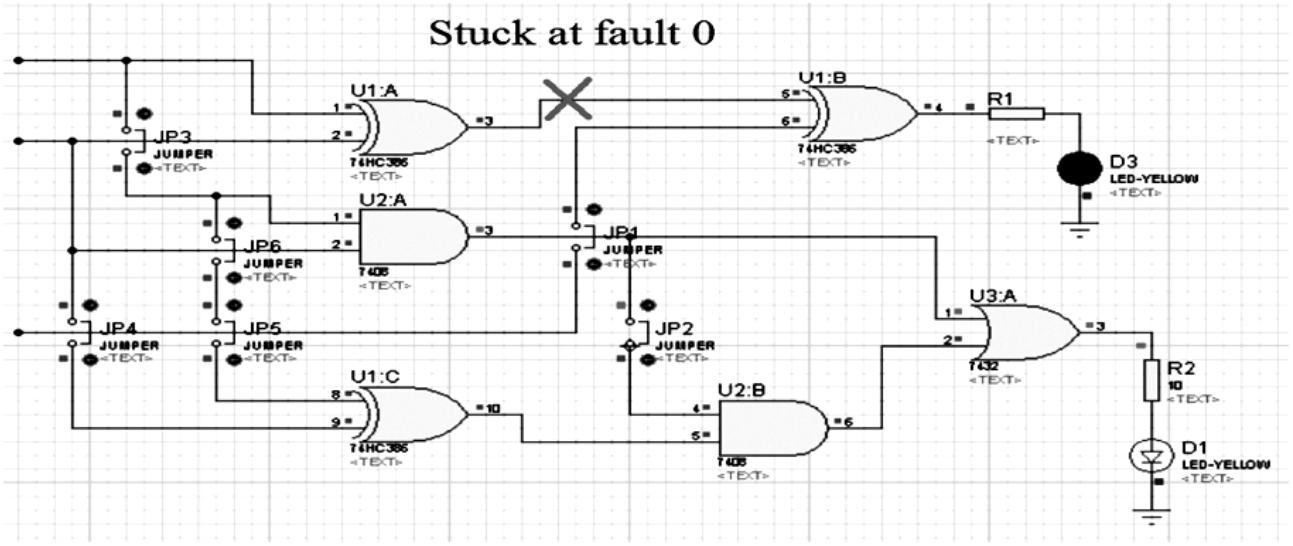

Figure 6: Monotonic logic half adder re-implemented circuit

2.3. Self-checking circuits

A Self checking circuit is an approach that promptly detects error by comparing input of circuit to the output of reverse circuit. Consider there is a circuit H whose input is X and output is Z. Another circuit present here is H^{-1} which is inverse of the previous circuit H. It is confirmed if Z is the input of the circuit H^{-1}, the output would be X only.

Meanwhile if it happens definitely circuit is fault free otherwise there may be a fault. This technique is called self checking fault detection technique.

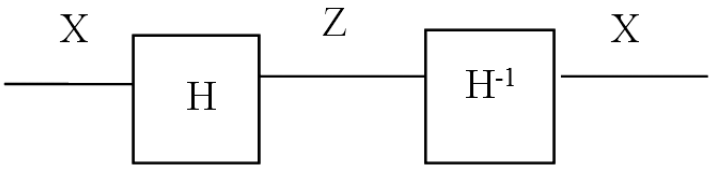

Figure 7: Time redundancy block diagram

Half adder circuit can executed also by the self checking circuit verification using inverse abstraction.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2.3.1. The Inverse Figure Of Half Adder Circuit Would Be

S	C	A	B
0	0	0	0
0	1	1	1
1	0	X	X
1	1	X	X

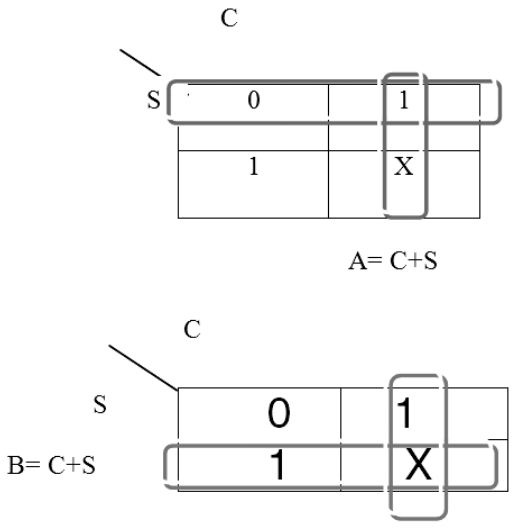

Figure 8: Inverse table for half adder circuit

A and B are the same inputs of half adder as the outputs of the inverse half adder circuit so the circuit is fault free. In fig 10 LEDs D1 and D2 showing the fault free condition by blinking.

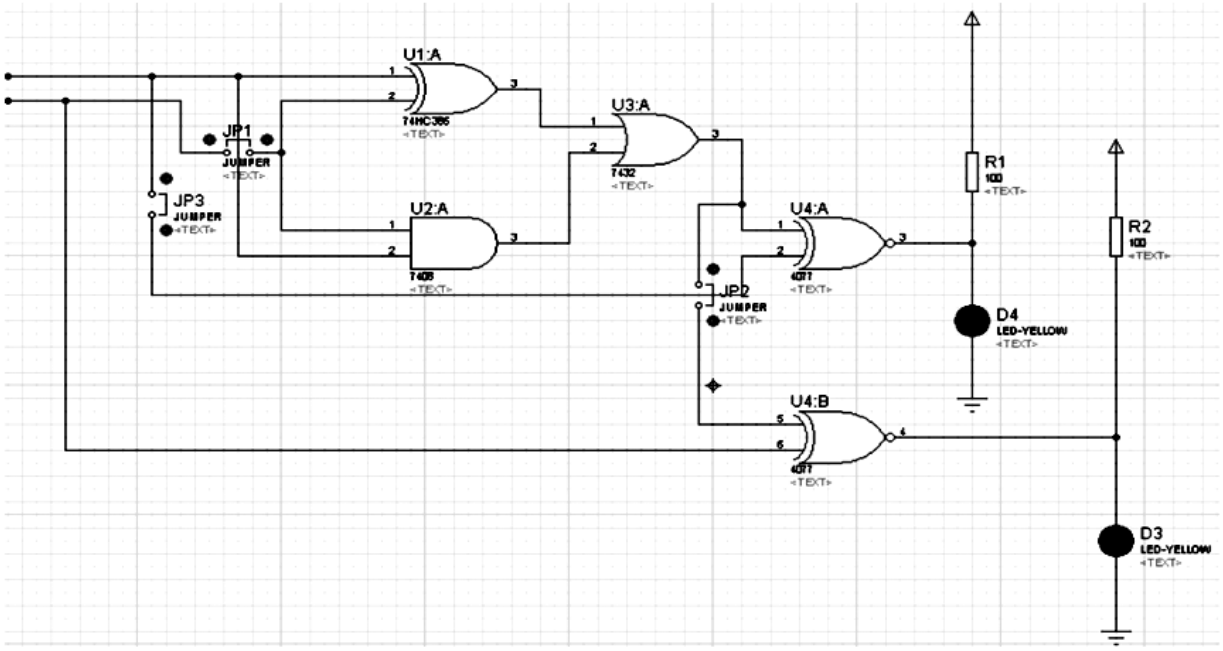

Figure 9: LEDs are in off condition

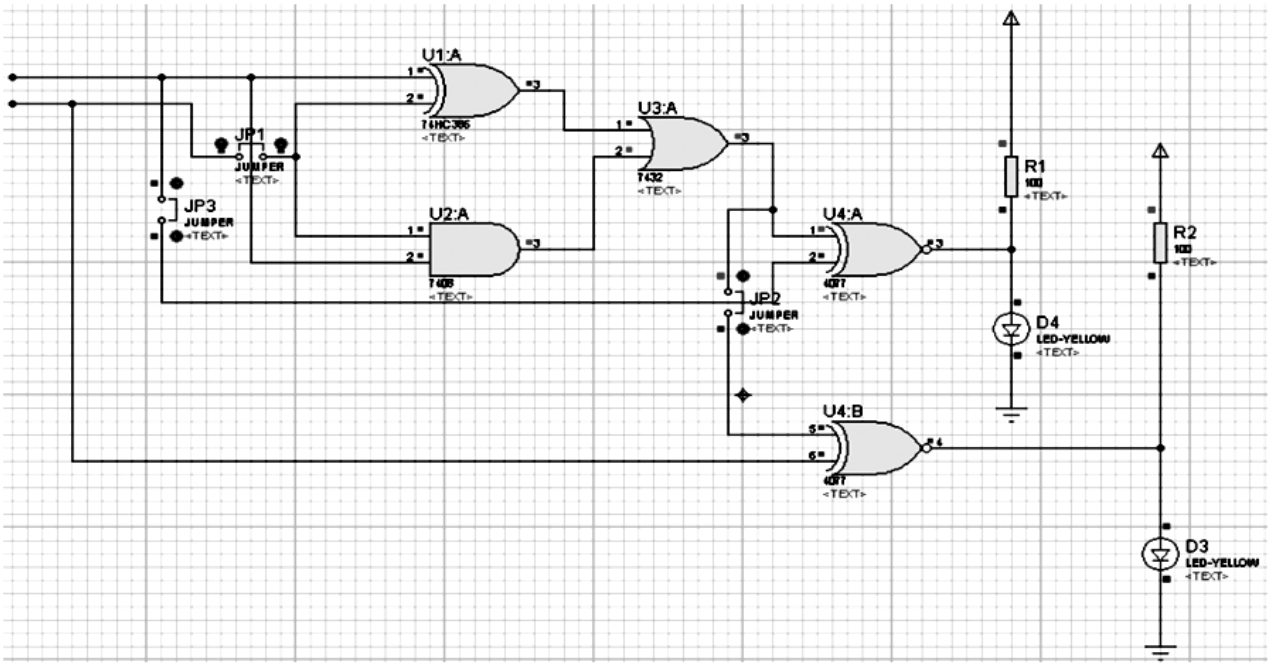

Figure 10: The circuit is fault free because LEDs are in on condition.

3. RESULT AND DISCUSSION

Table 1
Comparison Matrix of Fault Detection Methods

Method	*Speed of detection*	*Area and Cost*	*Delay*	*Power Consumption*	*Coverage*
Self-checking circuits.	Medium-Depend upon the circuit complexity	Medium-depends upon the logic gate requiredCost-less	Less- inputs and out puts would be same	Medium- depends upon the logic gate required	Medium-Not practical for all type of functionality
Monotonic logic.	Fast-As per the gate delay	Small- depends upon the circuitCost- very less	Medium- Depends upon the circuit complexity	Medium- Depends upon the circuit complexity	Good-multiple faults are avoided

From the results, different types of errors could be categorized and positioned on the circuit with strong fidelity. This shows that the suggested methods are capable to provide satisfactory precision in both of the fault categorization, and fault evaluation.

4. CONCLUSION

This paper reassessments and examines the different techniques used for detecting errors in combinational digital circuits. VLSI permits us to integrate maximum circuitry in compact and more trust worthy collection. Fault detection and fault location can now be contributed inside the IC level. VLSI performs the feasibility for enhancing the design performance of fault tolerant systems by using some class of techniques all through the system.

REFERENCES

[1] Constantinescu C, Member S. Dependability Evaluation of a Fault-Tolerant Processor by gspn modeling, ieee transactions on reliability, vol. 53, no. 3, september 2005 dependability2005;53(3):468-474.

[2] F. M. Gonçalves, Marcelino B. Santos, Isabel Teixeira, João Paulo Teixeira, "Self-Checking and Fault Tolerance Quality Assessment Using Fault Sampling," Proceedings of the 17th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems,pp.216-224,2002.

[3] Almukhaizim S, Drineas P, Makris Y. Compaction-based concurrent error detection for digital circuits. *Microelectronics Journal*",pp. 856-862,03.09.2005

[4] Palaka S, Rao KS. Fault Tolerant Logic Design For Multiple Faults In Combinational Circuits. International Journal of Engineering Research and Applications (IJERA). 2012;2(4):1237-1242.

[5] Engg I, Nagar a. Development research vlsi based self healing solution for fault tolerant digital circuits, ISSN: 2230-9926,International Journal of Development Research Vol. 5, Issue, 11, pp. 5947-5951, November, 2015

[6] R. H. Khade and d. S. Chaudhari, "a review of methodologies for testing and locating faults in integrated circuits," vol. 3, no. 6, pp. 239–241, 2014.

[7] A. K. Jameil, "a new single stuck fault detection algorithm for digital circuits," vol. 3, no. 1, pp. 1050–1056, 2015.

[8] P. R. H. Khade and S. Gourkar, "Fault Testing of CMOS Integrated Circuits Using Signature Analysis Method," vol. 2, no. 5, pp. 73–82, 2013.

[9] E. Engineering and S. Exchange, "digital logic - Error-Detection Circuit — How does this work/ ? - Electrica ... minute/ : Error-Detection Circuit — How does this work/ ?," pp. 12–13, 2016.

[10] S. M. Thamarai, K. Kuppusamy, and T. Meyyappan, "Fault Detection and Test Minimization Methods for Combinational Circuits - A Survey," vol. 2, pp. 140–146, 2011.