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Selective Harmonic Mitigation Pulse Width Modulation for Transistor Clamped Multilevel Inverters

A. Sahaya Ponrekha[1], A. Shashidhar[2] and M. Venkatesh[3]

ABSTRACT

In medium voltage high power applications, the switching frequency of the power converters are restricted to reduce the switching power losses which results in the distorted output. Hence, this paper aims to apply Selective Harmonic Mitigation Pulse Width Modulation (SHM PWM) technique for transistor clamped multilevel inverters. SHM PWM method limits the harmonic distortion in the output to satisfy grid codes requirement, even with low switching frequency. In addition to this, the transistor clamped topology is having less number of controlled power transistors, which reduces the semiconductors, cost and also simplifies the control circuit. The comparison of SHMPWM method and the conventional SHEPWM method(Selective Harmonic Elimination Pulse Width Modulation method) is also shown for five and eleven level inverter to know the effectiveness of SHMPWM method. From the results, it is clearly depicted that SHMPWM method reduces harmonics distortion effectively when compared to SHEPWM method.

Key words: THD, SHEPWM, SHMPWM, Multilevel inverter

1. INTRODUCTION

In recent years, to maintain the power quality, the power converters should have the output voltage with low harmonic distortion. Multilevel inverters became popular for its reduction in harmonic distortion. Now different topologies of multilevel inverter are used with different PWM techniques to reduce the harmonic distortions. Those different topologies are diode clamped inverter, flying capacitor clamped inverter, cascaded h-bridge inverter and transistor clamped inverter. [15], [16], [17].

The main disadvantage of multilevel inverter is the requirement of a large number of controlled switches which makes the firing circuit to be bulky and it has more switching losses. Hence, the transistor clamped inverter [10] is chosen as a good option by considering the necessity of limited number of switches.

The various PWM techniques used for multilevel inverters are sine PWM, space vector PWM and Harmonic injection PWM[1],[2]. The most commonly used PWM techniques are sinusoidal PWM and space vector PWM[3]. The limitation of these two methods is higher switching frequency. To overcome this limitation Programmed Pulse Width Modulation techniques are preferred.

Two different programmed pulse width modulations are Selective harmonic elimination pulse width modulation (SHEPWM)[4], [5], [6], [7] and Selective harmonic mitigation pulse width modulation(SHMPWM) [8], [9], [11], [12], [13], [14]. Conventional selective harmonic elimination method completely eliminates a few selected lower order harmonics. But the SHMPWM method mitigates more number of selected lower order harmonics below the maximum allowable limits given by grid codes standards.

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Till now SHMPWM method is implemented for cascaded H bridge multilevel inverter [8], [9], [11] and diode clamped inverter which is having more number of power transistors[12],[13],[14]. This paper proposes the SHMPWM method for transistor clamped multilevel inverter and its benefits are shown by comparing with the conventional SHEPWM method.

2. FIVE LEVEL TRANSISTOR CLAMPED MULTILEVEL INVERTER

2.1. Structure of five level transistor clamped multilevel inverter

The figure1 shows the structure of the transistor clamped five level inverter. It produces five output levels Vdc, Vdc/2, 0, -Vdc/2,and -Vdc. The output is taken across the two legs of the inverter. S1, S2, S3, S4 and S5 represent the power switches [10]. Thus five level transistor clamped inverter involves five power transistors only, where as conventional five level cascaded H bridge and diode clamped inverter involves eight power transistors. So it is understood that the number of power transistors are reduced more than 50% in transistor clamped multilevel inverters.

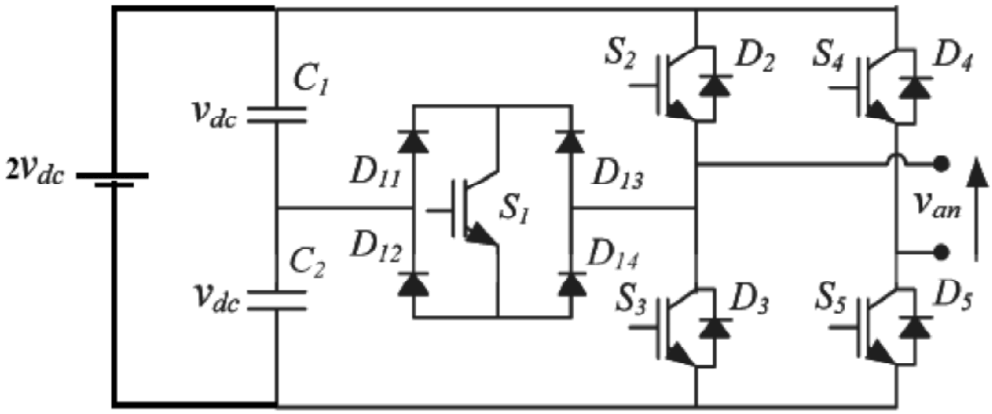

Figure 1: Five level transistor clamped inverter

The table 1 shows the switching states of the five level transistor clamped inverter for each level of output voltage.

Table 1
Switching states of five level transistor clamped inverter

S1	*S2*	*S3*	*S4*	*S5*	*Van*
0	1	0	0	1	2Vdc
1	0	0	0	1	Vdc
0	0 or 1	1or 0	0 or 1	1 or 0	0
1	0	0	1	0	-Vdc
0	0	1	1	0	-2Vdc

2.2. SHEPWM for five level inverter

In SHEPWM method to eliminate the selected lower order harmonics and to control the fundamental component, equations of the harmonic components are derived using fourier series analysis. For deriving these equations, the output voltage waveforms of the multilevel inverters has to be predefined. The figure2 shows the predefined switching pattern for five level inverter. The equation1 gives the fourier series expansion of predefined output voltage waveform of five level inverter. The Predefined waveform is having odd-quarter wave symmetry and hence all the even harmonics are zero.

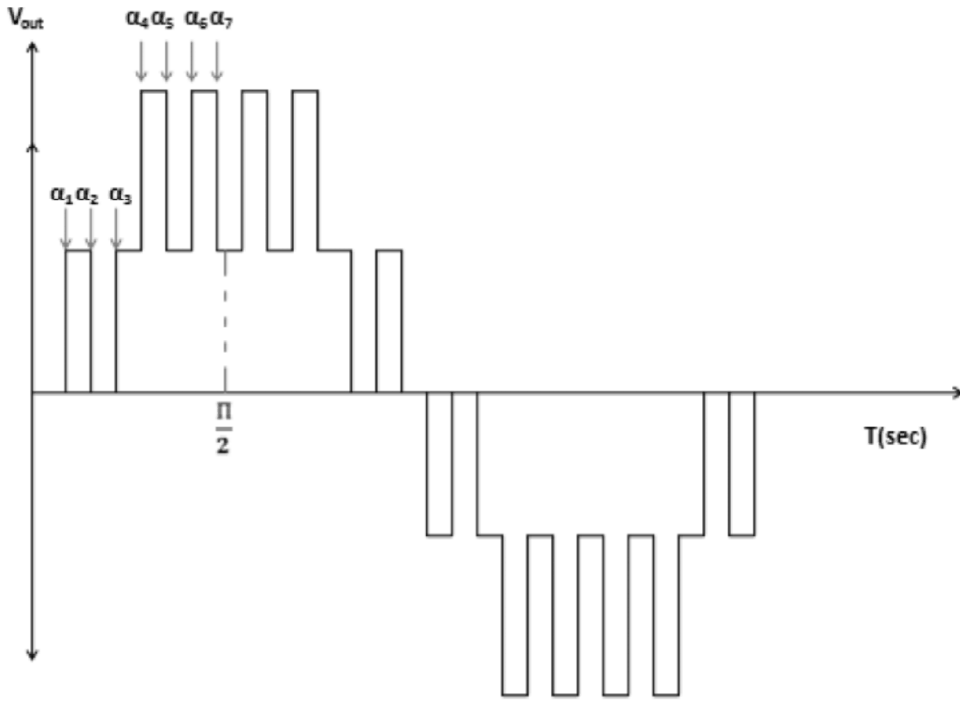

Figure 2: Predefined switching pattern of five level inverter

$$V_{out} = \sum_{n=1,3,5...}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) - \cos(n\alpha_5) + \cos(n\alpha_6) - \cos(n\alpha_7))\sin(nwt) \quad (1)$$

$$h_n = \frac{4V_{dc}}{n\pi}(\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) - \cos(n\alpha_5) + \cos(n\alpha_6) - \cos(n\alpha_7))$$

h_n is nth harmonic content

'n' is the harmonic order

V_{dc} is the voltage across each capacitor.

α_n are the switching angles

$$\alpha_1 < \alpha_2 < \alpha_3 ..... < \alpha_n < \frac{\Pi}{2}$$

The equations (2) and (3) are the nonlinear equations for the SHEPWM of five level inverter. In the equation(2), the fundamental component is equated to desired value by assuming a modulation index. The equations(3) having lower order harmonics are equated to zero. To solve these equations, Newton Raphson's iterative method is used. Newton Raphson's iterative method cannot be evaluated without the usage of initial values of the unknown parameter. Here the switching angles are the unknown parameters. The initial switching angles are found by converting the equations into Cauchy problem, which uses least square mean approximation method. These initial values are then passed into Newton Raphson's iterative method and finally, the accurate switching angles are obtained[5].

$$\frac{4}{\pi}[\cos(\propto_1)-\cos(\propto_2)+\cos(\propto_3)+\cos(\propto_4)-\cos(\propto_5)+\cos(\propto_6)-\cos(\propto_7)] = sM \quad (2)$$

Where s = $\frac{number\ of\ levels}{2}$ which should be a whole number, for five level inverter s = 2.

M = $\frac{h1}{sVdc}$ is the modulation index , h_1-Fundamental component of the output voltage

$$H_n = \frac{4}{n\Pi}[\cos(n \propto_1)-\cos(n \propto_2)+\cos(n \propto_3)+\cos(n \propto_4)-\cos(n \propto_5)+\cos(n \propto_6)-\cos(n \propto_7)] = 0 \quad (3)$$

$$n = 3, 5, 7, 9, 11, 13, 15$$

With the estimated switching angles, the controlled power transistors of the inverter are switched in the given order. By this way the fundamental harmonic content of output voltage is set to expected value and the harmonics up to 15 are completely eliminated. The figure3 shows the output voltage of five level transistor clamped inverter with SHEPWM technique. The parameters used for the simulation of five level inverter is shown in the table 2.

Table 2
Parameters used for the simulation of five level inverter

Parameters	*Values*
Voltage across capacitor(Vdc)	100 V
Switching Frequency of S1	700 Hz
Switching Frequency of S2	200 Hz
Switching Frequency of S3	550 Hz
Switching Frequency of S4	150 Hz
Switching Frequency of S5	150 Hz
Output Voltage Frequency	50 Hz

The figure 4 shows the frequency spectrum of the output voltage waveform of 5level transistor clamped inverter with SHEPWM. From the figure 4, it is known that the THD up to 40th harmonic is 32.09% and harmonics upto 15 are eliminated, from the output voltage as expected.

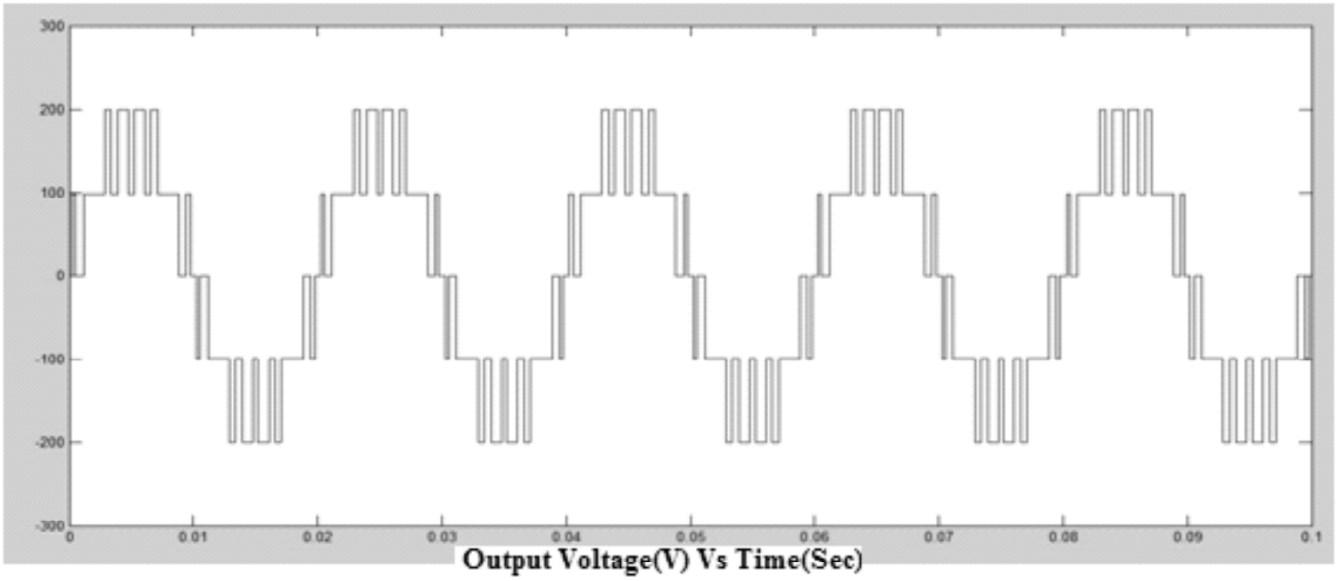

Figure 3: Output voltage of five level transistor clamped inverter with SHEPWM technique

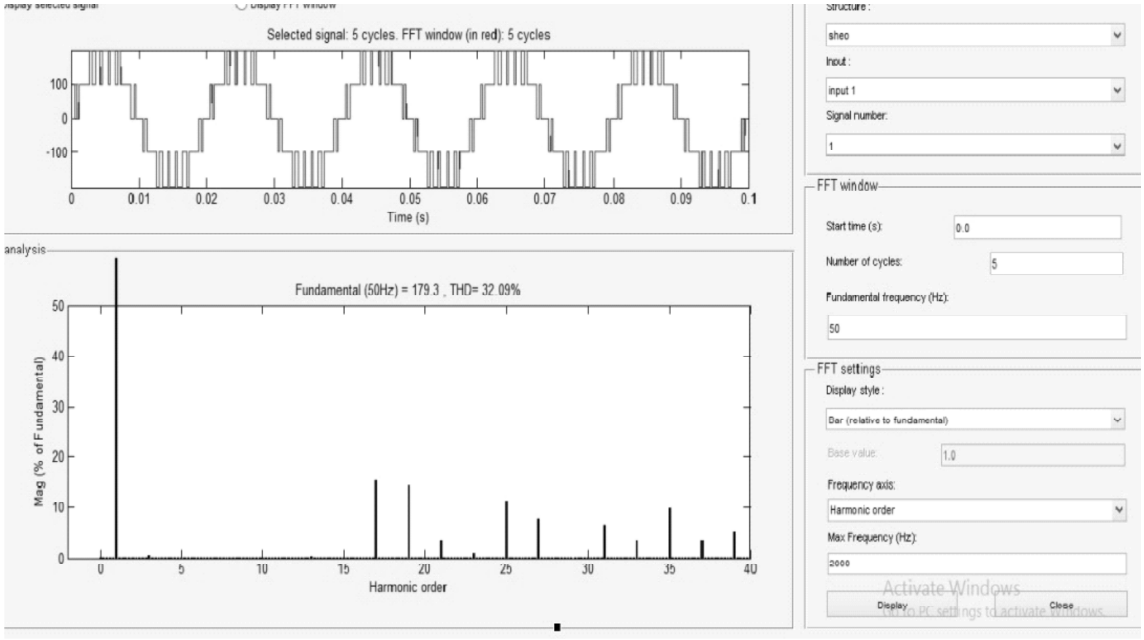

Figure 4: Frequency spectrum of the output voltage waveform of 5level transistor clamped inverter with SHEPWM

2.3. SHMPWM for five level inverter

In SHMPWM technique, more harmonics are mitigated below the limited values for same switching frequency, while compared with the SHEPWM. Those limited values are defined by the grid codes, which gives the maximum allowable limits for each harmonic order and THD to maintain the grid's quality. Here the EN 50160, CIGRE WG 36-05 are the two grid codes referred for SHMPWM[17], [18]. The grid code requirements are shown in the table 3.Using the same waveform shown in figure 2, the equations of SHMPWM technique for the five level inverter are written. The SHMPWM technique is based on solving the following inequality equations (4) and (5), where L_n is the maximum allowed level of nth harmonic imposed by the applied grid code. The challenge in SHMPWM is to solve the inequality equations. By writing a program in Optimisation tool of MATLAB, those equations are solved. By solving the equations the exact switching angles are obtained.

$$| sM - H_1 | \leq L_1, \text{ where } H_1 = \frac{4}{\pi}[\cos(\propto_1)-\cos(\propto_2)+\cos(\propto_3)+\cos(\propto_4)-\cos(\propto_5)+\cos(\propto_6)-\cos(\propto_7)]$$

and

$$M = \frac{h1}{sVdc} \tag{4}$$

s = 2 for five level inverer

$$Hn = \frac{4}{n\Pi}[\cos(n \propto_1)-\cos(n \propto_2)+\cos(n \propto_3) + \cos(n \propto_4)-\cosn(\propto_5)+\cos(n\propto_6)-\cos(n\propto_7)] \leq H_1 L_n \tag{5}$$

n = 5, 7, 11, 13, 17, 19, 23, 25, 29,31, 35.

The controlled power transistors are switched using the pre calculated switching angles. Figure 5 shows the output voltage of five level inverter with SHMPWM technique. Using the FFT analysis ,the frequency spectrum of the output voltage is obtained as shown in figure 6. Even though harmonics up to 35 are tried to be mitigated, it is clearly known from the figure 6 few harmonics are beyond the limited values, the THD upto 40th harmonic is 19.02% which is less compared to the result of SHEPWM method (32.09%).

Table 3
Grid code requirements of EN 50160, CIGRE WG 36-05

Odd non-triplen harmonics		*Odd tripplen harmonics*	
Harmonic order(n)	*Relative voltage(L_n)*	*Harmonic order(n)*	*Relative voltage(L_n)*
5	6%	3	5%
7	5%	9	1.5%
11	3%	15	0.5%
13	2%	21	0.5%
17	1.5%	>21	0.2%
19	1.5%		
23	1.5%		
>25	0.2+(32.5/n)		
THD up to 40th harmonics <=8%			

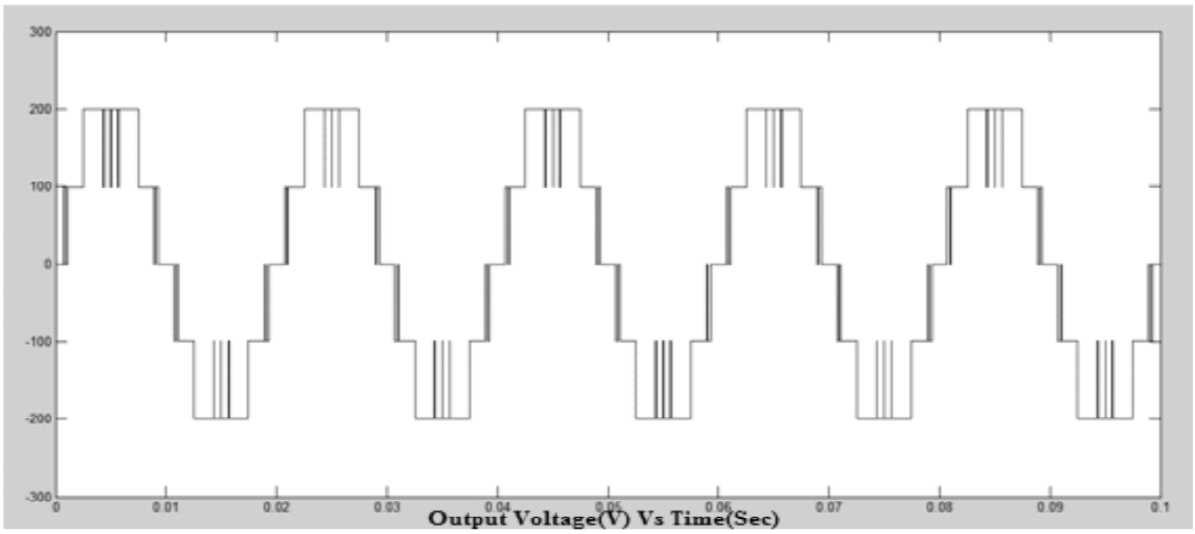

Figure 5: Output voltage of five level inverter with SHMPWM technique

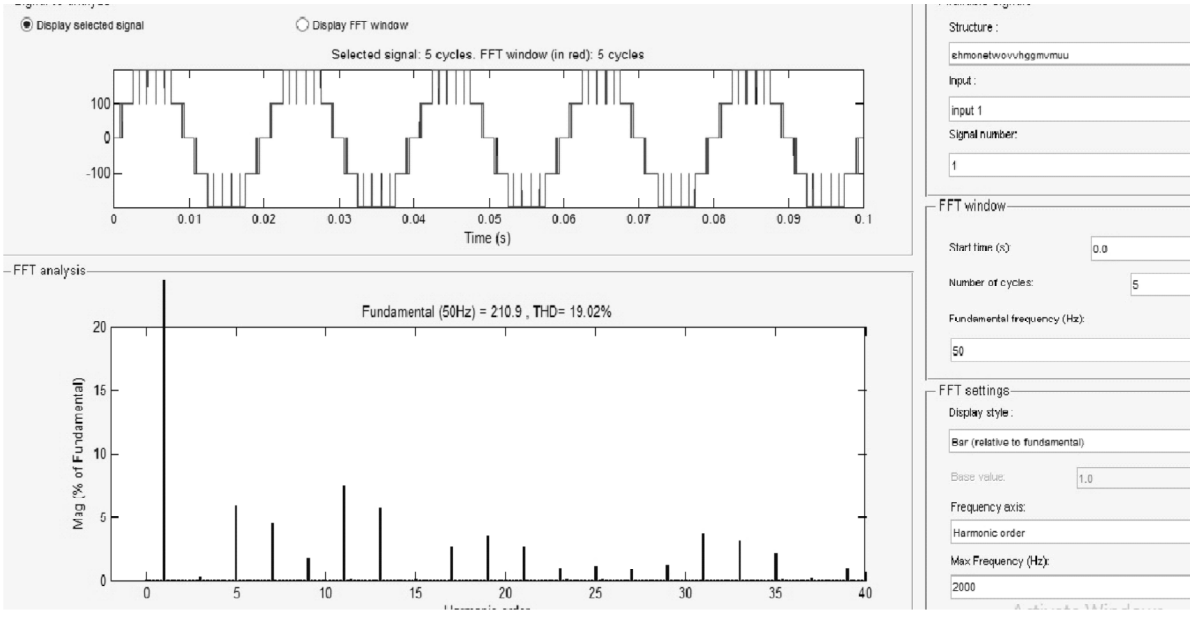

Figure 6: Frequency spectrum of Output voltage of five level inverter with SHMPWM technique

3. ELEVEN LEVEL TRANSISTOR CLAMPED MULTILEVEL INVERTER

3.1. Structure of eleven level transistor clamped multilevel inverter

The topology of eleven level transistor clamped multilevel inverter is shown in the figure 7.Eleven level transistor clamped inverter involves 8 power transistors only, where as conventional H bridge eleven level inverter involves 20 transistors [8]. The table 4 shows the switching states of the eleven level transistor clamped inverter.

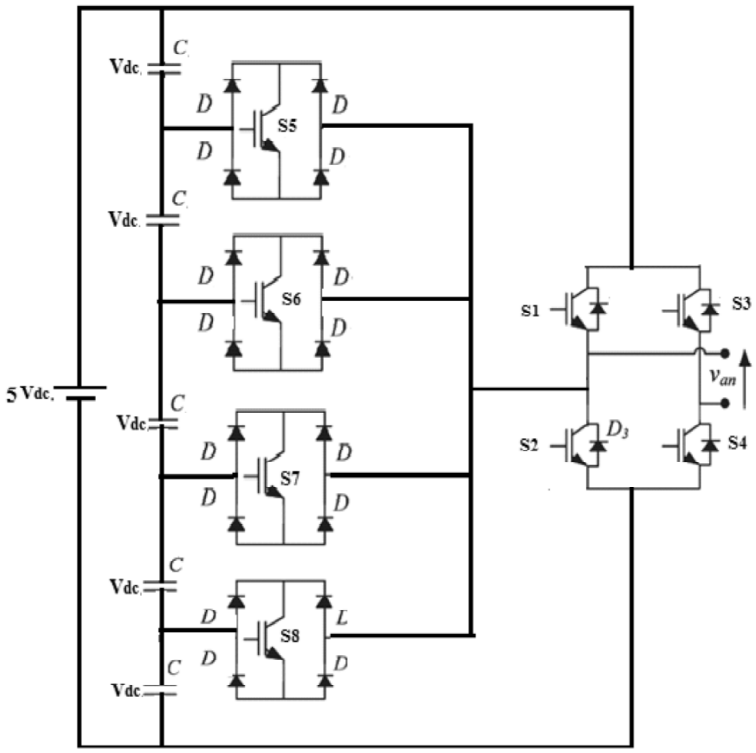

Figure 7: Topology of eleven level transistor clamped inverter

Table 4
Switching states of the eleven level transistor clamped inverter

S1	*S2*	*S3*	*S4*	*S5S*	*S6*	*S7*	*S8*	*Van*
1	0	0	1	0	0	0	0	5Vdc
0	0	0	1	1	0	0	0	4Vdc
0	0	0	1	0	1	0	0	$3V_{dc}$
0	0	0	1	0	0	1	0	2Vdc
0	0	0	1	0	0	0	1	Vdc
0 or 1	1or 0	0or1	1or0	0	0	0	0	0
0	0	1	0	0	0	0	1	-Vdc
0	0	1	0	0	0	1	0	-2Vdc
0	0	1	0	0	1	0	0	-3Vdc
0	0	1	0	1	0	0	0	-4Vdc
0	1	1	0	0	0	0	0	-5Vdc

For eleven level inverter, similar to five level inverter, the predefined output voltage waveform is drawn as shown in the figure 8. Equation 6 gives the Fourier series expansion of the output voltage of the eleven level inverter, which is derived from the predefined switching pattern for the eleven level inverter.

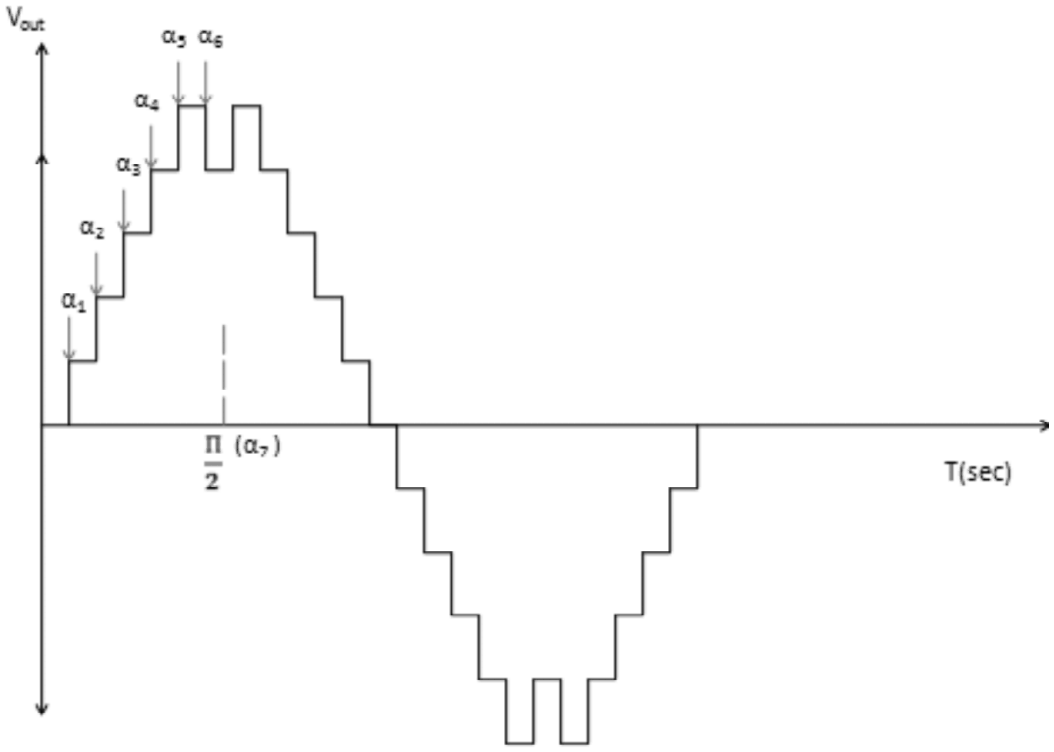

Figure 8: Predefined output voltage waveform of eleven level inverter

$$V_{out} = \sum_{n=1,3,5...}^{\infty} \frac{4V_{dc}}{n\pi}\left(\cos(n\alpha_1)+\cos(n\alpha_2)+\cos(n\alpha_3)+\cos(n\alpha_4)+\cos(n\alpha_5)-\cos(n\alpha_6)\right)\sin(nwt) \quad (6)$$

3.2. SHEPWM for eleven level inverter

As similar to five level inverter the equations 7 and 8 are the nonlinear equations for the SHEPWM of eleven level inverter.

$$H_1 = \frac{4}{\pi}[\cos(\propto_1)+\cos(\propto_2)+\cos(\propto_3)+\cos(\propto_4)+\cos(\propto_5)-\cos(\propto_6)] = sM \quad (7)$$

Where M = $\frac{h1}{sVdc}$ is the modulation index, h_1-Fundamental component of the output voltage

s = 4 for eleven level inverter

$$H_n = \frac{4}{n\Pi}[\cos(n \propto_1)+\cos(n\propto_2)+\cos(n \propto_3)+\cos(n \propto_4)+\cos(n \propto_5)-\cos(n \propto_6)] = 0 \quad (8)$$

n = 3, 5, 7, 9, 11, 13

The switching angles for eleven level inverter are pre calculated by solving the equations. By applying the switching angles, the fundamental harmonic content is set to the expected value and the harmonics up to 13 are completely eliminated. The figure 9 and 10 show the output voltage and the frequency spectrum of output voltage wave form for the eleven level inverter with SHEWM technique. From the figure10 it is clear that the harmonics up to 13 are completely eliminated. The THD upto 40^{th} harmonics is 10.52%. The parameters used for the simulation of eleven level inverter is shown in the table 5.

Table 5
The parameters used for the simulation of eleven level inverter

Parameters	*Values*
Voltage across capacitor(Vdc)	100 V
Switching Frequency of S1	100 Hz
Switching Frequency of S2	250 Hz
Switching Frequency of S3	50 Hz
Switching Frequency of S4	50 Hz
Switching Frequency of S5	250 Hz
Switching Frequency of S6	200 Hz
Switching Frequency of S7	200 Hz
Switching Frequency of S8	250 Hz
Output Voltage Frequency	50 Hz

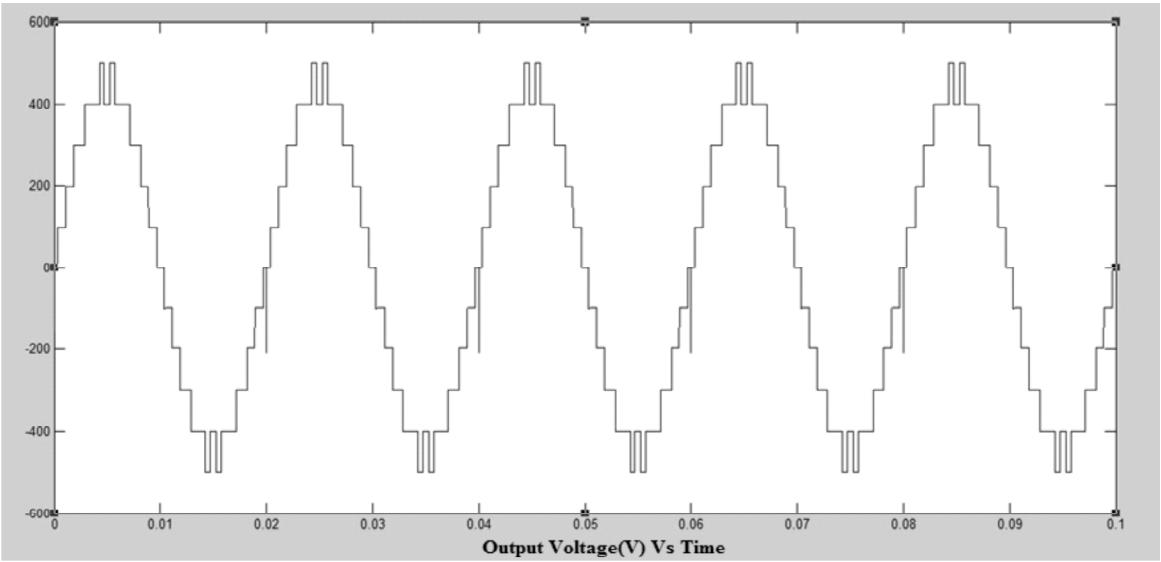

Figure 9: Output voltage of eleven level transistor clamped inverter with SHEPWM technique

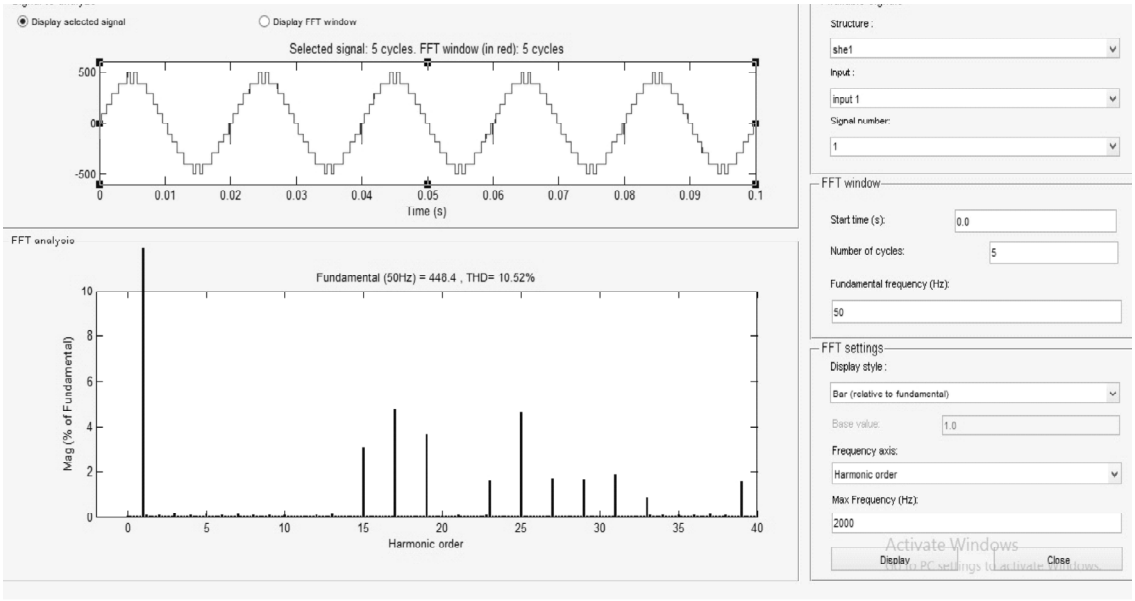

Figure 10: Frequency spectrum of Output voltage of eleven level inverter with SHEPWM technique

3.3. SHMPWM Method for eleven level inverter

Similar to five level inverter, the SHMPWM method is applied for eleven level inverter. The equations are the inequality equations for the eleven level inverter with SHMPWM technique. By solving these equations the switching angles are estimated. The same grid codes, which is shown in the table are used as limited values(Ln).

$|sM - H_1| \le L_i$, where M = $\frac{h1}{4Vdc}$ and [cos($\propto_1$)+cos($\propto_2$)+cos($\propto_3$)+cos($\propto_4$)+cos($\propto_5$)-cos($\propto_6$)]

s = 4 for eleven level inverter

$$H_n = \frac{4}{n\Pi}\left(\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) + \cos(n\alpha_5) - \cos(n\alpha_6)\right) \le H_1 L_n$$

n = 5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35.

With the calculated switching angles the controlled transistors of eleven level transistor clamped inverter are fired. The figures 11 and 12 show the output voltage and its frequency spectrum for eleven level inverter with SHMPWM technique. It is depicted from the figure11 that the harmonics up to 35 are mitigated and the THD up to 40th harmonics is 8.17% which is less compared to SHEPWM method (10.52%).

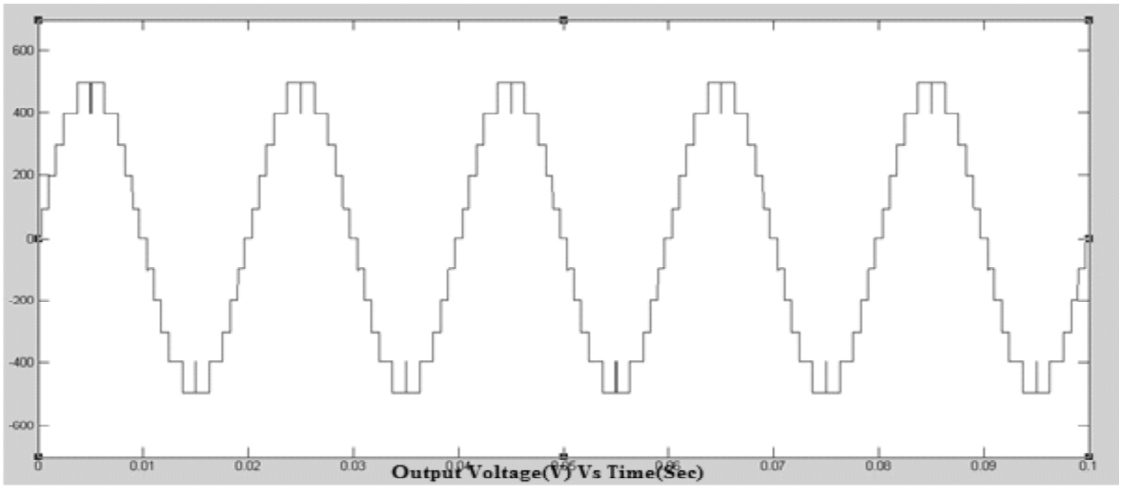

Figure 11: Output voltage of eleven level transistor clamped inverter with SHMPWM technique

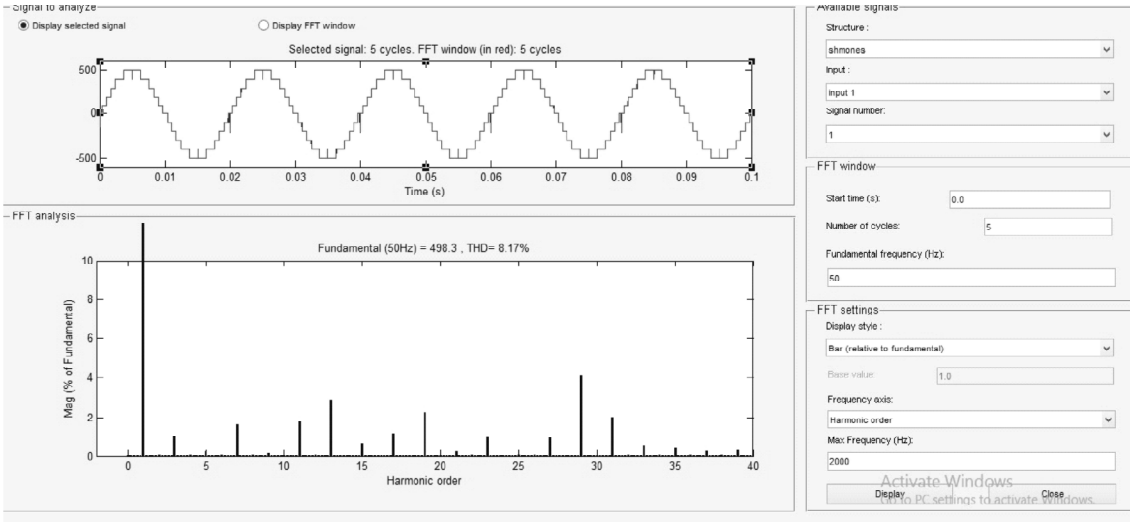

Figure 12: Frequency spectrum of Output voltage of eleven level inverter with SHMPWM technique

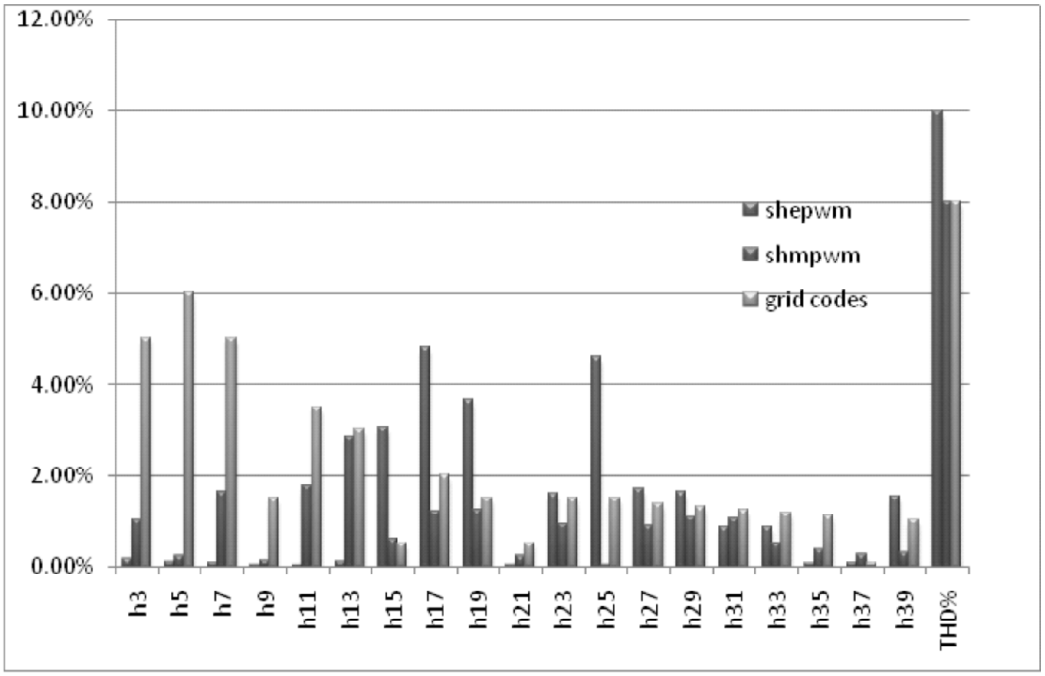

Figure 13: comparison of the SHEPWM method and SHMPWM method with the limited values for eleven level inverter

The figure13 shows the comparison between the SHEPWM method and SHMPWM method with the limited values given by the gridcodes for eleven level transistor clamped inverter. From the figure13 it is visible that using SHMPWM method the harmonics up to 40 are mitigated below the limited values.

CONCLUSION

In this paper SHMPWM technique was introduced for transistor clamped five level and eleven level inverters. The transistor clamped topology of five level inverter is having only five controlled transistors and eleven level inverter is having only eight controlled transistors only, which reduces the cost of the system and simplifies the control circuit. The simulation result of five level inverter with SHMPWM method gives the output voltage with the THD up to 40th harmonic as 19.02%, which is low compared to SHEPWM method(32.09%). Even though the THD is less for five level inverter using SHMPWM technique, few harmonics are violating the grid code's standard. But using SHMPWM technique for eleven level inverter all the harmonics up to 35 are limited below the grid code's standards. The switching frequency of the switches used for the simulation of eleven level inverter are 50Hz,100Hz,200Hz and 250Hz. Even with the low switching transitions, the eleven level inverter with SHMPWM gives the output voltage with THD up to 40th harmonic as 8.17%, which is approximately equal to gridcode's standard (8%) and. less compared to SHEPWM method (10.52%).

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