International Journal of Control Theory and Applications

ISSN : 0974-5572

Volume 9 • Number 45 • 2016

Study and Designing of Fourth Order BEC Circuit for Flash Analog to Digital Converter Using MUX Based Encoder

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Abstract : Binary code plays an important role in the field of digital signal processing and hence a thermometer to binary encoder acts as a vital element in functioning of flash ADCs. Output of flash ADCs is in thermometer code. Ideally, thermometer code shows single transition but in case of clock jitters and device mismatch multiple transitions take place introducing bubbles in the code. This error leads to acute inaccuracy in encoding process. In the present work a bubble error correction circuit has been proposed that can eliminate bubble error upto fourth order as compared to existing circuit that eliminated error only upto third order. Simulation shows the transistor requirement of existing and proposed circuit is same thus making present circuit more efficient and acceptable.

Keywords : *Flash ADC, TIQ technique, Bubble error correction circuit, MUX based encoder.*

1. INTRODUCTION

The majority of signals existing on the planet are analog in nature.Digital signals as compared to analog signals show many advantages like signal security, strength,less noise interference etc. Circuit making use of digital signals are faster and hence the errors that could have induced due to the transmission purposes reduces significantly. Hence, there arises the need of a conversion circuit converting analog signals efficiently into digital signals. Increasing use of small sized battery operated devices can be sustained by a low power flash ADC and hence power consumption is a major concern in the design of ADC which could be used in certain devices like mobile phones, laptops, etc.

Present work deals with the Threshold Inverter Quantization approach in designing of a comparator circuit. This approach abolishes the use of an array of resistors from the usually used flash Analog to Digital converter which leads to the reduction in the area of the chip ultimately cutting down the power consumption.

Although wallace-tree encoder is capable of self correction of bubble errors however the circuit becomes relatively complex with lower speed and higher power consumption. On the other hand MUX based encoder operates at a high speed which means less delay.

2. ADC AND ITS ARCHITECTURE

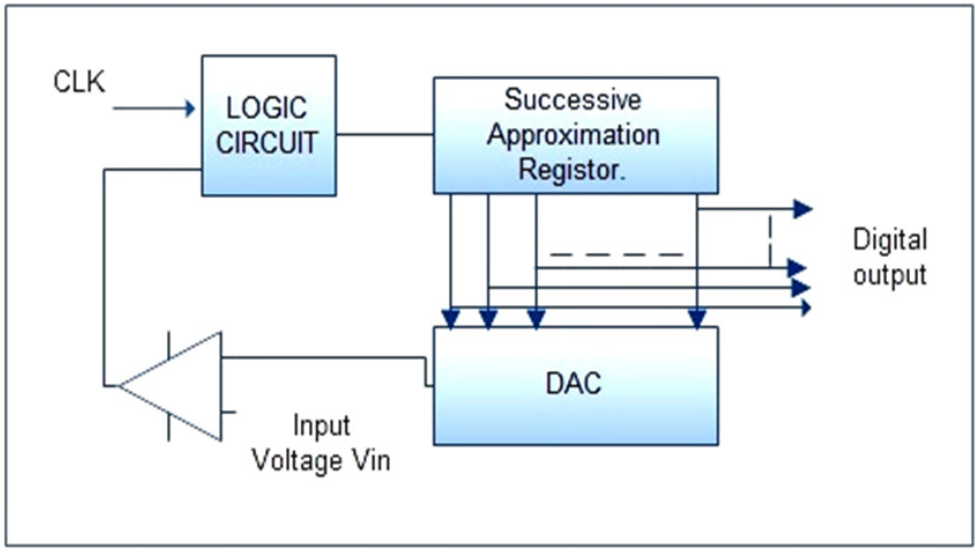

Figure 1: Block diagram of Successive Approximation ADC

Analog-to-digital converter does the conversion of a continuous quantity like a voltage into a digital form. The process of the conversion involves sampling of the analog signal followed up by quantization. The result which we get is a sequence of digital values which have been obtained from continuous-time as well as the continuous amplitude signal.

We have studied the architecture of :

1. Flash ADC
2. Pipelined ADC
3. SAR ADC
4. ∑Δ ADC

By studying the reference papers[1-4] we have formulated asummary which is as below:

Table 1
Summary of ADC Architecture

Architecture	*Resolution(bits)*	*Speed(sps)*	*Latency(cycle)*	*Comments*
Flash	<10	250M- 1G	1	• Extremely fast • Input bandwidth is high • Power consumption is max. • Uneconomical
Pipelined	8-16	1M – 100M	M	• Throughput rate is high • Low power consumption • On-chip self calibration • Needs 50% duty cycles • Requires minimum clock freq.

Architecture	*Resolution(bits)*	*Speed(sps)*	*Latency(cycle)*	*Comments*
SAR	10-18	76K – 5M	N	• Resolution and accuracy are high • Power consumption is low • Few external components • Sampling rates are limited • Input bandwidth is low
ΣΔ	>14	> 200K	Large	• Resolution is quite high • Input bandwidth is high • Digital on-chip filtering • Limited sampling rates

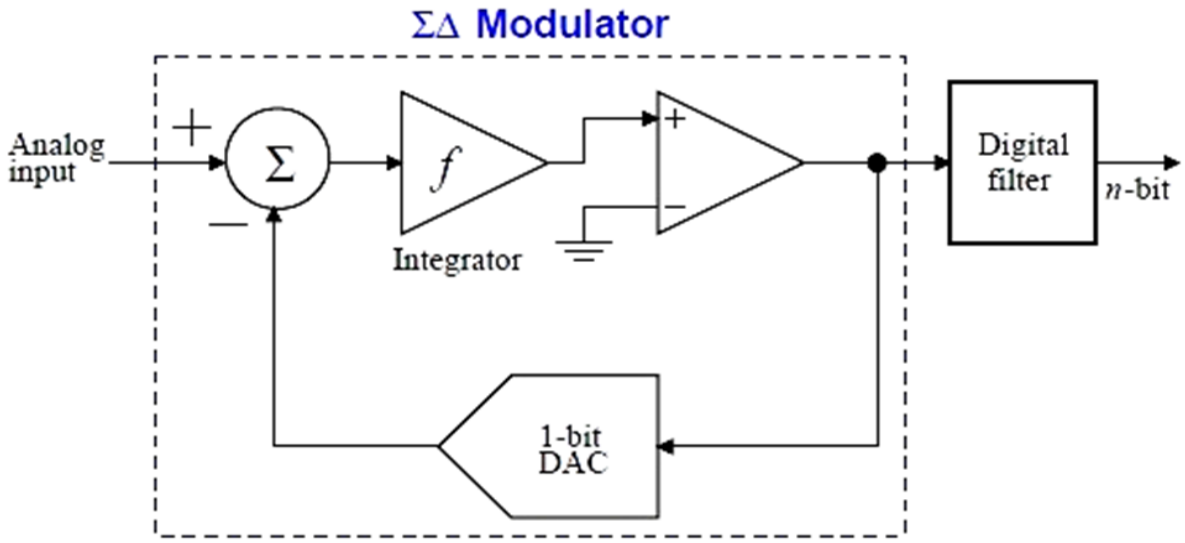

Figure 2: Block Diagram of Sigma Delta ADC

3. TIQ FLASH ADC

In N-bit Flash ADC , comparison takes place between the input analog voltage and the reference voltage using 2^N-1 comparators which produces thermometer code as the output. Resistor ladder is used to generate the reference voltage. The design of resistive ladder is very complex contributing in larger size and power.

TIQ Comparator compares analog input signal with reference voltage converting the analog signal to digital form. When the input voltage signal is lower relative to reference voltage the output is '0' and else the output will be'1'. Circuitry for gain booster circuit consist of two cascading inverters same as that of comparator but differ in the sizing of transistor.TIQ comparator comprises of two cascaded CMOS inverters. Function of first inverter is to set the reference voltage of comparator. It is done by varying the width and length of both transistors of inverter. Voltage gain is enhanced by the second inverter. V_m can mathematically be stated as under:

$$V_m = \frac{\sqrt{\frac{p}{n}\frac{p}{n}}.(V_{dd} - |V_{TP}|) + V_T}{\sqrt{\frac{p}{n}\frac{p}{n}}} \quad (1)$$

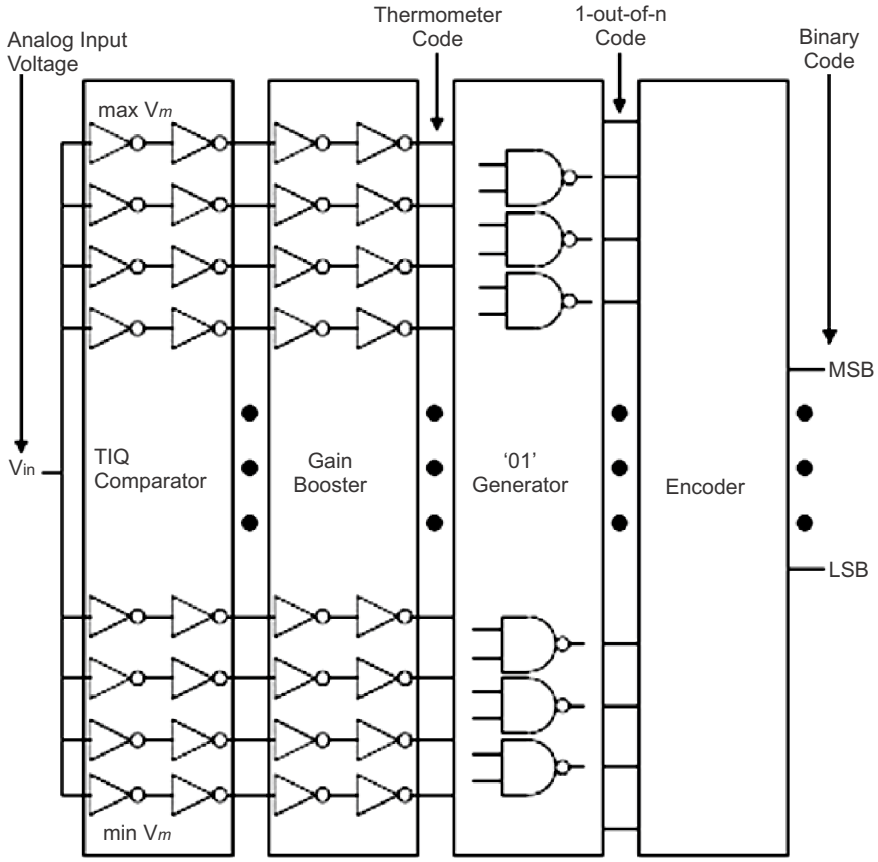

Figure 3: Block diagram of TIQ Comparator [15]

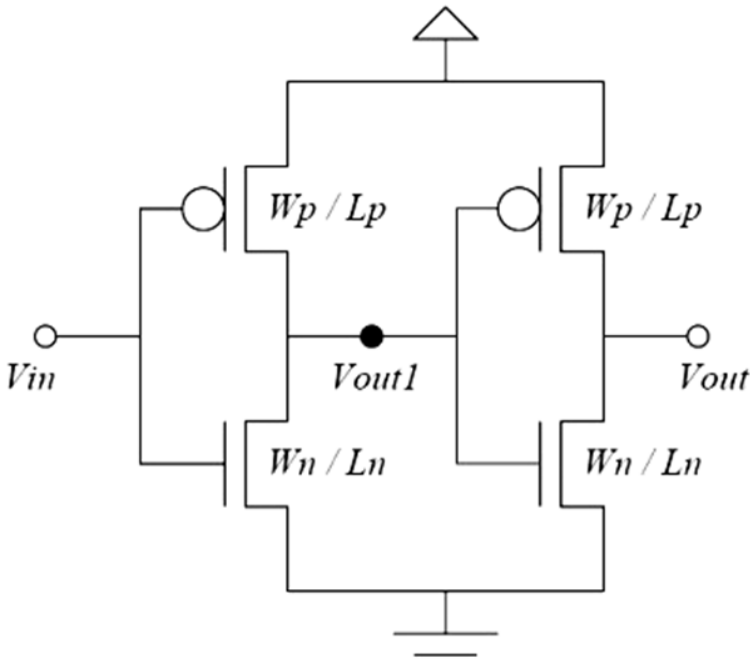

Figure 4: Circuit diagram of TIQ Comparator[5]

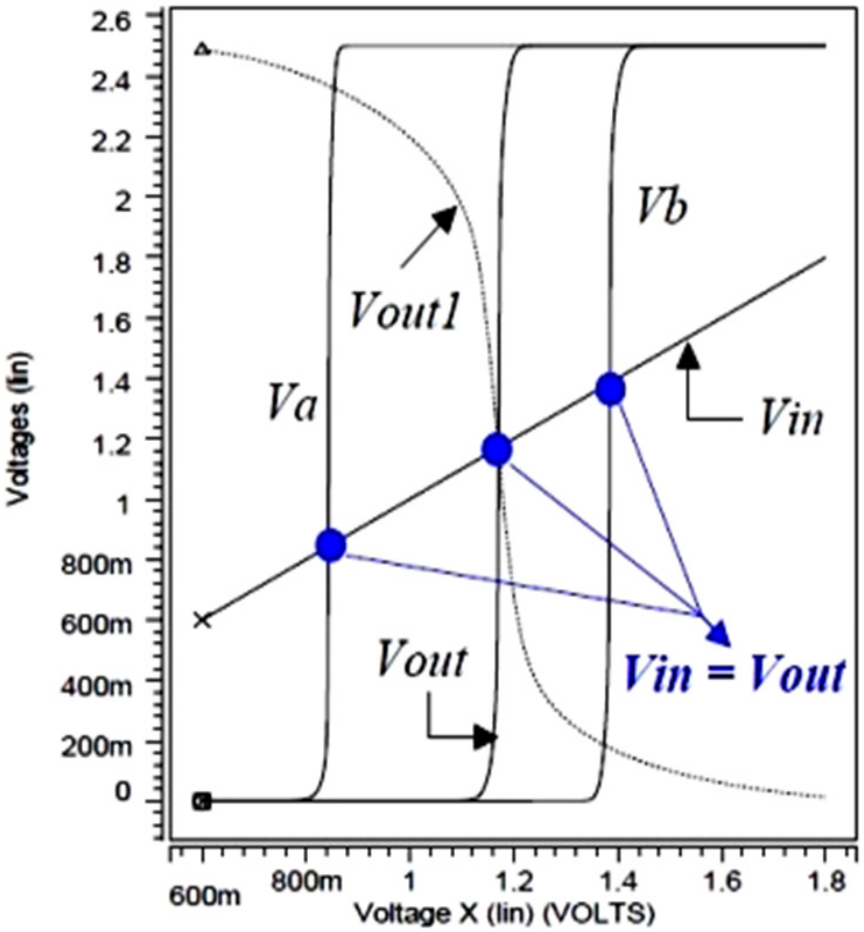

Figure 5. VTC of TIQ Comparator [5]

The TIQ technique has several benefits:[6]

1. Simplicity of comparator circuit.
2. Higher rate of comparison.
3. Elimination of the Resistor ladder network.

4. BUBBLE ERROR

A phenomenon in which the input to TH2B have one or more invalid bits is termed as bubble error. Due to multiple transitions in thermometer code the invalid bits also known as bubbles come into existence[7,8]. It is mainly caused by device mismatch, comparator offset voltage and clock jitters. Offset voltage differencebetween the comparatorsgreater than 1 LSB introduces the bubble error[9].Various order of bubble error exists ranging from first order to nth orderas per the number of invalid bits.

Introduction of bubble in the sequence generated by flash ADC causes feeding of the invalid input bit to MUX based encoder. Ultimately, the output of TH2B encoder will turn fallacious. Since the input given to TH2B is an fallacious thermometer code, TH2B circuits might show deviation from the expected output.

Table 2 shows bubble error of various order in a 15-to-4 TH2B encoder input.

Table 2
Table explaining bubble error correction

	Input with bubble error			*Proposed BEC circuit output*		
	A	B	C	A	B	C
T15	0	0	0	0	0	0
T14	0	0	0	0	0	0
T13	0	0	0	0	0	0
T12	0	0	0	0	0	0
T11	0	1	0	0	1	0
T10	1	1	1	1	1	1
T9	1	0	1	1	1	1
T8	1	0	1	1	1	1
T7	1	1	1	1	1	1
T6	0	1	1	1	1	1
T5	1	1	0	1	1	1
T4	1	1	0	1	1	1
T3	1	1	0	1	1	1
T2	1	1	1	1	1	1
T1	1	1	1	1	1	1

In the above table we can see various orders of bubble error ranging from first order to third order bubble error. Sequence without bubble error is 000001111111111. From the column A we can see appearance of a zero at the T6 bit hence making the above sequence invalid. This situation is repeated in column B & C where second order bubble error and third order bubble error is introduced.

5. ENCODERS FOR ADC

5.1. Rom Based Encoder

Basic methodology to convert thermometer code to binary or gray code is to use a gray or binary ROM based encoder [10]. ROM is a programmable logic device. It will store combination of the input variables and for every combination it generates the output.

5.2. Fat Tree Based Encoder

The process of encoding of the Thermometer to binary code is done in two stages by using this encoder. Fat tree encoder does not have a requirement of clock signal as well as sensing amplifiers and also the pull-up resistors. It is much more tolerant to noise as compared to the ROM circuit. The complete static CMOS implementation of OR gates will eliminate the consumption of static power Hence, the circuit will be very less power consuming as compared to the ROM circuit. The layout of fat tree is much more difficult for us to design as compared to the ROM. The Boolean expressions of the 4 bit flash ADC fat tree encoder are.

$$
\begin{aligned}
G_3 &= d_0 \\
G_2 &= d_0 \oplus (c_0 + c_1) \\
G_1 &= (c_0 + c_1) \oplus (b_0 + b_1 + b_2 + b_3) \\
G_0 &= (b_0 + b_1 + b_2 + b_3) \oplus (a_0 + a_1 + a_2 + a_3 + a_4 + a_5 + a_6 + a_7)
\end{aligned} \tag{2}
$$

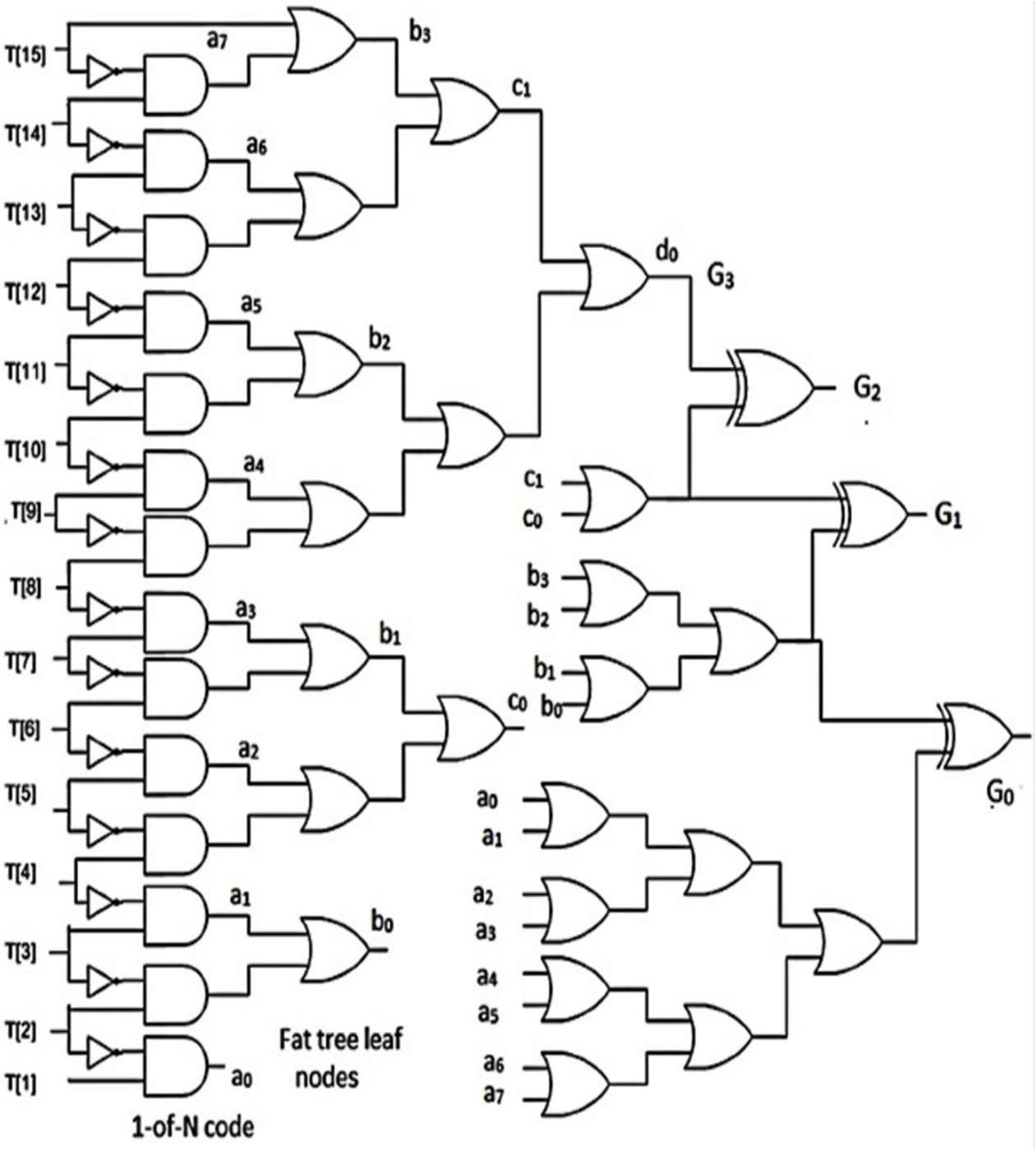

Figure 6: Fat Tree based encoder

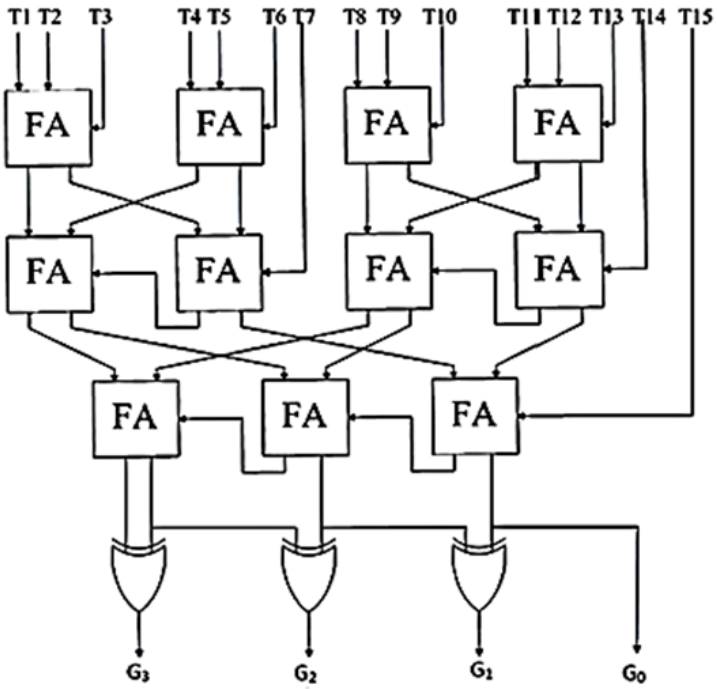

Figure 7: Wallace Tree based encoder

5.3. Wallace Tree Based Encoder

Wallace tree encoder [13] is extremely uncomplicated approach which counts the number of 1's. The Wallace tree based decoder counts the number of number of 1s. This is useful for bubble Suppression. Large delay and power are the disadvantage of this approach.[7,11]

The number of full adders being used in the Wallace tree encoder is given by the following equation:

$$m = 2^n - n - 1 \tag{3}$$

Referring to the above equation, m is the number of full adders used for n bit flash ADC. Best advantage of Wallace tree encoder is the encoded value is precisely matched with best approximated value of the output. However, it will take a long latency in order to get the results. So therefore it will not be suitable for the high speed operations which are higher than 1GHz.

5.4. Design- Proposed Circuit : Bubble Error Correction Circuit

We have proposed a MUX based Thermometer to Binary encoder with the BEC circuit that can eliminate bubble error upto fourth order. The thermometer code is converted to binary code using a MUX-based encoder.

MUX based encoder uses only 2:1 MUX and works on binary search algorithm. Level of significance decides the generation of bits[12,13]. A n-bit encoder has 2^n-1 input bits(thermometer code).Centre bit of thermometer input acts as MSB. MSB goes high when more than half of the input bits is high. Next lower significant bit can be found by dividing the thermometer code into two parts separated by MSB.2:1 MUX decodes the center bit of two divided parts and the earlier output *i.e.*, MSB will now act as multiplexer's control signal. Multiplexer's output forms the next lower significant bit. This splitting continues for the next lower significant bit and are multiplexed recursively until only one 2:1 MUX is left behind.

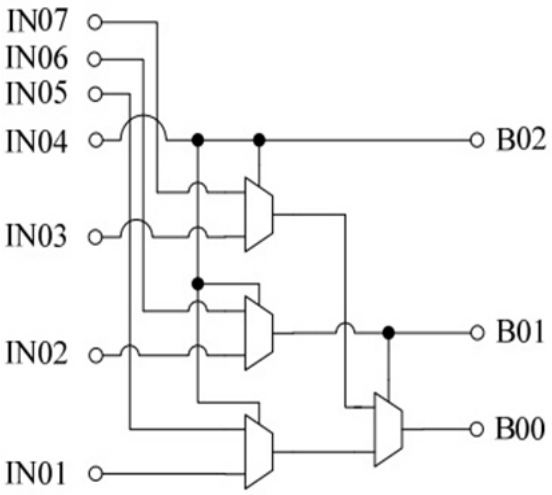

Figure 8: MUX based 7 to 3 TM2B encoder without BEC circuit

For an *n*-bit MUX based encoder, the number of transistor used is-

$$T_{MX} = 4.\sum_{i=1}^{n-1}(2^{n-i}-1) \tag{4}$$

Past researches shows the bubble error correction ability upto third order. Here, we proposes BEC circuit which corrects the bubble errors up to fourth order. Block diagram of the proposed circuit has been shown in the figure 9. The MUX based Thermometer to Binary encoder in the previous researches has effectively turned to the Multiplexer based sub circuit in the proposed circuit. Now the proposed BEC circuit is added prior to the MUX based encoder circuit. This new circuit will now remove the bubble error upto fourth order in the thermometer code[14].

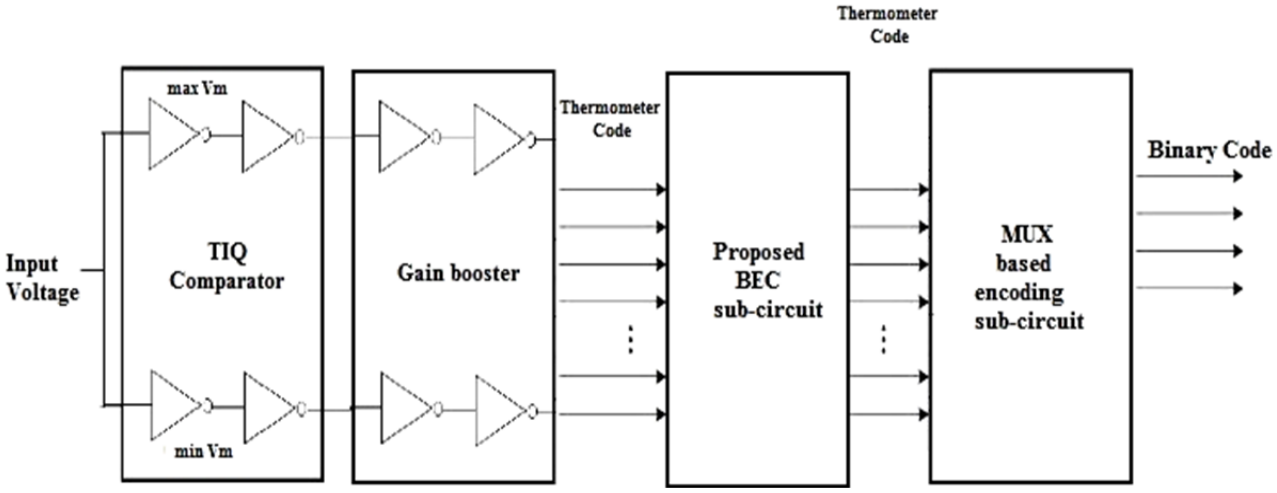

Figure 9: Block diagram of proposed-circuit

A set of 2 inputs-OR gate, 3 inputs-OR gate and 4 inputs-OR gate forms the basis of BEC sub circuit. Leaving aside the most significant bit, the output of 4 inputs-OR gate circuit will be given by the equation below.

$$OUT_i = IN_i + IN\ i+1\ IN_{i+2} + IN_{i+3}$$

The output of 3 inputs-OR gate circuit will be given by the equation below.

$$OUTi = INi + IN\,i + 1 + IN\,i + 2$$

The output of 2 inputs-OR gate circuit will be given by the equation below.

$$OUTi = INi + IN\,i + 1$$

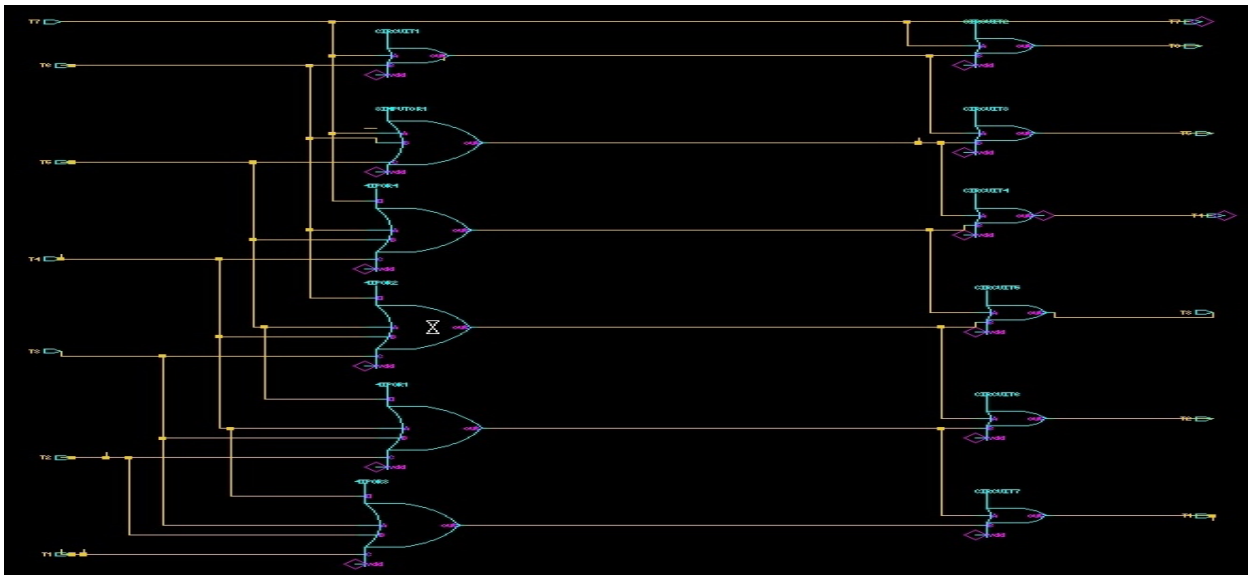

Figure 10: Proposed-BEC sub circuit

6. RESULTS AND DISCUSSION

Number of transistors required in different types of encoder can be understood through table 3.Although ROM based encoder requires less transistors the conversion speed is relatively slow and because of constant static current which is used for presetting the encoder the power consumption goes high. Wallace tree requires lesser transistors but is unsuitable for the high speed of operations. Fat tree encoder has slightly less transistor requirement than proposed circuit but it's difficult layout abide us from using it.Proposed BEC circuit with MUX based encoder eliminate bubble error upto fourth order whileexisting circuit eliminatebubble error upto third order even when the requirement of transistors for both circuit remains same making our circuit more acceptable and efficient.

Table 3
Circuit complexity of 63-to-6 TM2B encoder circuits

Circuit	*Transistor Requiremnent*
ROM-based + BEC circuit	714(210 + 504)
Fat-tree + BEC circuit	832(428 + 504)
Wallace tree + BEC circuit	722
MUX-based + existing BEC circuit(upto 3rd order)	836(342 + 494)
MUX-based + proposed BEC circuit(upto 4th order)	836(342 + 494)

7. CONCLUSION

In this paper, we have proposed a BEC circuit which has to be added prior to the MUX-based Thermometer to Binary encoder that can remove the bubble error upto fourth order. Flash ADC based on the TIQ technique is used instead of the primitive resistor ladder network technique. Bubble error occurs due to the mismatch of devices, comparator offset voltages , clock jitters, etc. can be eliminated using the proposed circuit. New circuit can be used with all previous encoder methods to correct bubble error just by making some design changes. Simulation of circuit will be done in future work which would include variation in simulation technologies and variation in (W/L) ratio to show that our proposed circuit will have lower complexity and lower consumption of power. Proposed circuit will be tested in order to verify the simulation results in the next research.

REFRENCES

[1] Daly D C , Chandrakasan A P.A 6-bit, 0.2 V to 0.9 V Highly Digital Flash ADC With Comparator Redundancy, Solid-State Circuits, IEEE Journal , vol. 44, pp. 3030-3038, November 2009.

[2] Deguchi K , Suwa N, Ito M, Kumamoto T and Miki T. A 6-bit 3.5- GS/s 0.9-V 98-mW Flash ADC in 90-nm CMOS, Solid-State Circuits, IEEE Journal , vol. 43, pp. 2303-2310, October 2008.

[3] Sandner C, Clara M, Santner A, Hartig T, and Kuttner F, A 6-bit 1.2-GS/s low-power flash-ADC in O.13-μm digital CMOS, Solid-State Circuits, IEEE Journal oj, vol. 40, pp. 1499-1505, July 2005.

[4] R. van de Plassche, CMOS integrated analog-to-digital and digital-to analog converters. 2nd ed. Kluwer Academic Pulisher, 2003.

[5] Kumar Piyush. Low-Power Heterogeneous Encoder Based 4-Bit Flash ADC Using TIQ, International Journal of Electrical and Electronics Research ISSN 2348-6988 (online) Vol. 3, Issue 2, pp: (662-669), Month: April - June 2015

[6] Agrawal N, Paily R. An improved ROM architecture for bubble error suppression in high speed flash ADCs, Student Paper, 2008 Annual IEEE Conference, Aalborg, 2008, pp. 1-5.

[7] Sall E, Vesterbacka M , Andersson K O. A study of digital decoders in flash analog-to-digital converters, Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on, 2004, pp. I-129-I-132 Vol.1..

[8] Razavi B. Principles of data conversion system design. IEEE Press; 1995.

[9] Chunn A , Sarin R K . Comparison of thermometer to binary encoders for flash ADCs, India Conference (INDICON), 2013 Annual IEEE, Mumbai, 2013, pp. 1-4.

[10] Chuang Yao-Jen, Ou Hsin-Hung , Liu Bin-Da. A novel bubble tolerant thermometer-to-binary encoder for flash A/D converter, VLSI Design, Automation and Test, 2005. (VLSI-TSA-DAT). 2005 IEEE VLSI-TSA International Symposium on, 2005, pp. 315-318.

[11] Lee Daegyu , Yoo Jincheol , Choi Kyusun , Ghaznavi J . Fat tree encoder design for ultra-high speed flash A/D converters, Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on, 2002, pp. II-87-II-90 vol.2.

[12] .Sall E, Vesterbacka M . Comparison of two thermometer-to-binary decoders for high-performance flash ADCs, NORCHIP Conference, 2005. 23rd, 2005, pp. 253-256. doi: 10.1109/NORCHP.2005.1597037

[13] Sail E, Vesterbacka M . A multiplexer based decoder for flash analog-to-digital converters, TENCON 2004. 2004 IEEERegion 10 Conference, 2004, pp. 250-253 Vol. 4.

[14] Bui van hieu, Senghyun beak, Seunghwan choi, Jongkook seon, Taikyeong ted. Jeong. Thermometer to binary encoder with bubble error correction (BEC) circuit for flash analog to digital converter(FADC), Communications and Electronics (ICCE), 2010 Third International Conference on , 11-13 Aug. 2010, pp 102 – 106

[15] Perumal , Perumal J, V. Yuvaraj. Design of Analog to Digital Converter Using CMOS Logic, Advances in Recent Technologies in Communication and Computing, 2009. ARTCom '09. International Conference on, Kottayam, Kerala, 2009, pp. 74-76.