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Practical Set up to Test a Novel Neutral Point Oscillation Mitigation Technique for Three Level Inverter

K. Narasimha Raju*, O. Chandra Sekhar* and N. Kiran**

Abstract: A perceived and existing issue with three phase neutral point clamped (NPC) inverter is the unbalancing voltage at the neutral point. .The neutral point stabilization is done by various methods like carrier-based PWM, space vector PWM, hybrid PWM. The conventional carrier based PWM technique doesn't provide a valid solution for all power factors and SVPWM is complex in implementation and increases switching losses. In this paper a practical setup has been developed to test a novel carrier-based PWM technique. The proposed technique deals with level shifting of carrier wave based on neutral point voltage and current feedback. The proposed technique is simple in implementation and has more degrees of control over neutral point voltage than the conventional reference level shifting techniques. This is implemented in MATLAB/SIMULINK and a Hardware setup is developed with DSP controller.

Keywords: CB pulse width modulation, NPC inverter, Dc link in stabilization, DSP controller, CCS, Neutral point stabilization.

1. INTRODUCTION

The multilevel converters era has been started in 1975 and are used in high power medium voltage Industrial applications [1]. Multilevel inverter is to synthesize a near voltage from several levels of dc voltages. As number of levels increases, the synthesized output waveform has more steps that approaches a sine waveform. As the steps are added to waveform, the harmonic distortion of the output wave decreases. To obtain a quality output voltage or current waveform it is required to switch the inverter with high-frequencies using various PWM strategies [2]. The increased switching frequency increases the stress on the switch. But for a multilevel inverter with same power level as each switch has to carry only one level of voltage switching stress decreases. The multilevel inverter has been used in different applications like traction drive system, VAR compensation and enhancement active filtering, high voltage motor drive, high voltage dc transmission, FACTS [3]. Multilevel inverters are classified into Diode clamped multilevel inverter, Flying - capacitor multilevel inverter, Cascaded multilevel inverter. Advantages of Diode Clamped Multi-Level Inverter are: (1) They can generate output voltages with extremely low distortion and lower dv/dt. (2) They draw input current with very low distortion. (3) They can operate with lower switching frequency. The major problem with three level inverter is neutral point voltage instability. Due to neutral point deviation the distorted voltage occurs the load. For balancing neutral point voltage different schemes are proposed in literature they are: Carrier based PWM, Space vector PWM[4]. The existing carrier based PWM techniques in the literature proposes to add an OFFSET "f" of appropriate polarity to reference wave. Which would result in stabilization of neutral point oscillation [5], But these techniques doesn't provide a valid solution for all power factors. The other popular technique is the space vector PWM, in this technique the non near vectors are used to control the neutral point oscillation. The drawback of this is complexity of control logic and increased switching loses.

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In this paper, a practical setup to test a novel carrier based PWM proposed in [8] is developed. As per this scheme an OFFSET "f" of appropriate polarity based on neutral point voltage and phase current feedback signals is added to carrier wave. Unlike the conventional carrier PWM techniques were level shifting of reference signal is done. The advantage of level shifting carrier wave is that it has more degrees of control as the no of carrier signals increase with level of inverter and reference signal is only one. A practical setup has been developed with 3 level NPC power circuit, driver circuit, dead time circuit and the control logic has been developed using DSP TMS320F28335.

2. DIODE CLAMPED MULTILEVEL INVERTER

Three-level Neutral point clamped (NPC) Inverter is the most well-known topology of multi-level conversion systems. Figure 1 shows the NPC inverter circuit diagram. The common three level inverters are noteworthy for high power applications. It was invented first by Nabae in 1981 [7]. The main drawback of this model is capacitors unbalancing or neutral point unstable. In a three level inverter, an array of 4 switches and 6 diodes make the leg of NPC to be switched to $V_{dc}/2$, 0, $-V_{dc}/2$. To balance the capacitor voltage unbalance and to rectify Neutral point instabilization a Novel level shifted carrier based PWM with closed loop system is implemented.

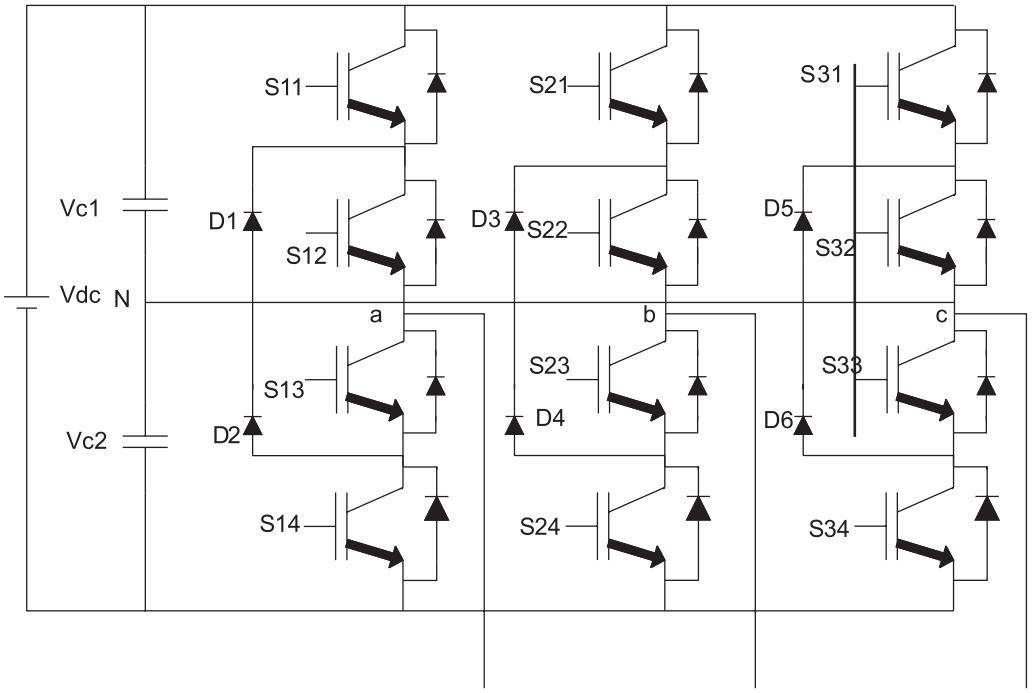

Figure 1: Three phase NPC inverter

3. PROPOSED TECHNIQUE

The proposed technique "A Novel Level Shifted Carrier Based PWM" [8] is opted for three level Diode Clamped Multilevel inverter.

As per the proposed technique the neutral point voltage ($V_{C1} - V_{C2}$) and current are sensed using voltage and current sensors. Based on the neutral point voltage and current using RSS Table 1 [5] offset (f) to be added to carrier signal is determined. The block diagram of the control circuit is shown in Figure 3. The level shifted PWM signals generated are shown in Figure 4. By this the ON-OFF time periods of switches are adjusted, that means ON time period of the switch which discharges a overcharged capacitor is maintained more and OFF time of the switch is reduced and vice-versa. With this modulation of pulse width neutral point balance is attained.

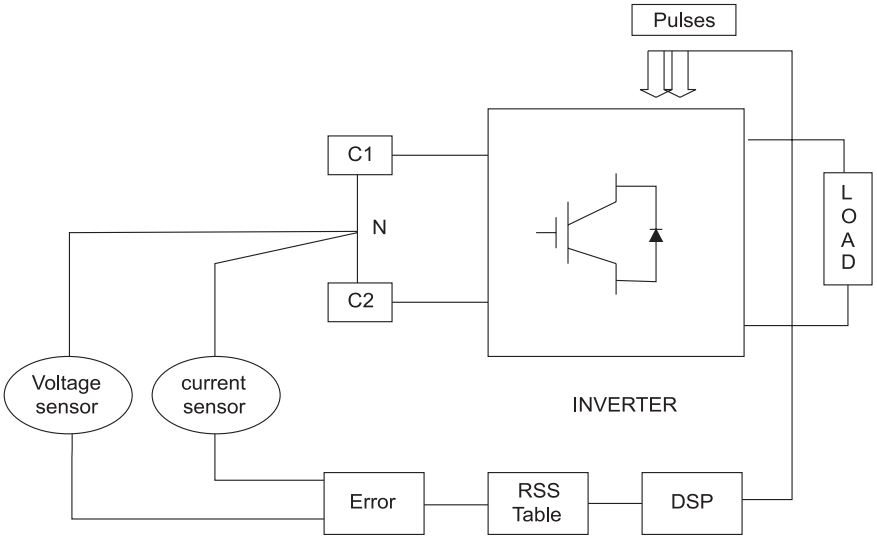

Figure 2: Block diagram for proposed technique

Table 1
RSS Truth table to increment or decrement the value of e for neutral-point voltage balancing

$Sign(V_{C1} - V_{C2})$	$Sign(I_n)$	$Error(e)$
0	–	0
1	1	–1
1	–1	1
–1	1	1
–1	–1	–1

4. SIMULATION MODEL OF PROPOSED CONCEPT

The performance of three-phase neutral point clamped inverter is Simulated in the Matlab/Simulink by choosing the input as V_S = 400 V, R, L Load = 50 ohm and 1 mH, Capacitors C1 = C2 = 10 mf.

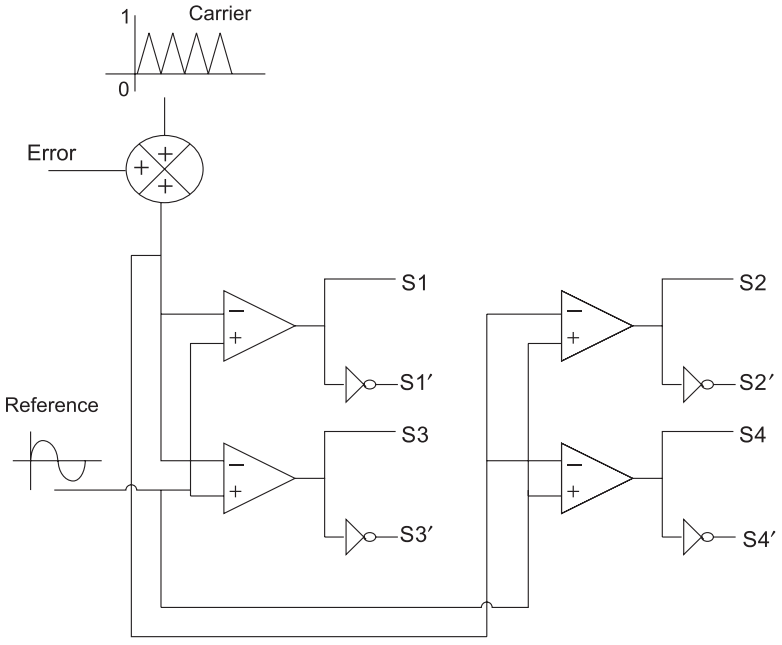

Figure 3: Proposed control technique for simulation

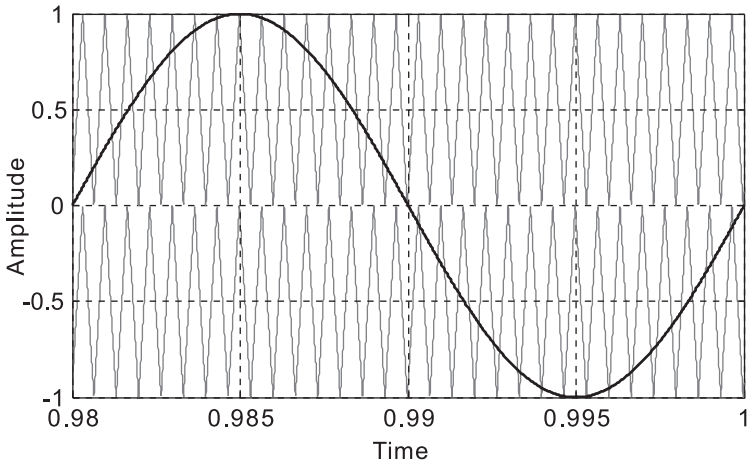

Figure 4: Sine PWM comparison

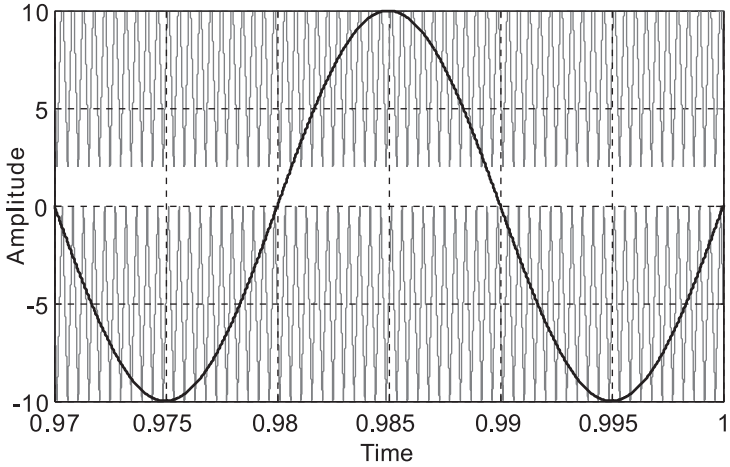

Figure 5: Level shifted comparison

Figure 4 and Figure 5, shows the comparison of carrier and reference signal of conventional SPWM and proposed technique with fundamental frequency 50Hz, the modulation index is 0.8 and device switching Frequency is 1000 Hz using figure.3 model.

5. HARDWARE DESCRIPTION

In practical open loop neutral point clamped inverter is developed with 3KW load in the laboratory. This set up involves development of, printed circuit board (PCB) designed Buffer circuit, PCB designed Gate driver circuit, Driver circuit Transformer, Three level NPC using MOSFET switches, Capacitor bank, Regulated power supply (RPS). For generating the inverter Sine PWM pules with level shifted carrier DSP TMS320F28335 control board is used. The description of circuits, equipment used in hardware development is discussed below.

Buffer Circuit

As the DSPcontroller generated signals are not sufficient to drive the current. A buffer circuit is employed to amplify the current from DSP buffer circuit is connected that gives sufficient current to turn on IGBTs. Figure 6 is buffer circuit designed to amplify current from DSP. Buffers are driving chips, that they boost some characteristics of the circuit. In this case, the current is increased without compromising voltage. Buffer is used to boost the current so that each device may operate properly. A typical gate supplies approximately 1mA- if buffer is added this may upto 15 mA.

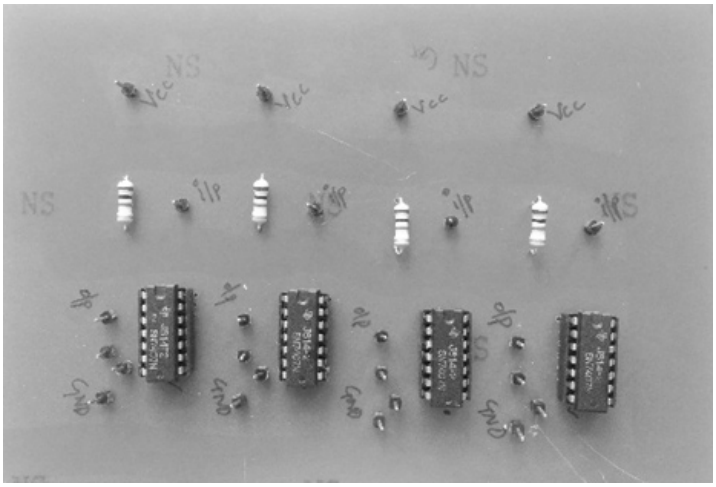

Figure 6: PCB designed Buffer circuit

Gate Driver Circuit

Gate driver circuit provides both positive and negative voltage for MOSFETs that is to turn ON switch positive voltage and turn off switch negative voltages are given. So, gate driver is known as bipolar voltage supplier. Gate driver is used for Electric Isolation between Control and Power circuit. Primary role of isolation and gate driver circuit are, To give required gate voltage and current to MOSFETs for switching, To transmit the control signals to the bridge circuit faithfully, Provides electrical isolation between power switch and control circuit. Driver circuit amplifies control signal to required level for switching of power switch. The TLP250 driver has an output stage and a power supply connection. The extraordinary thing about the TLP250 is an optically isolated driver, meaning that the input and output are optically isolated. Figure 7 shows the circuit board of gate driver used in practical development with opto couplers, rectifier. Supplies 15v, 9v voltage for positive and negative switches. The isolation is optical- the input stage is an LED and the receiving output is light sensitive (photodetector). It is designed for positive voltage it takes 15v and for negative it takes 9v.

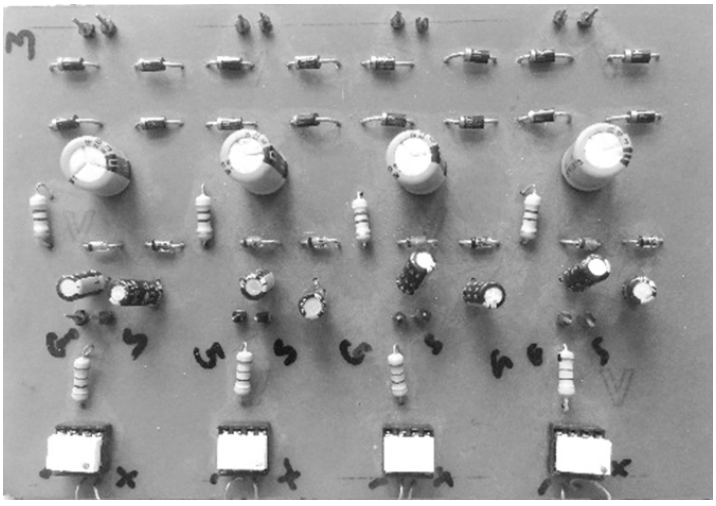

Figure 7: PCB designed Gate driver circuit

Dead-Band Circuit

Dead band is used to produce a delay time between two switches in same phase of inverter. Figure 8 is designed to produce delay time by utilizing NOT gate. The not gate in this gives complimentary pulse

for switch to avoid short circuit of the power supply in the PWM inverters. Dead-band control provides a helpful method for battle current “shoot-through” problems in a power converter. “shoot-through” occurs when both the upper and lower switches in the same phase of a power converter are ON simultaneously, this condition shorts the power supply. Shoot-through issues occur because the switches turn on faster than they turn off. It designed to produce 1m/sec delay.

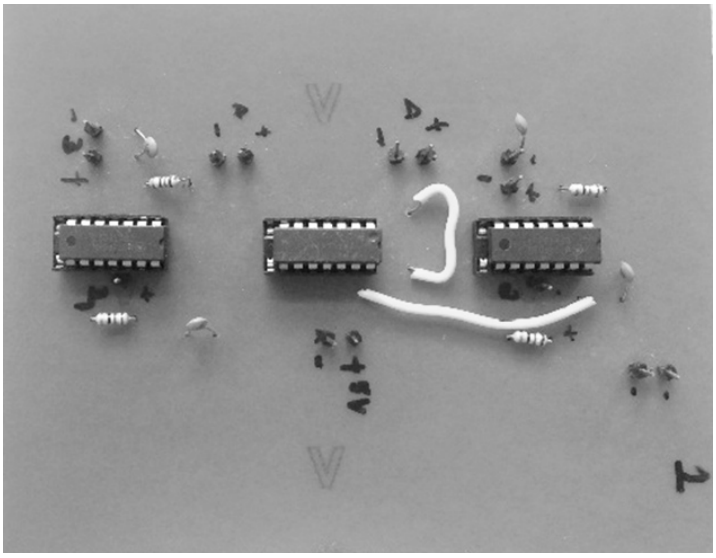

Figure 8: PCB designed Dead-Band circuit

Transformer

A 230/24v multiple output transformer is designed to obtain isolated supply for the driver circuit of different switches in the inverter. This also reduces too many RPS for supplying voltage. Figure 9 shows the 230/24v multiple output transformer which supplies voltage to gate driver circuits.

Figure 9. Practically designed transformer 230/24v

The table.2 shown is the components data sheet which are included for designing practical three level neutral point clamped inverter.

Table.2
Components data sheet

S.No.	*Component*	*Specification*
1	Optocoupler	ICTLP250
2	AND gate	IC7408
3	NOT gate	IC7404
4	Resistors	22 Ω ,390 Ω,70 Ω
5	Capacitors	22 nF, 220 µF, 63 V 1 µF , 63 V
6	Zener Diodes	IN4744A, 1W, 15 V IN4740A, 1W, 9 V
7	Diodes	IN4007
8	Buffer	IC7407
9	Transformer	230/24 volts
10	RPS	0-40 volts
11	Mosfets	IRFP250 Vdss = 200v, Rds = <0.85 ohm, Id = 33A.

6. EXPERIMENTAL SETUP

The block diagram of the experimental setup developed is shown in Figure 10 below.The proposed control logic is developed by programming DSP320F28335 controller using CCSV4.

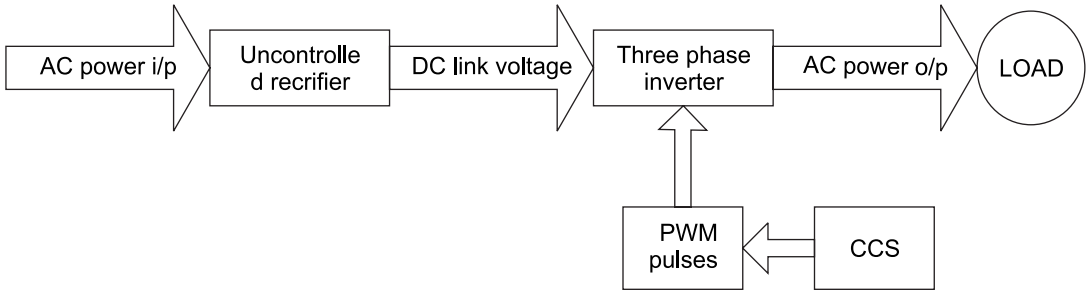

Figure 10: Block diagram for generating PWM pulses using DSP

The PWM pulse generated by DSP is observed in digital oscilloscopeas shown in Figure 11. The experimental setup developed for three level NPC inverter with DSP control board is shown in Figure 12.

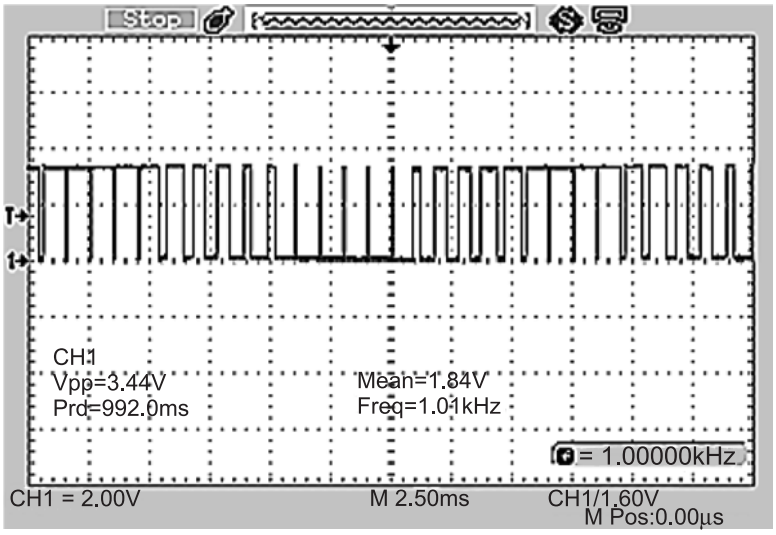

Figure 11: Sine PWM switching pulse at switching

Frequency 1 KHz and duty ratio 50%, Sine = 50Hz

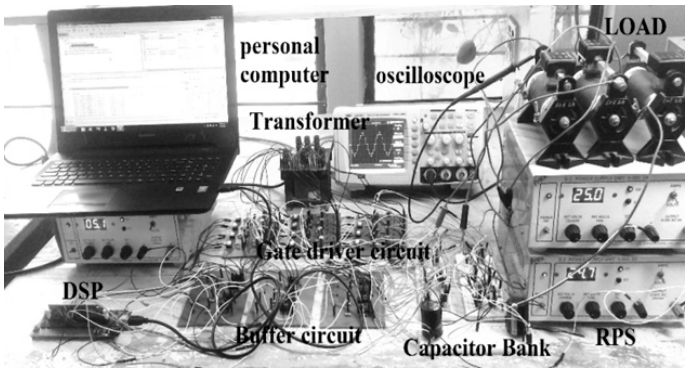

Figure 12: Open loop three level DCMLI inverter inpractical

7. RESULTS

The performance of proposed technique and conventional sine PWM (SPWM) technique are compared in terms of neutral point stabilization of 3level NPC under the following operating conditions.

1. Unbalanced load
2. Different load p.f.
3. Difference in initial capacitor voltages

The respective results in figures (12-19).Figures (30-35) shows the DSP generated PWM pulses for three phase NPC inverter with complimentary with switching frequency 1 KHz. Also three level NPC inverter output voltage is obtained.

Simulation Results:

1. Unbalanced loadconditions: As the unbalanced load is applied on inverter, it causes the variation in charging and discharging times of capacitor which creates neutral point voltage variation. The unbalanced load of about 100Ω, 20mH, 2000Ω is applied on the inverter. The obtained results are shown in Figure (12&13).

   Without feedback

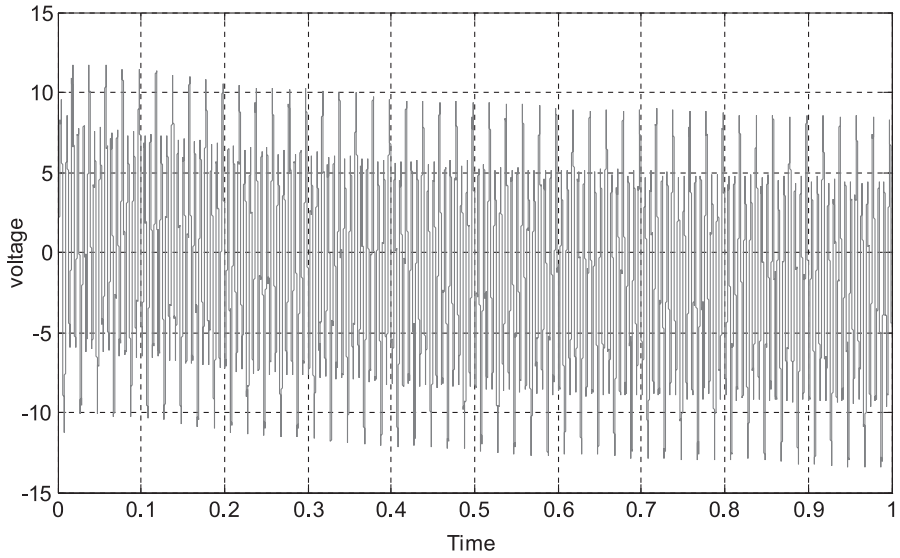

Figure 12: Neutral point voltage with unbalanced load

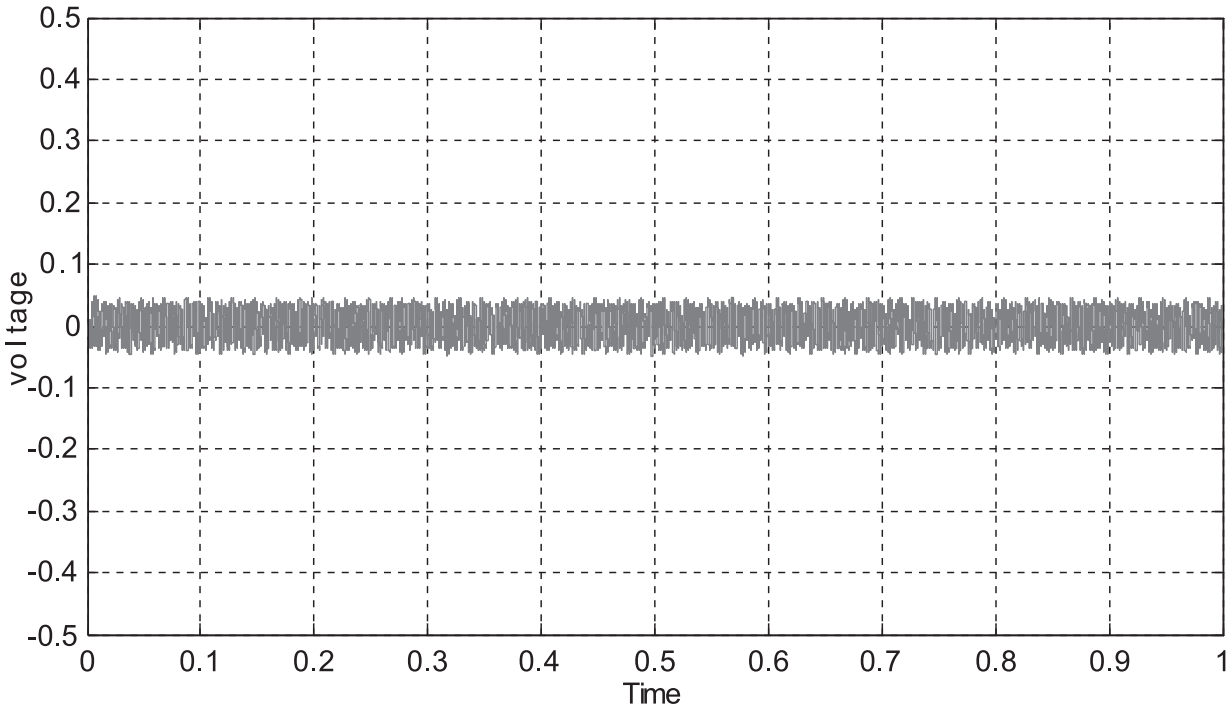

Figure 13: Neutral point voltage with unbalanced load

2. **Different load power factors**: As the power power factor of the load changes, the desired reference changes there by switch on and off time changes this causes neutral point voltage variation. The proposed technique is applied for 0.2, 0.6 and 0.8 power factor loads. The obtained results are shown in Fig's (14 - 18).

With feedback

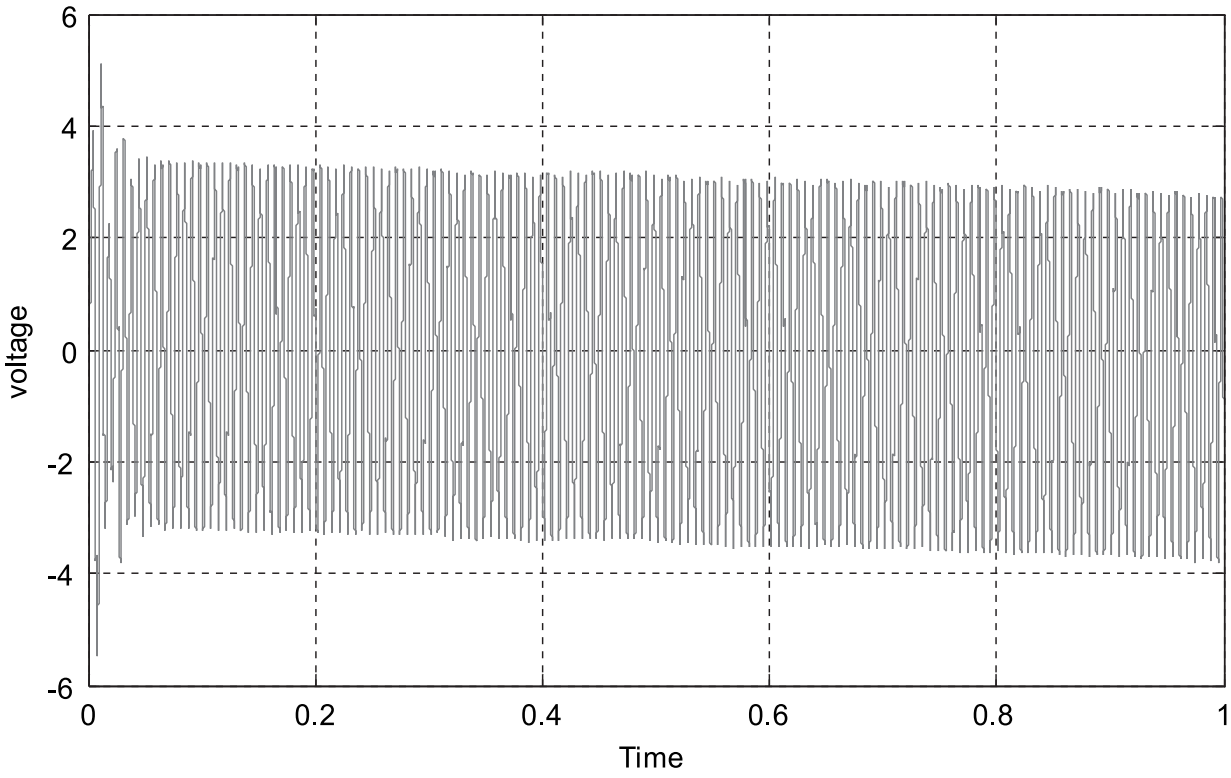

Figure 14: Neutral point voltage at Power factor 0.2

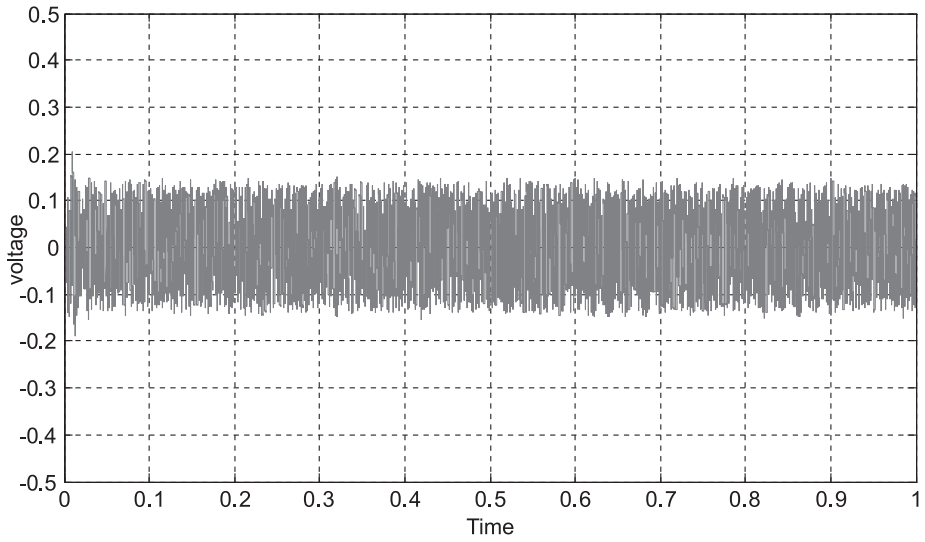

Figure 15: Neutral point voltage at Power factor 0.2

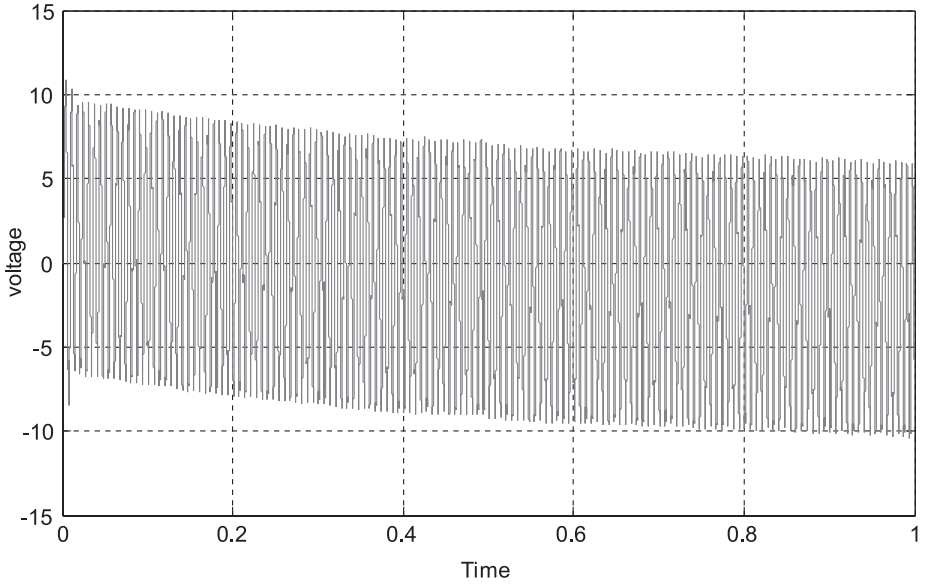

Figure 16: Neutral point voltage at Power factor 0.6

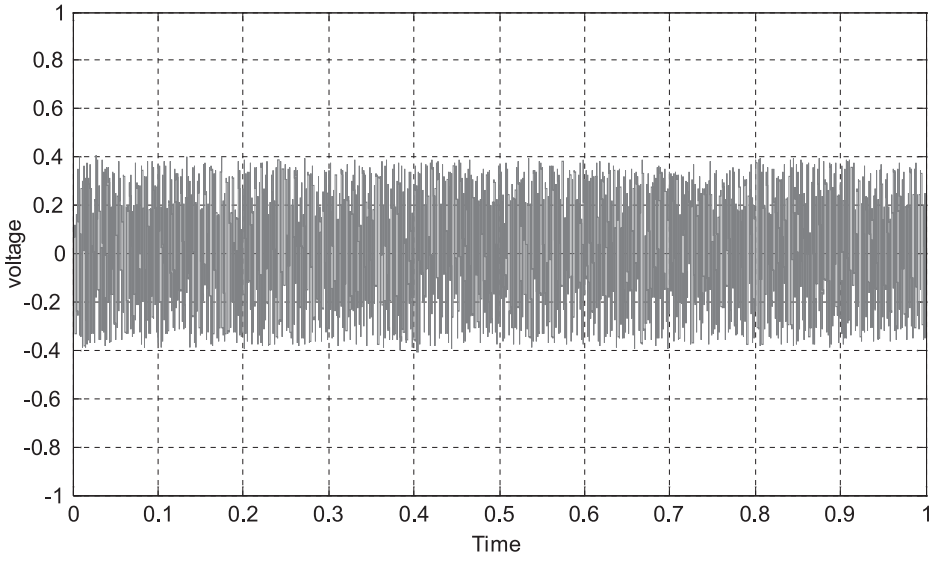

Figure 17: Neutral point voltage at Power factor 0.6

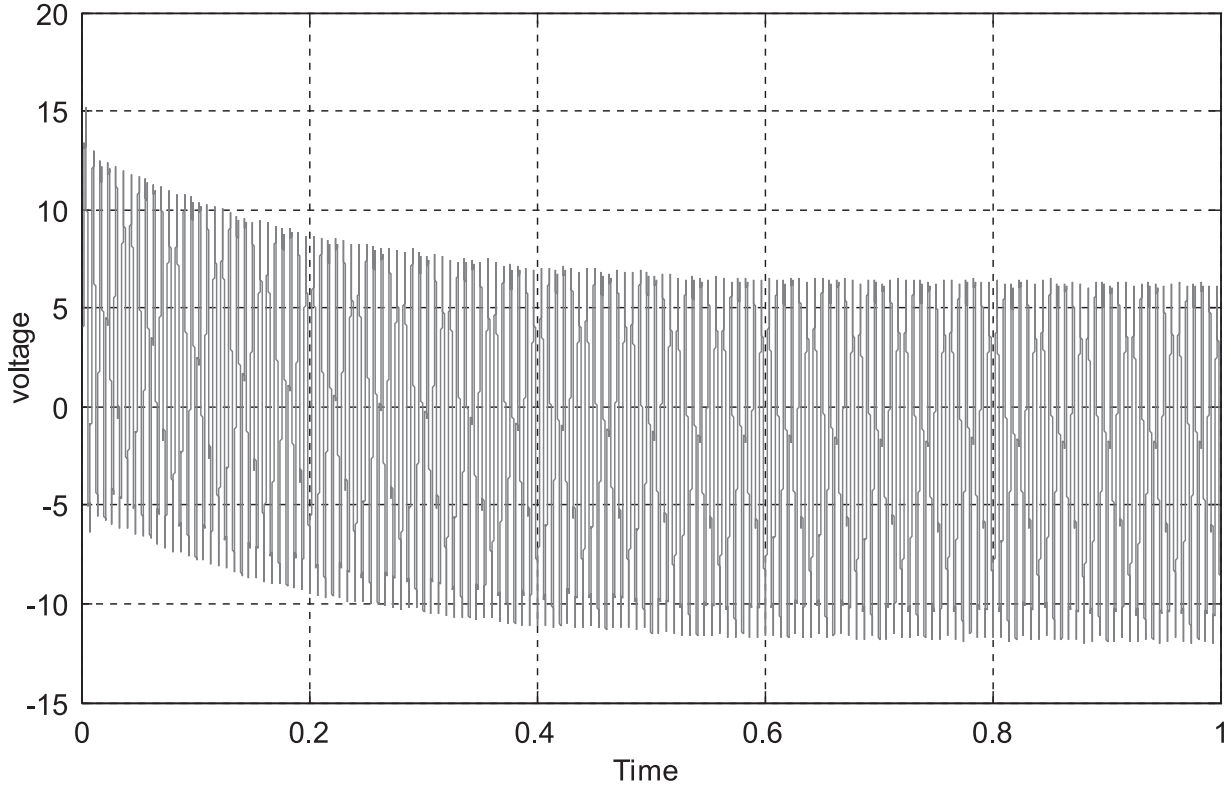

Figure 18: Neutral point voltage at Power factor 0.8

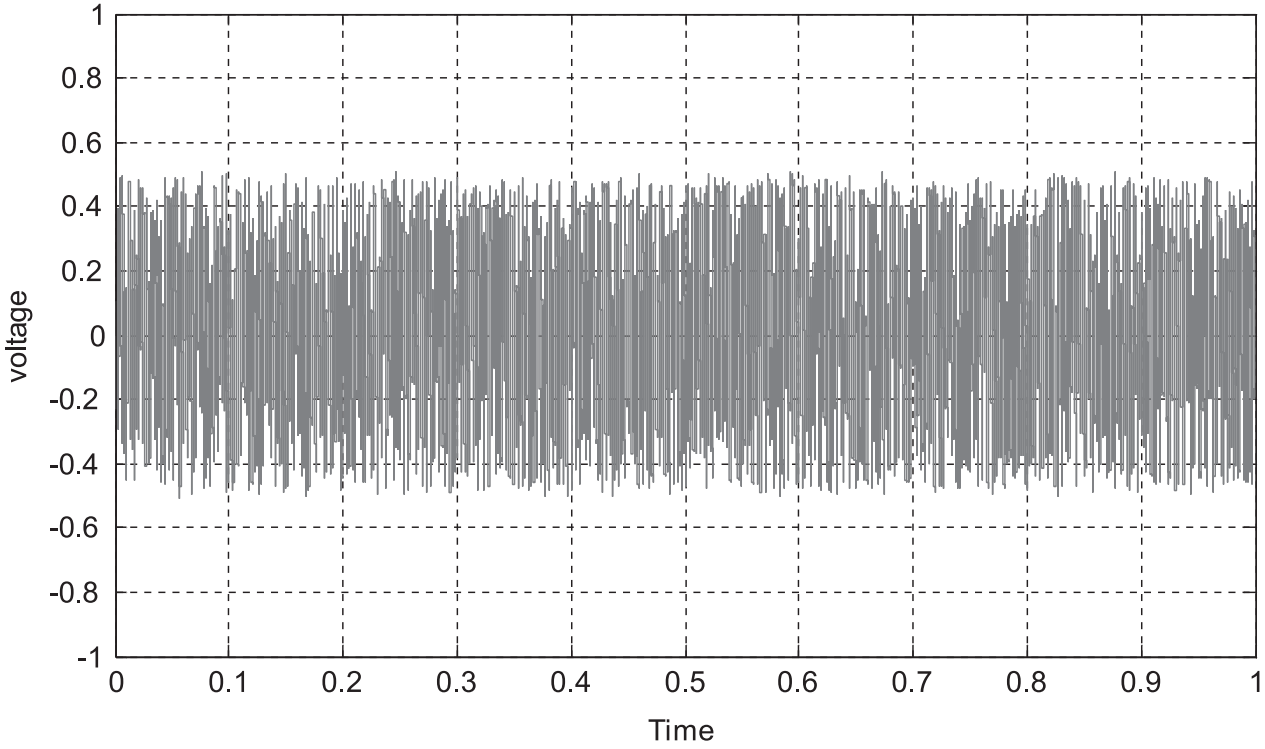

Figure 19: Neutral point voltage at Power factor 0.8

3. **Difference in initial capacitor voltages**: Though the capacitors of the same voltages and power are taken, they have differences due to manufacturing tolerances. These causes different charging periods of the capacitor. Thus capacitor voltage change. This condition is checked in the simulation by applying initial capacitor voltage difference of 40v shown in Fig's (20 - 23).

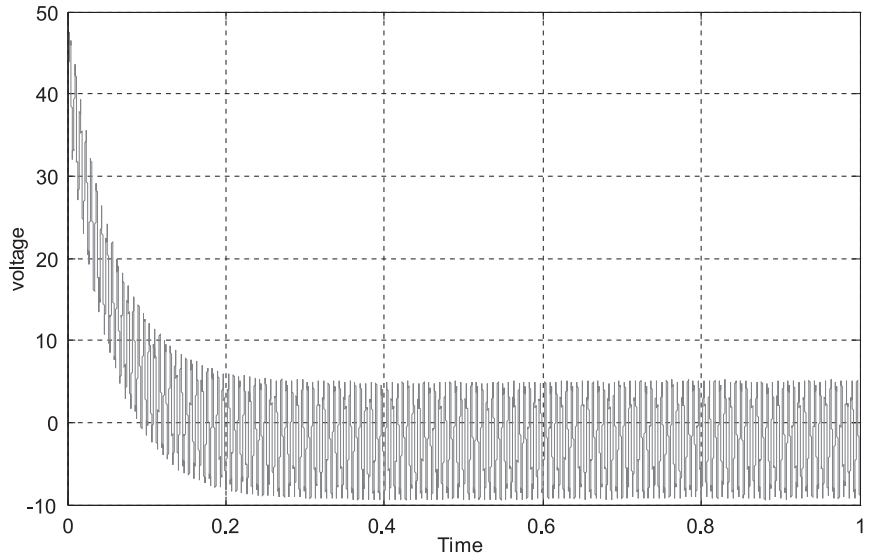

Figure 20: Neutral point voltage when initial voltage of capacitor C1=100v

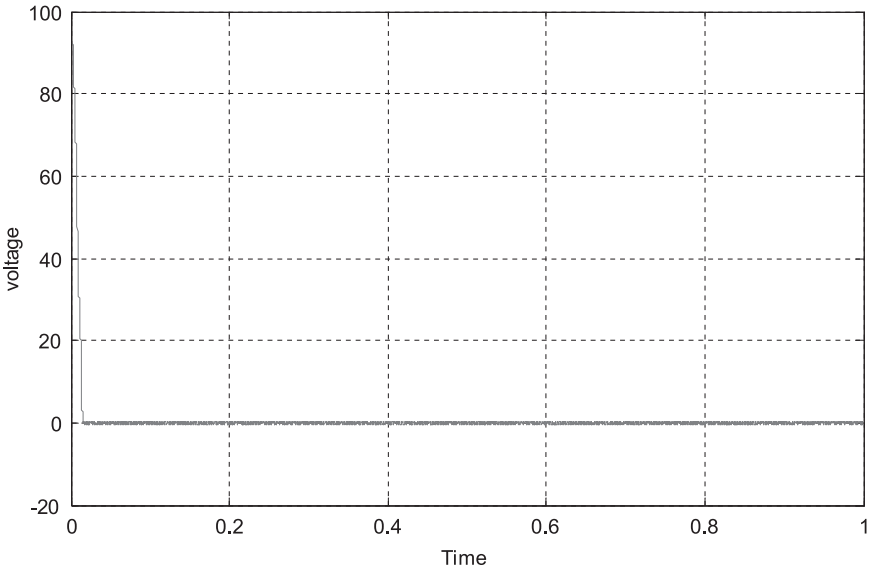

Figure 21: Neutral point voltage when initial voltage of CapacitorC1=100v

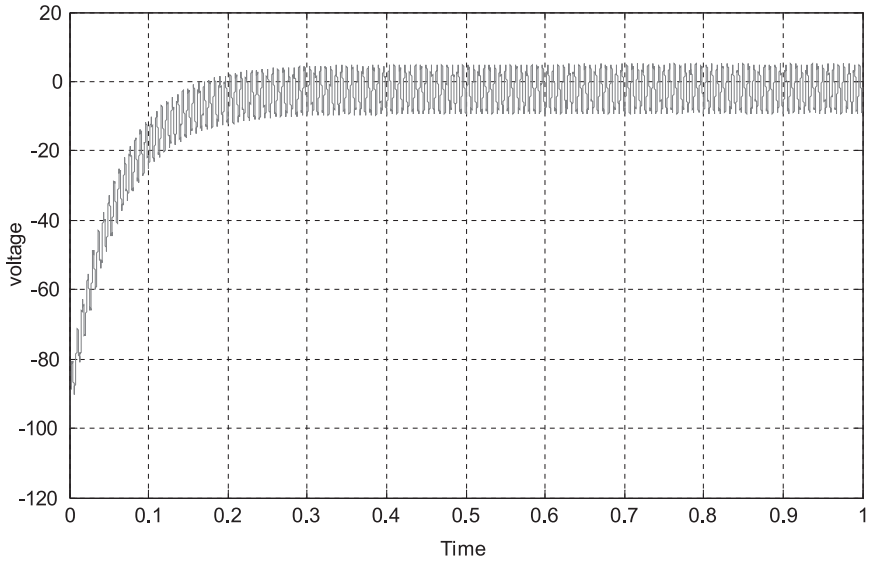

Figure 22: Neutral point voltage when initial voltage of capacitorC1=100v, C2=60v

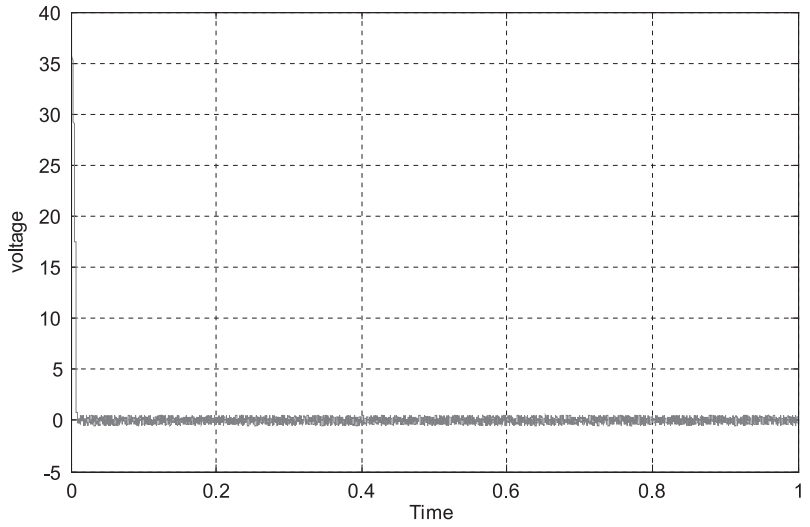

Figure 23: Neutral point voltage when initial voltage of CapacitorC1=100v, C2=60

4. The balanced load is applied on inverter of about 100 Ω, 10 mH, 1000 Ω is applied on the inverter. The output voltages at unity power factor and respective THD's are shown below.

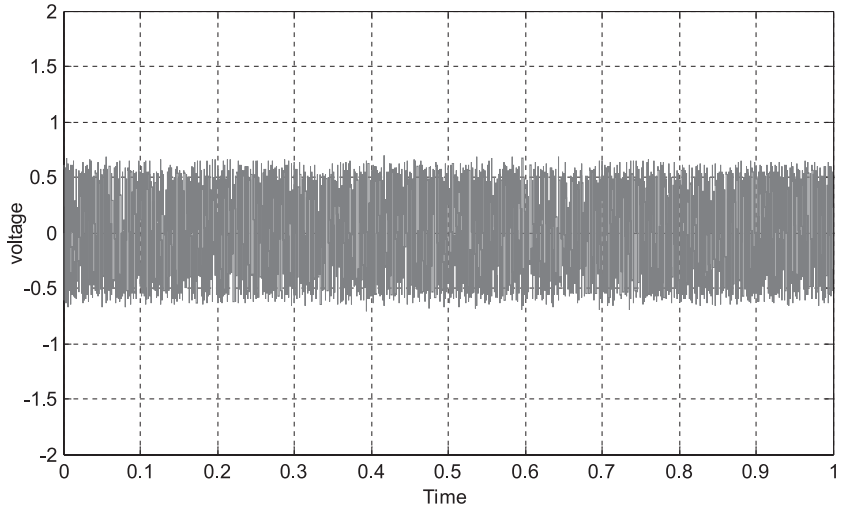

Figure 24: Neutral point voltage with balanced load

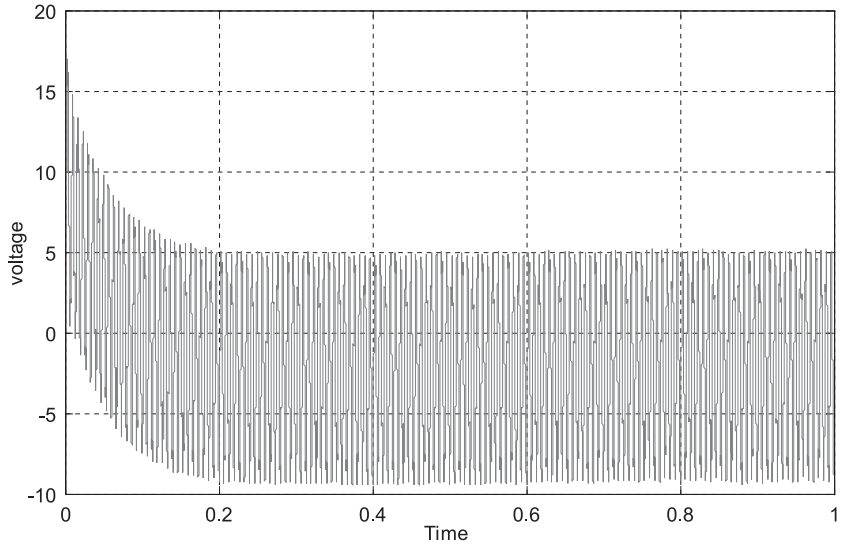

Figure 25: Neutral point voltage at balanced load

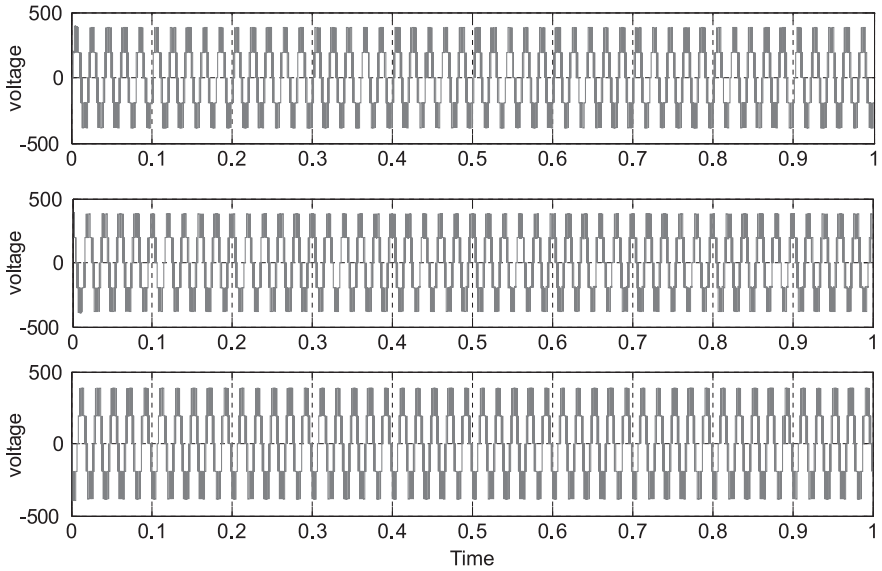

Figure 26: Three level NPC inverter output voltage without Feedback at unity Power factor

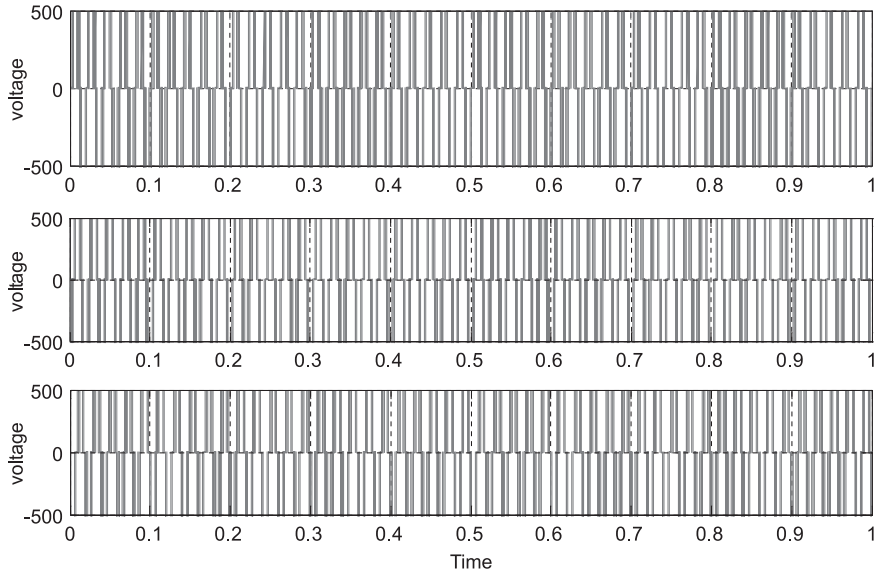

Figure 27: Three level NPC inverter output voltage with Feedback at unity Power factor

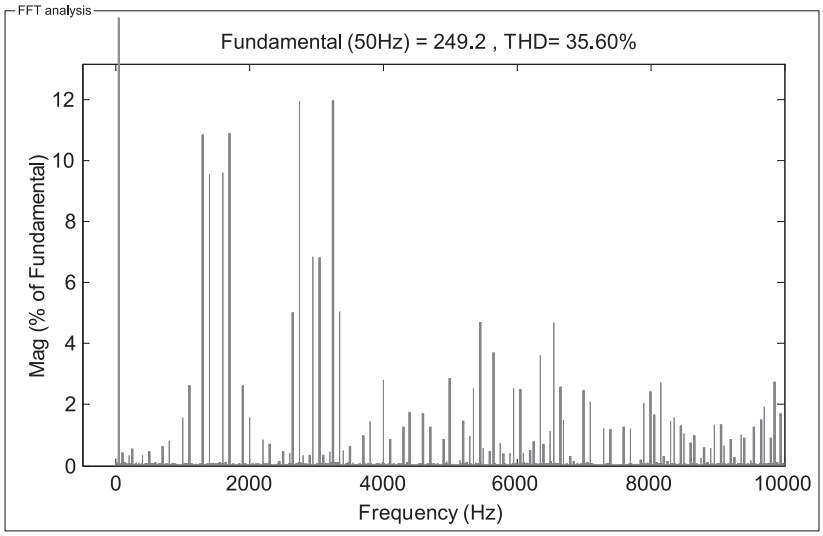

Figure 28: THD analysis of SPWM figure

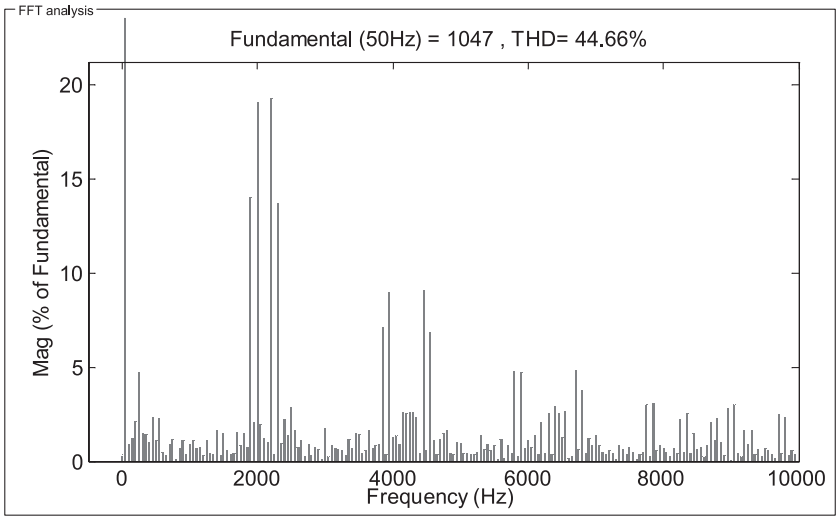

Figure 29: THD analysis of proposed technique

8. HARDWARE RESULTS

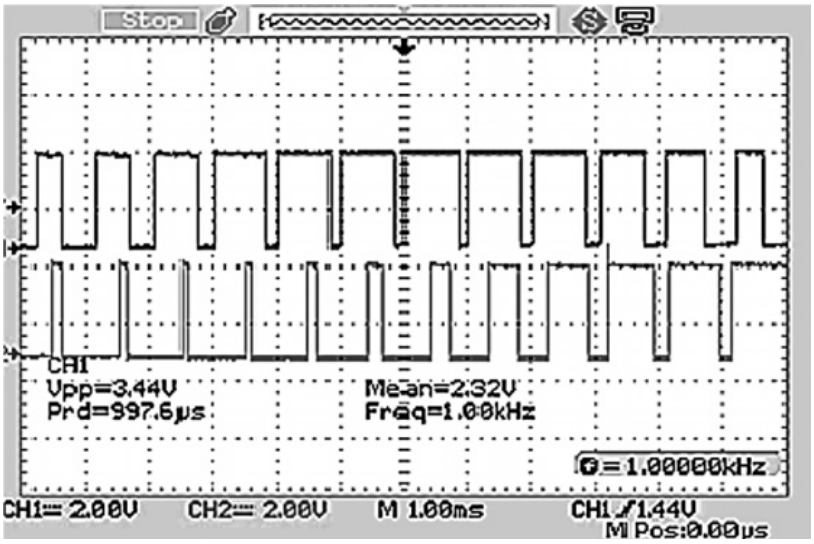

Figure 30: Sine PWM pulses at switching frequency 1 KHz, 1 KHz, Sine = 50Hz with phase shift (0^o and 120^o)

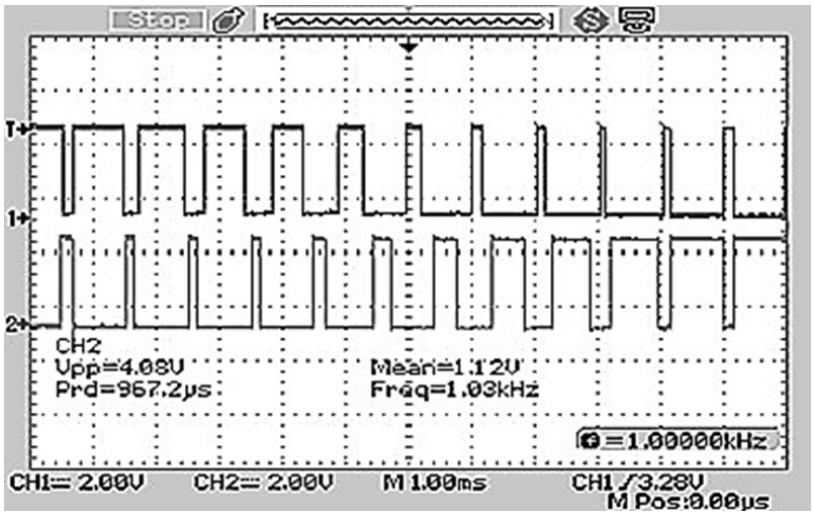

Figure 31: Sine PWM pulses at switching frequency 1 KHz with phase shift, sine=50Hz(0^o and 240^o)

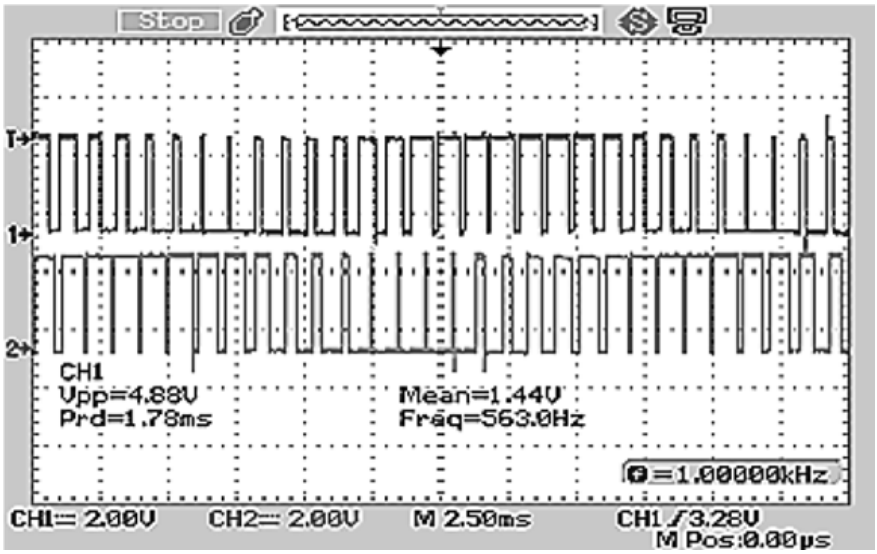

Figure 32: Sine PWM pulses at switching frequency 1 KHz with complementary (ePWM1A and ePWM1B)

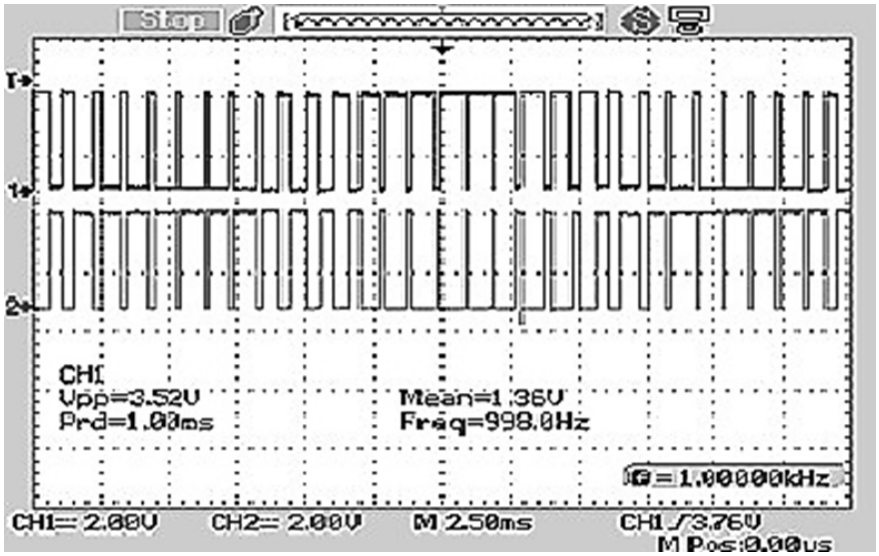

Figure 33: Sine PWM pulses at switching frequency 1 KHz with complementary (ePWM2A and ePWM2B)

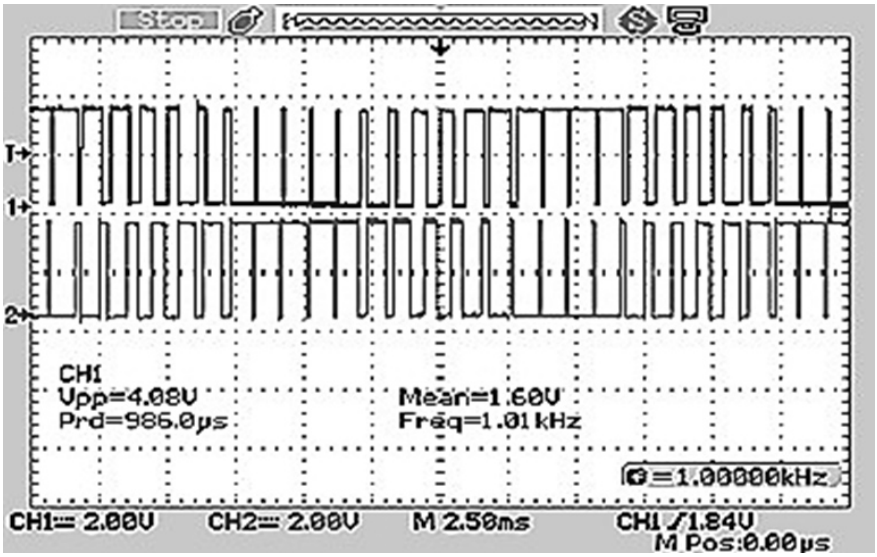

Figure 34: Sine PWM pulses at switching frequency1 KHz with Complementary (ePWM3A and ePWM3B)

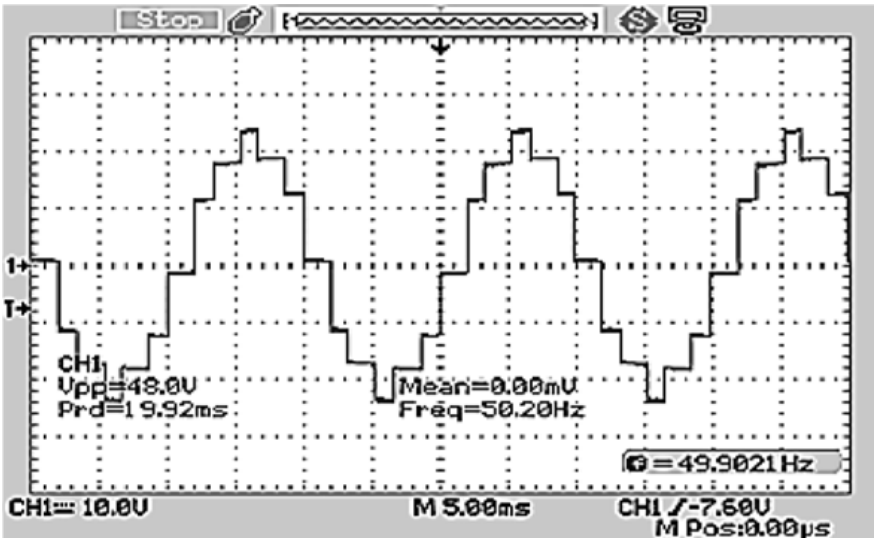

Figure 35: Open loop three level DCMLI output voltage Waveform with three phase R-Load

9. CONCLUSION

In this paper, design and implementation of proposed level shifted carrier PWM technique for Three-level neutral point clamped inverter is presented .It can be observed that neutral point voltage is stabilized for various power factors, unbalanced load and capacitor tolerances. It is analyzed that reduction in neutral point voltage of proposed technique is more compared with conventional SPWM at different aspects. With the proposed technique is simple and effective it reduces harmonic content in output and neutral point oscillations. The. Simulation Practical results are also provided to verify the implementation of approach of Matlab/Simulink and DSP based proposed PWM scheme. Practical open loop three level neutral point clamped inverter supplying 3KW load is developed and tested in the laboratory using DSPTMS320F28335 board programmed with code composer studio

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