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A 280μW High Gain Inductively Degenerated LNA for Medical Radio Communication

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ABSTRACT

An ultra-low power, high gain inductively degenerated common source (IDCS) LNA for medical radio (MedRadio) communications in the frequency band of 401–406 MHz is implemented using 0.18–μm technology. An upsurge LNA is designed for biomedical applications with an emphasis on the covenant between gain, noise and power consumption. The IDCS LNA operates in subthreshold region which extremely reduces the power consumption and relaxes the voltage headroom without screwing the LNA performance. The relaxed voltage headroom concedes current-reuse technique to implement single to differential (SD) LNA or to stack mixer on top of LNA. The proposed LNA achieves power gain (S_{21}) of 21 dB, S_{11}& S_{22} are much less than -10 dB, NF of 2.1 dB and P_{1dB} of -18 dBm while consuming 280 μA current from a 1-V supply voltage. The overall pre and post layout simulations of proposed LNA shows acceptable agreement with theoretical predictions. The layout occupying 0.587 mm^2. The gain enhancement and reduction in power has been optimized compared with previous works implies that LNA obtains the highest figure of merit.

Keywords: Low Noise Amplifier (LNA), IDCS topology, MedRadio, Current-reuse technique, Optimum noise & power.

1. INTRODUCTION

The Federal Communication Commission (FCC) has introduced medical radio communications (MedRadio) in the frequency range of 401-406 MHz, which is a wireless communication standard specially dedicated for wearable and implantable medical devices (Example: pacemakers, defibrillators and brain machine interface (BMI), and so on). MedRadio is having ten 300-kHz (402-405) and twenty 100-kHz (401-402 & 405-406) bandwidth channels. There are many other bands available for medical devices like ISM (*industrial, scientific and medical*), which is using by many other applications, so more possibility of interference. FCC has allocated separate band to provide reliable, continuous and cost-effective health monitoring in hospitals and homes. Medical devices must meet low power consumption to enhance the battery life.

A top level link budget analysis and specifications of LNA are crucial for wireless medical communication given in Table 1.

The application scenario of implantable medical device isshown in Fig.1.The RF communication link between sensor and base stationis to operate within a room or hospital with a distance of 1-10 m.

Most of the proposed techniques of LNA for MedRadio communication use fully differential topology [3-5]. Though there are plenty advantages with fully differential, it is suffering from use of an additional balun at its input side. Balun usually increases both area and power. The low power operation is achieved

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Table 1
Link budget analysis of MedRadio, [1] & [2].

Parameter	*Value*
Free Space Path Loss (FSPL)	44.6 dB
Effective Isotropic Radiated Power (EIRP)	– 16 dBm
Minimum Received signal power	– 93.6 dBm
Front-end Noise Figure	8 dB
Power Consumption	≤ 500μW
IIP3	≥ -25 dBm

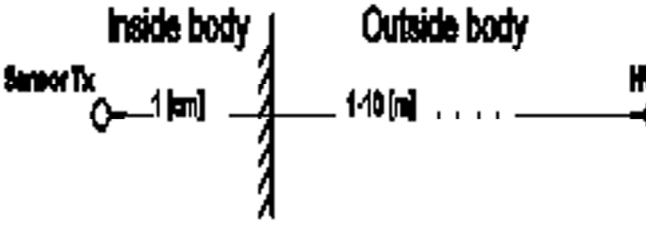

Figure 1: Application scenario of an implantable medical device.

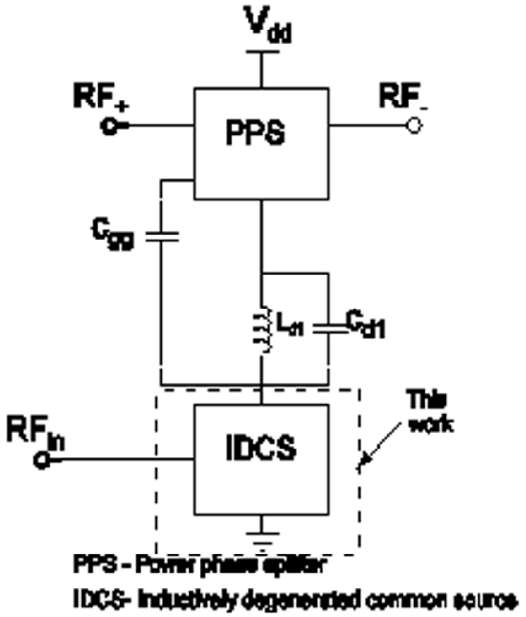

Figure 2: Block diagram of SD LNA for medical radio communication.

using stacked architecture to re-use the current by stacking mixer on top of the LNA [6] or can be used to implement SD LNA which avoids the use of balun as shown in Fig.2. But this approach have resulted in high supply voltage which causes for high power consumption. So IDCS topology should consume very less power. Bulk driven CMOS technique is also good choice to reduce the power consumption, but it demands for double twin-well process.

It is challenging task to reduce the power consumption of LNA without compromising on any other parameters. Subthreshold region RF CMOS is a good choice for designing low power LNA. In subthreshold region transition frequency (f_t) and IIP_3 may be effected, but in MedRadio IIP_3 is relaxed as given in Table 1. In this work we have focused on designing of LNA using subthreshold region of operation at optimum noise and power. Section II describes the basic theory of subthreshold region and modelling of RF inductors. Section III describes the implementation of IDCS topology at optimum noise and power. Section IV shows thesimulation results of both pre & post layout and comparison withthe existing designs. Section V concludes this work.

2. PRELIMINARY

2.1. Subtheshold region of RF CMOS

Current leakages are ever present in electronic systems, and many forms of leakage are considered by engineers to be unusable. This thinking is starting to change as new frontiers in ultra-low power begin to be

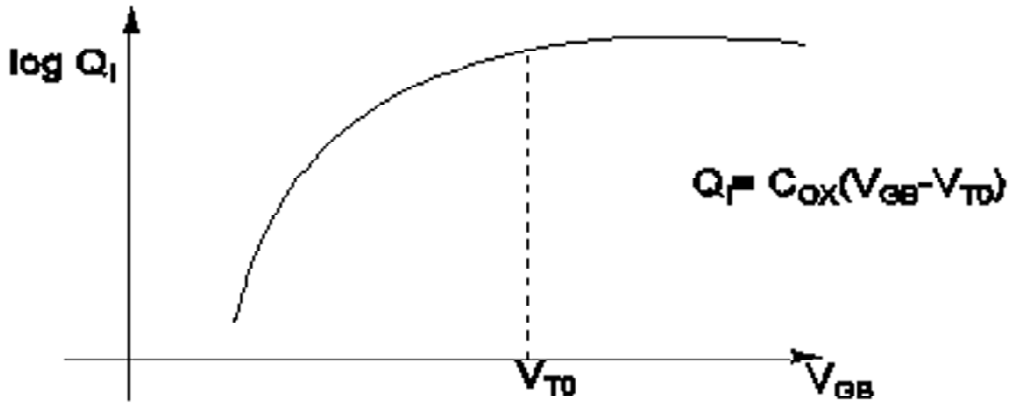

Figure 3: Charge variation below threshold voltage [13].

exploited through precise control of sub-threshold leakage currents of MOSFET devices for analog applications. A finite (nonzero) current does flow in a MOSFET even for gate voltages below the threshold voltage and this effect is more marked for short channel length devices than their long channel counterparts. In strong inversion region MOSFET model makes the assumption that the inversion charge Q_I goes to zero when the gate voltage drops below the threshold voltage. But this is not true below V_t, the channel charge drops exponentially with decreasing gate voltage as shown in Fig. 3.

In subthreshold region current is due to diffusion of carriers given by [7]

$$I_D = \frac{2\mu_n C_{ox} V_T^2}{K} \exp\left[\frac{-KV_{T0n}}{V_T}\right] \frac{W}{L} e^{\frac{KV_G}{V_T}} \left[e^{\frac{-V_s}{V_T}} - e^{\frac{-V_D}{V_T}}\right] \quad (1)$$

Where K is kappa constant varies from 0.6 to 0.8, V_T is thermal voltage and V_G, V_D and V_S are gate, drain and source voltages respectively.In subthreshold region there is possibility to get high g_m over I_D, which is much needed to reduce noise figure. Though g_m over I_D values are higher than strong inversion region, the value of g_m is smaller. Here g_m cannot be increased by increasing W/L values, but it happens if current density is kept constant. In subthreshold region g_m can be given as [7]

$$g_m = \frac{KI_D}{V_T} \quad (2)$$

2.2. Modelling of RF inductors

In designing LNA for RF frequencies, selection of inductors should be done at most care. Since quality factor and internal resistance of these inductors will affect the both gain and noise figure of entire circuit. RF inductors are mainly characterized by number of turns, width and diameter of each turn. So before selecting inductor we should do the basic simulation to know its internal resistance and quality factor. Usually RF inductors have a third terminal to change inductance through external voltage. If it is not using we have connect it to ground. RF inductors are characterized by connecting a current source in parallel to it. Now we have to look in to the ac response of impedance. Usually inductor has some internal resistance and parasitic capacitance, so it resonates at some frequency. From the impedance response we can easily find resistance and quality factor.

3. CIRCUIT IMPLEMENTATION

3.1. Inductively Degenerated Common Source (IDCS) topology

In all types of receivers Low Noise Amplifier is the first amplifying block. Apart from amplification it is responsible for other important parameters of receiver like noise figure (NF), linearity and maximum power

transfer. LNA receives signal from antenna whose impedance is 50 ohms. So to receive maximum power from antenna input impedance of LNA should match with antenna. This is the primary goal of every designer in LNA design. There are many techniques available to match the impedance as reported in [8].

An inductively degenerated common source topology provides the noiseless impedance matching without using physical resistance. The circuit diagram is shown in Fig.4.Assume that I_{in} is flowing entirely through C_{GS}, then gate to source voltage is $I_{IN}/(sC_{GS})$ and hence drain current of $g_m I_{IN}/(sC_{GS})$. These two currents flow through L_{deg}, producing a voltage

$$V_P = \left(I_{IN} + \frac{g_m I_{IN}}{sC_{GS}} \right) sL_{\deg} \tag{3}$$

Since $V_{IN} = V_{GS} + V_p$, we have

Interestingly the input impedance contains a frequency independent real part given by $\frac{g_m L_{\deg}}{C_{GS}}$. Thus the second term can be chosen equal to 50 ohm. Note that Inductively degenerated common source (IDCS)topology is very popularbecause of its superior noise performance i.e., the inductive degeneration is ideally noiselessand the RF input signal is pre-amplified by the input matching series resonant network.In basic IDCS topology it is not possible to achieve impedance matching at optimum noise and power. There are different optimization techniques in IDCS topology as reported [9]. In power constrained simultaneous noise impedance matching (PCSNIM), an additional capacitor is added in parallel to C_{GS} so that the value of L_{deg} can be reduced. In this technique the input matching network resonates with L_{deg} and C_t.

$$\omega_0 = \frac{1}{\sqrt{L_{\deg} C_t}} \quad where \; C_t = C_{ex} + C_{GS} \tag{5}$$

C_{ex} should not be more than four times of C_{GS} otherwise the value of noise factor increases proportionally. So to avoid this difficulty an additional inductor is added at the gate of transistor so that we can have freedom on C_{ex}.

Now input impedance of the circuit is given as

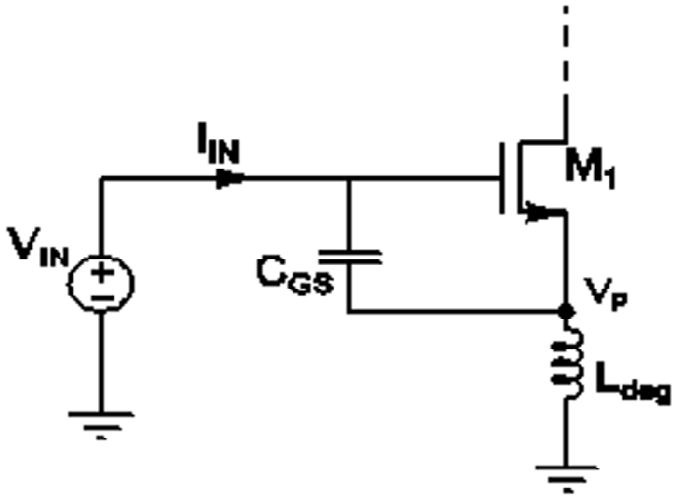

Figure 4: Basic IDCS topology [14].

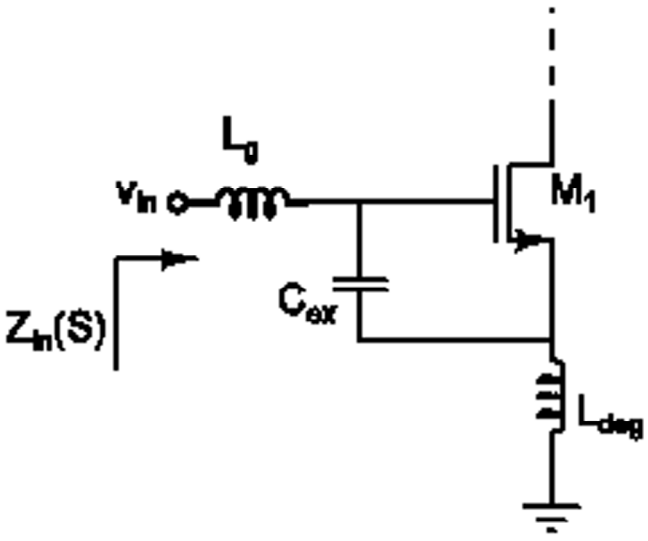

Figure 5: IDCS topology with noise and power optimization [7].

$$Z_{in}(s) = \frac{1}{sC_t} + s\left(L_{\deg} + L_g\right) + \frac{g_m}{C_t} L_{\deg} \tag{6}$$

Where
$$C_t = C_{GS} + C_{ex} \text{ and } \omega_0 = \frac{1}{\sqrt{\left(L_{\deg} + L_g\right) C_t}} \tag{7}$$

At $\omega = \omega_0$, $R_T = R_s = \frac{g_m}{C_t} L_{\deg}$. Here adding L_g gives an additional freedom to set ω_0 and R_T (terminal impedance) independently. Noise figure of IDCS transistor M_1 can be calculated as [10]

$$\text{Noise factor } (NF) = 1 + \frac{\omega_0}{\omega_t} \gamma \frac{g_{d0}}{g_m} \frac{1}{2Q_{in}} \left(1 - 2cX_d + \left(4Q_{in}^2 + 1\right) X_d^2\right) \tag{8}$$

Where γ is excess noise coefficient, ω_t is transistor transitionfrequency, ω_0 is the operating frequency, g_{d0} is trans-conductanceat $V_{DS} = 0$, c is the noise correlation factor of gateand drain, Q_{in} is the quality factor of input RLC networkwhich is equal to

$$Q_{in} = \frac{1}{2\omega_0 C_t R_s} = \frac{\omega_0 \left(L_{\deg} + L_g\right)}{2R_S} \tag{9}$$

$$\text{and } X_d = \frac{g_m}{g_{d0}} \sqrt{\frac{\delta}{5\gamma}} \tag{10}$$

In "(8)" we can observe that Nf is mainlydecided by $\frac{\omega_0}{\omega_t}$ ratio and rest of the second term, which iscalled as noise scaling factor (NSF).At fixed biasing point NSF varies with Q_{in} and c values. So selection of Q_{in} value directly affects the Noise factor. For 180 nm technology the value of c is -j 0.55 [1]. In this design, we have chosen Q_{in} value is 8 andsupply voltage of 1 V. The main advantage of this technique ispassive amplification provided by input RLC network, which is Q_{in} times of v_{in} apart from active amplification (i.e., $g_m v_{in} R_{load}$).

3.2. Proposed LNA

The circuit diagram of proposed LNA is given in Fig. 6.

Here R_B and C_B are chosen such that noise of I_B and M_B are isolated.Since all parameters of LNA are interdependent, so fixing the component values is very difficult. In the literature PCSNIM and folded cascode techniques [9] have restricted the quality factor of the input matching network to 5. In the proposed architecture there is a freedom on quality factor because of the subthreshold region of operation. This allows us to choose higher values for Q_{in}. A good start must be required to avoid the multiple iterations in the designing. So here we have given a successful designing procedure as shown in Fig. 7. The best way of starting design is with load tank and follow as per the flowchart. While selecting quality factor of input matching network we should take care of NSF, $f_t (f_0 << f_t$ is desired) and similarly selection of W/L should not affect any other parameters of LNA.

4. SIMULATION RESULTS

This design has been studied in detail and optimized throughcareful investigation and extensive simulation in UMC 0.18-μm CMOS technology to produce results which are compared with existing

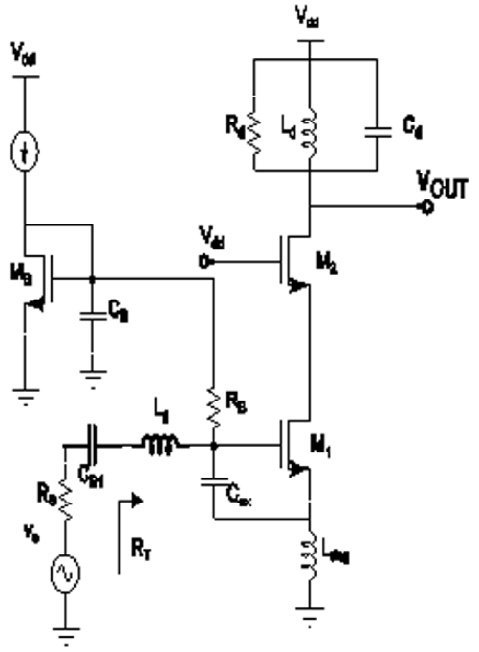

Figure 6: Proposed subthreshold PCSNIM IDCS LNA.

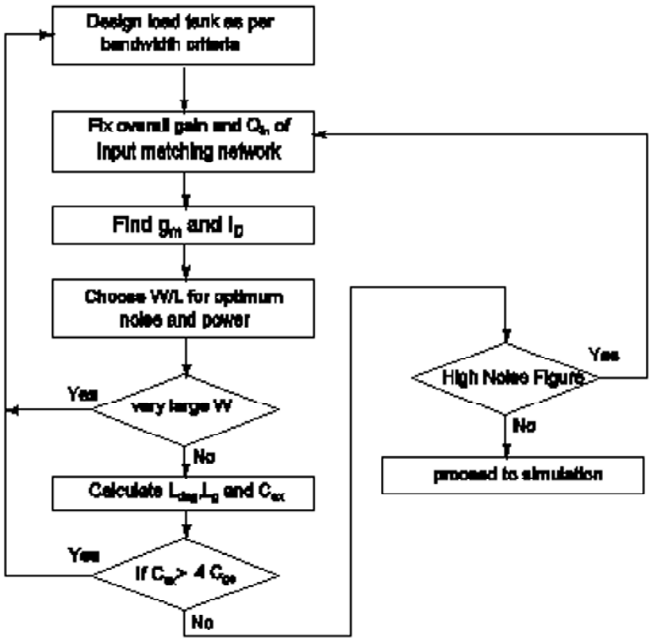

Figure 7: Design flowchart of subthreshold PCSNIM IDCS LNA.

designs as reported in Table 2.Here we have shown both pre and post (extracted) layout results. The power gain (S_{21}) and reverse isolation (S_{11}) are shown in Fig. 8 and Fig. 9 respectively. The power gain of post layout simulation is almost half of the pre layout simulation. This is mainly due to R and C extraction which increases the load resistance, but the voltage gain of pre and post layout simulation are almost same. As we know that if load impedance does not match with the source impedance then actual power gain is

$$S_{ij}^{1} = S_{ij}\frac{\sqrt{Z_j}}{\sqrt{Z_i}} \tag{13}$$

Where Z_i and Z_j are output and input impedances respectively. The noise figure and stability analysis of simulations are shown in Fig.10 and Fig.11 respectively. The extracted NF is around 3.1 dB which is including NF of buffer at the output. As per Stern stability analysis,the stability factor (K_f) should be >1 for unconditional stablesystem. The layout of proposed technique and simulation of input referred 1-dB compression point (P_{1dB}) are shown in Fig. 12 and Fig. 13 respectively.

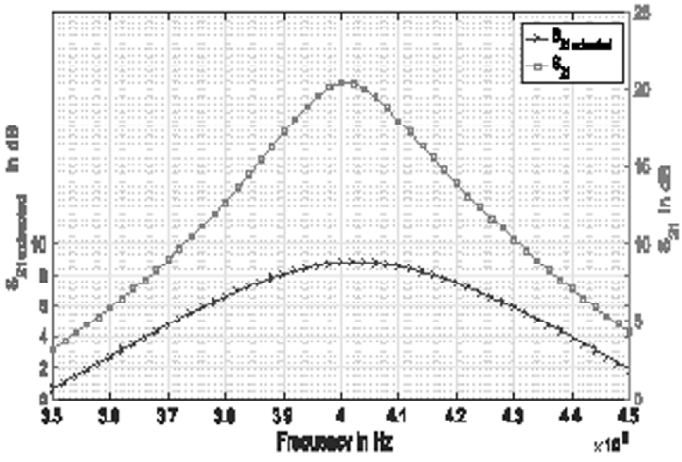

Figure 8: Analysis of power gain (S_{21})

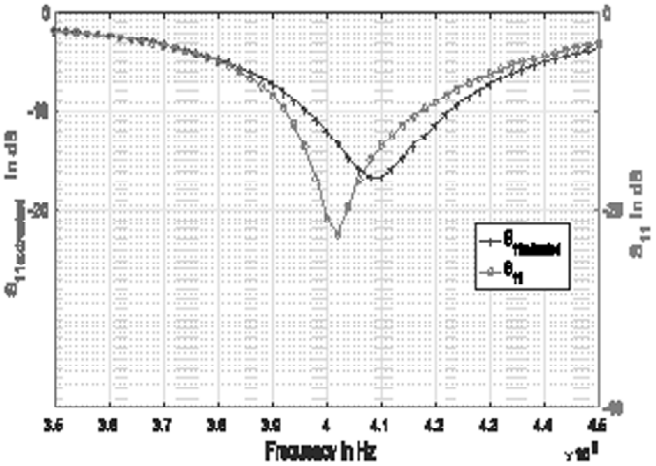

Figure 9: Analysis of Impedance matching (S_{11})

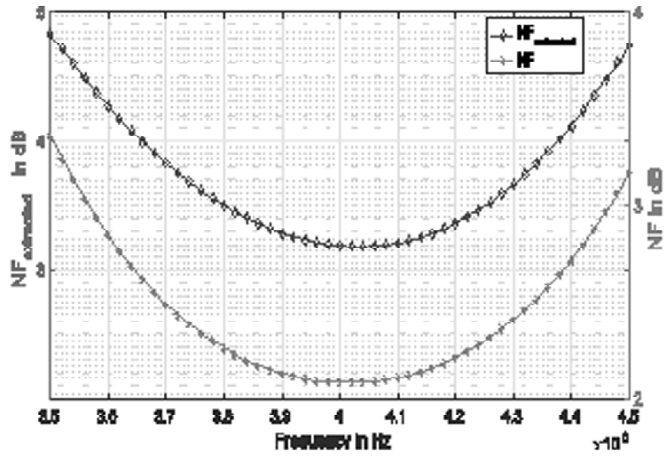

Figure 10: Analysis of Noise Figure.

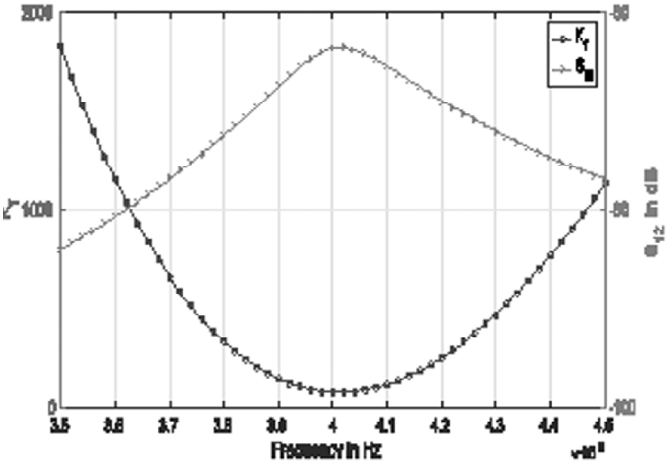

Figure 11: Stability analysis.

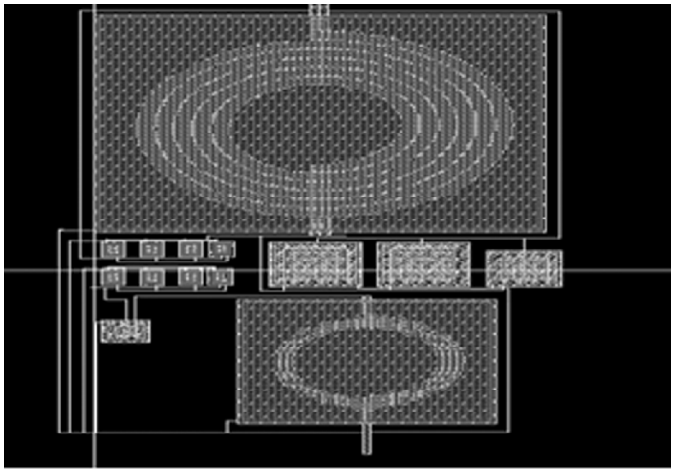

Figure 12: Layout of proposed LNA (L_g taken as an external component).

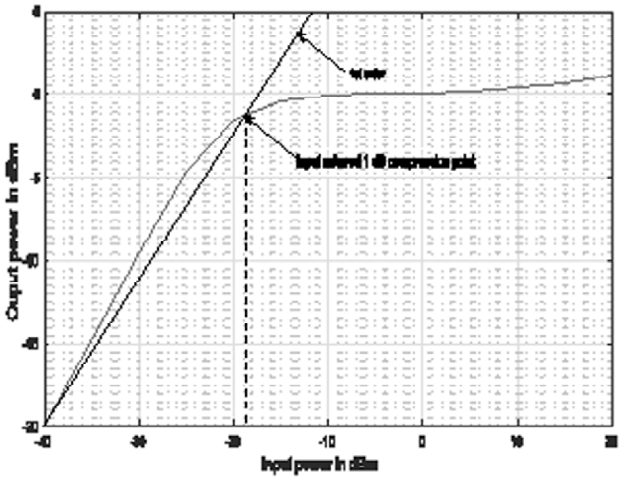

Figure 13: Calculation of 1-dB compression point.

Table 2
Performance comparison of Low noise amplifier.

Work	Technology (μm)	Frequency (MHz)	Power gain (dB)	Noise Figure (dB)	Power dissipation (mW)	IIP_3 (dBm)	Figure of Merit***
[11] Pre-Layout	0.36	401-406	23^	4	3.59	—	0.01
[9] Measured	0.25	900	12	1.3	2	-4	2.03
[10]Measured	0.6	1500	22	3.5	30	-9.7	0.05
[1]Measured	0.18	401-406	20	2.8	0.15	-8.1	4.57
[12]Pre-Layout	0.18	1200	18.75^	2.52	1.926	-19.69*	0.73
[15] Post-Layout	0.18	402-405	15	11.6	1.6	-26	0.0026~
[16] Post-Layout	0.18	401-457	29^	5	0.37	-19.5	0.833~
This Work Pre-Layout Post-Layout	0.18	401-406	21	2.1	0.28	-18*	4.11
	0.18	401-406	20^	3.2	0.28	-18*	2.3

^ Voltage gain * P_{1dB}~RF front-end $IIP_3 = P_{1dB}$ + 10dB assumed [1] & [7].

$$***\text{Figure of Merit} = = \frac{Gain[Abs.]11P_3[mW]}{P_{DC}[mW](NF-1)[Abs.]}.f[GHz] \quad (14)$$

5. SUMMARY AND CONCLUSION

We have demonstrated ultra-low power LNA using subthreshold PCSNIM techniquefor narrow-band applications using UMC 0.18-µmCMOS process. An inductively degenerated common sourcetopology has been used as basic technique to match the inputimpedance with noise and power optimization. The mainassets of this topology except narrow-band of operation areimpedance & noise optimization at low power and passiveamplification from input matching network. The gain loss dueto sub-threshold biasing is compensated by input matchingnetwork. This kind of IDCS LNA is most suitable for current re-use techniques.The proposed LNA achieves power gain (S_{21}) of 21 dB, S_{11} and S_{22} are less than -10 dB, NF of 2.1 dB and P_{1dB} of -18 dBm while consuming 280 µA current from a 1-V supply voltage.There is a scope to reduce the power furtherby increasing Q_{in} and (or) reducing the width of transistor.This effects the NF and linearity performance, butthese parameters are relaxed in MedRadio specifications. The proposed method can also be tuned (5-6 GHz) for wireless body area networks (WBAN), commonly used in biomedical facilities such as equipment to assist heart rate monitoring, diagnosis, and drug delivery.

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