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Analyzing the Effect of Voltage Variation in a Thin-Film Transistor with Silicon

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ABSTRACT

In this paper, high-performance poly-Si TFT with $ZrTiO_4$ as gate dielectric material under optimized MILC silicide material has been analyzed. The EOT of the dielectric use is 4.1 nm. The electrical performance of this setup attained a low value for threshold voltage of -2 V and a steep SS of 1.70E+00 V/dec. These properties thus obtained pose to be the best performance properties of the poly-Si TFT with high-K gate dielectric material that is ZTO.

***IndexTerms*:** TFT, ZTO, MILC, EOT

1. INTRODUCTION

In VLSI, the topic of major concern is the methods that can be adopted to improve the performance and increase the miniaturization of the MOS devices. For the last forty years, the gate dielectric material being used is Silicon Dioxide since it provides a continuous improved performance as it is scaled down which also improves the performance of MOS device. This continuous scaling, for the last few years, has resulted in the continuous increase in the power dissipation which poses to be a serious issue [1-2]. The gate dielectric material, Silicon Dioxide, scaling has reached to a limit that further scaling will lead to an increase in the direct tunneling effect, power consumption, etc. [2-4]. Gate dielectric thickness of MOSFET device for the Scaling has been presented according to the prediction of ITRS in the following figure1 [5]

It is clear from the roadmap that with the continuous scaling of the gate-dielectric material there is a continuous increase in the gate leakage currents, so to resolve this problem of leakage currents alternative

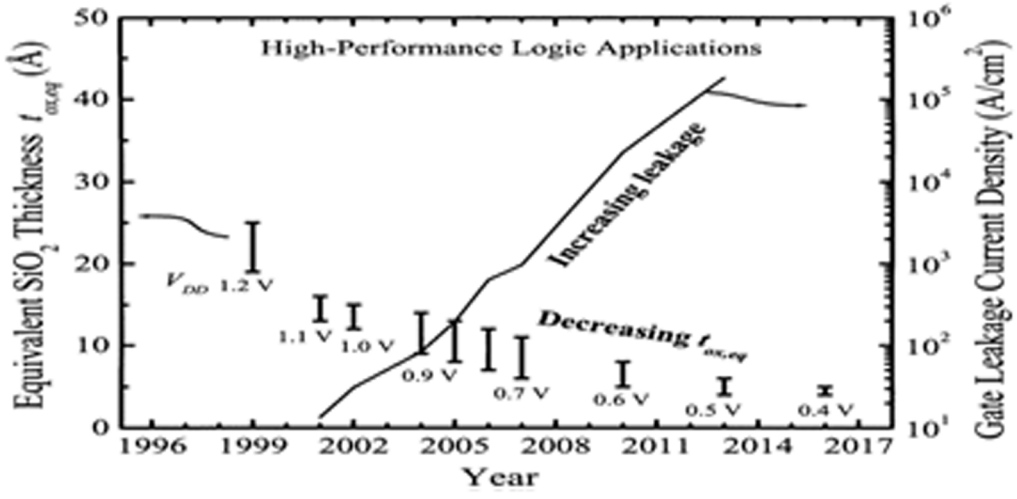

Figure 1: Scaling Trends of MOSFET gate dielectric thickness [5]

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dielectric materials with high dielectric constant are being investigated to find a proper replacement of Silicon Dioxide.

Thin-film transistor (TFT) is a type of Field Effect Transistor (FET) which has been widely employed in various displays as these provide high driving current. To overcome the limitations of poly-Si TFT with SPC channel and scaled Silicon Dioxide gate dielectric, metal- oxide gate dielectrics with high-k dielectric constants have been investigated. Some of them are HfO_2, $HfSiO_2$, Al_2O_3, Pr_2O_3, $LaAlO_3$, Y_2O_3, Eu_2O_3 and $PrTiO_4$. All these candidates proved themselves unsuitable in one way or the other. The high-K dielectric material that can be used should have high dielectric constant, band-gap matching with poly-Si, and low cost elements. All these requirements have been obtained from $ZrTiO_4$ (ZTO) as its dielectric constant is higher (50.5), band alignment is also in acceptable form and highly good thermal stability with poly-Si [6-8]. Figure 2 shows the proposed cross-section of poly-Si TFT with high- K gate dielectric material like ZTO [6].

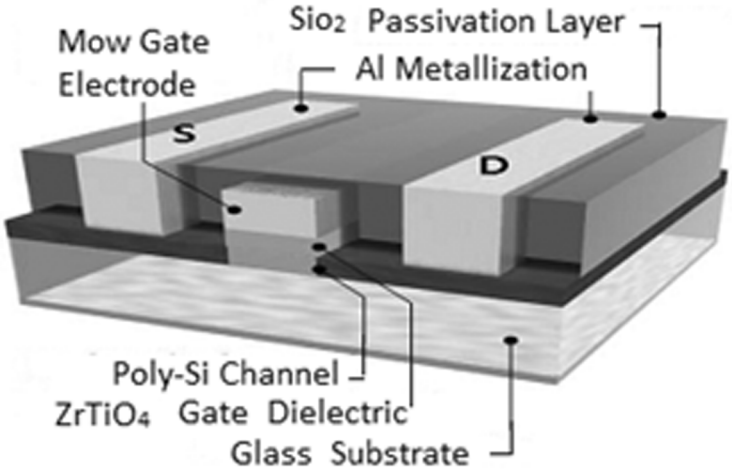

Figure 2: Cross-section of proposed poly-Si TFT [6]

2. EXPERIMENTAL WORK

The cross-sectional view of the poly-Si TFT with ZTO dielectric is being shown in the figure 2. For better performance, the optimization is done in two parts, first, by optimizing metal induced crystallized material and second, the dielectric optimization with ZTO. Initially, at a temperature of about 500 ºC a 50-nm thick amorphous-Si is deposited by LPCVD. Sputtering is done to deposit 5-nm thick $NiSi_2$ nanoparticle seeds. Then annealing is done at temperature of about 550 ºC by ambient H_2 for 2 hours for MILC process. In MILC, alpha silicon film layers are used for managing the Ni functionality with silicide seeds and crystallization method has been optimized. Alpha Si films are selected with thickness of 100-nm along with SiO_2 layer structure with 200nm thickness. This setup is simulated at temperature of 450 degree with low chemical vapor process with corning glass. Threshold voltage roll-off functionalities and electrical characteristics are tested with the proposed poly-Si TFT with ZTO material under optimized MILC silicide material.

3. RESULTS AND DISCUSSIONS

The simulations are done by using software Microwind3.1. The variation in length has been made with the values of 8, 10, and 15 μm with a fixed width of 4μm. The variation in the threshold voltage roll-off and electrical characteristics has been studied on the basis of a) Voltage vs Voltage, b) Voltage vs Current, and c) Voltage vs Time.The voltage versus time simulation is done to obtain the transient analysis of the available signals. Here the simulations are done between the nodes SL and inv_invD with SL and WL as two clocks or pulses provided to the transistor.

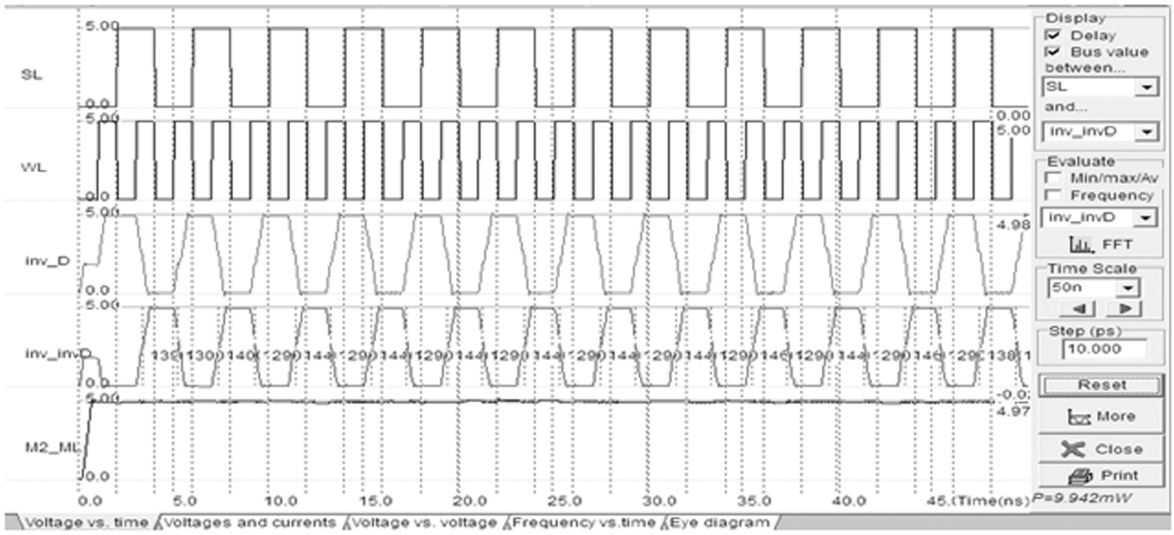

Figure 3: Voltage vs Time Curve

The results shown in the figure 3 show that the overall performance of the device has increased due to the decrease in the net delay at the output node.

Voltage vs Voltage simulation is done to obtain the transfer characteristics of the selected nodes. In this mode, the inverter characteristics have been calculated and also the values of the stop node and start node from 0 to V_{DD} are calculated.

The results shown in figure 4 depict that the total voltage obtained at the output node is much efficient. It depicts that the efficiency of the device has increased remarkably with low leakage and low power dissipation.

Further, the proposed results we have obtained are being compared with the existing results. From this comparison in figur 5, we have found that there is an increase in the threshold voltage roll-off in the

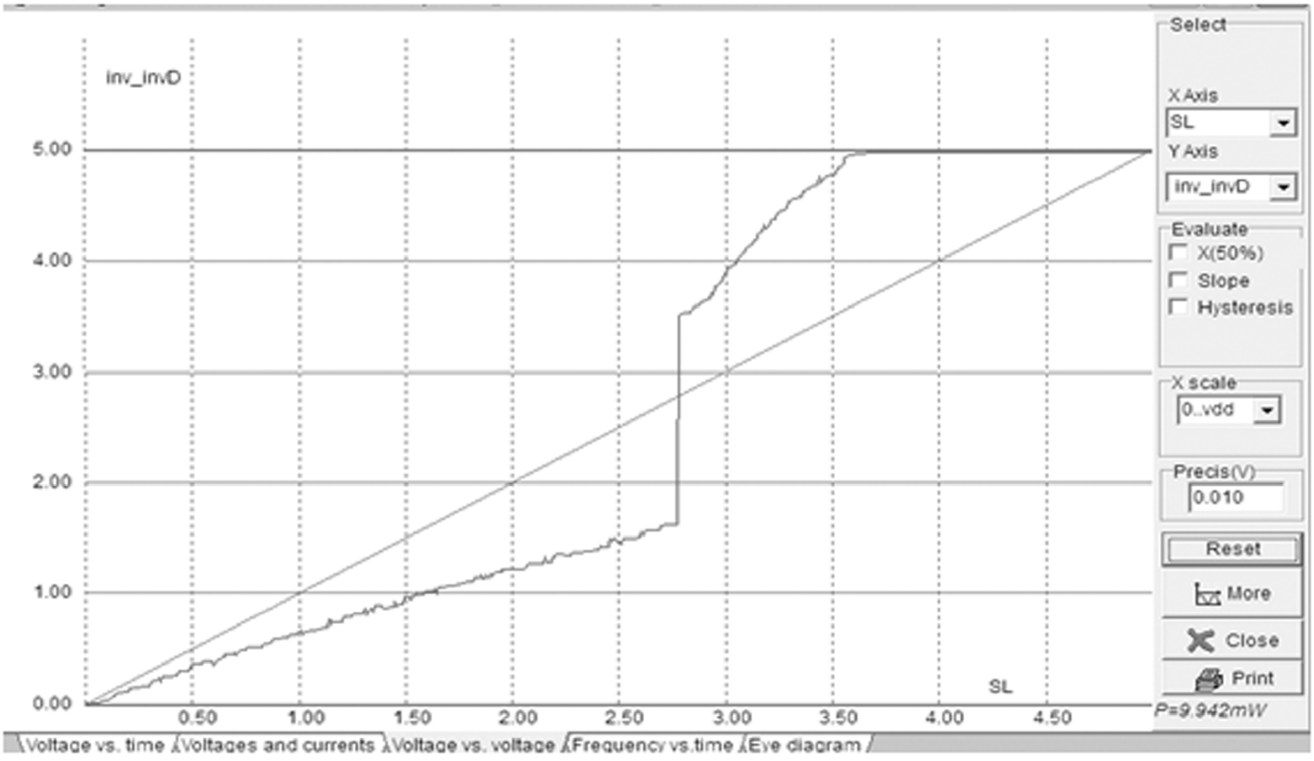

Figure 4: Voltage vs Voltage Curve

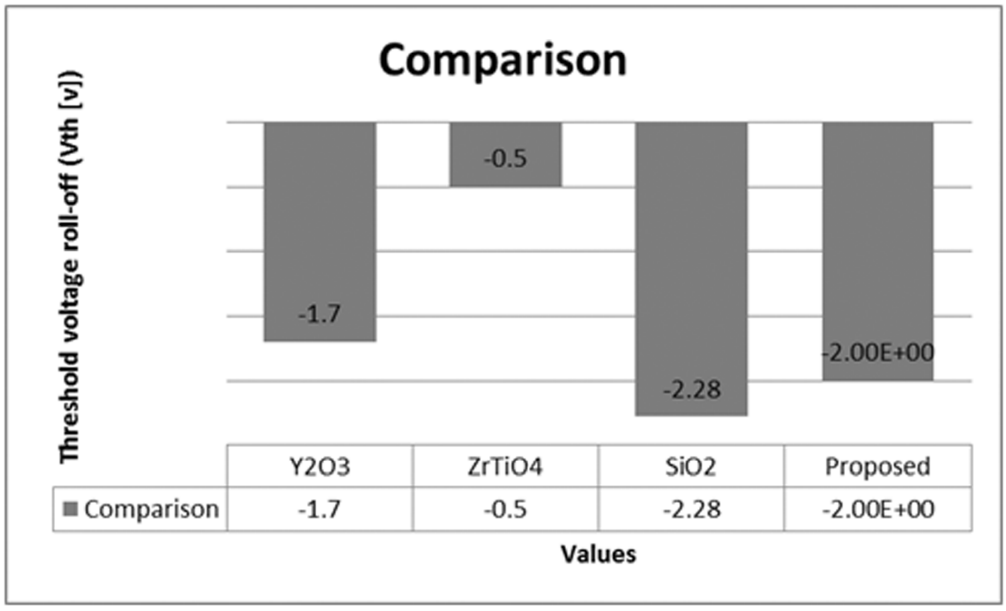

Figure 5: Vth roll-off properties comparison

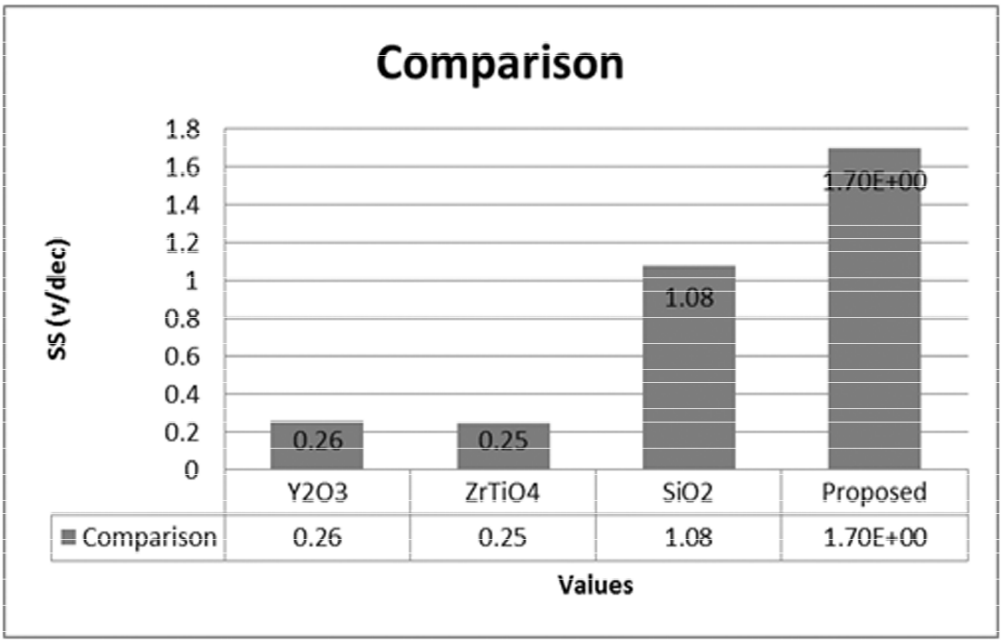

Figure 6: Electrical properties on steep comparison

proposed work from the earlier one. Hence the decrease in the leakage current and the power dissipation has been observed.

Figure 6 describes the comparison in the electrical properties on the basis of SS (V/dec). The graph shows the advancement in the SS of the proposed work. That is, subthreshold conduction is 1.7V per 10 times of the total drain current flowing through the device. In other words, the average subthreshold current has decreased resulting in the improvement in the performance of the MOS device.

4. CONCLUSION

This paper is concluding performance of poly-Si TFT with high- K gate dielectric material ZTO under optimized MILC silicide material with a dielectric thickness of 4 μm and channel length have been varied from 8, 10, and 15μm has been studied. This setup exhibited a low Vth of -2 V and steep SS of 1.70 V/dec.

The increase in the suppression of voltage roll-off has also been observed and was found very effective. These results obtained from the setup of poly-Si TFT with high-K gate dielectric material under optimized silicide material can thus be concluded as the best performance of the poly-Si TFT in comparison to the poly-Si TFT with high-K gate dielectrics used till now.

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