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ANOVEL NINE-LEVEL INVERTER FORMED BY FLOATING CAPACITORS

B. Prathap Reddy[*], K.Sreekanth Reddy[**] and Shrish Gupta [***]

Abstract: In this paper, a novel single-phase, nine-level inverter topology with floating capacitors is presented. The proposed topology which can produce nine voltage levels in the output with minimum number of diodes, driver circuits and switches as compare to normal nine-level cascaded type of multilevel inverter. The proposed topology can enhance the power quality, minimizing the switching losses and produce high quality voltage waveforms with nine no. of levels. Additionally, the proposed topology can be worked at all load power factors. Another advantage of this proposed inverter is used for reactive power compensation. The examination of the model is finished by method for computer simulation by using MATLAB/SIMUL- INK. This novel inverter has low common-mode voltage variation and dv/dt.

Key Words: Cascaded H-Bridges, floating capacitors, nine-level cascaded inverter, MATLAB.

1. INTRODUCTION

With the advantage of multilevel converters, the execution of high and medium power applications motor drives are varied in drastic manner [1], [2]. The common type of multilevel converters are the cascaded H-Bridge inverter [4], the flying capacitor inverter (FCI) [3], the Diode clamped inverter [5]. In the diode clamped inverter [5], more number of dc voltage sources are produced by dividing the single dc bus voltage with capacitors banks. This topology having more number of clamping diodes and having the limitation of dc bus capacitor unbalance in case of more voltage levels[6],[7].

The diode clamped inverter can operated in a limited modulation period is present in [8]. The idea of FCI was proposed in 1992 [4]. In this topology various capacitors of various magnitudes are used to produce more voltage levels. The features of this type of topology are modularity, no use of clamping diodes, free of unbalance in dc bus capacitors, etc. [9]. Also, in the diode clamped inverter type, single source is used to produce more number of pole voltage levels. In [10], [11] more number of topologies are presented for balancing the capacitor voltages. However, producing the more levels of voltage in FCI needs more number of capacitors. In [12], [13] more number of levels have produced by cross connecting the capacitors using extra switches. The operation of FCI with asymmetrical capacitor voltages are generates voltage levels haveproposed in [14]. Multilevel inverters are power Electronic converters, they produce a appropriate AC voltage output waveform from different dc sources as inputs [15].

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To produce a qualitative output current and voltage with less quantity of ripple content, they requiring high carrier frequency along with various PWM strategies. In high-power and high-voltage applications, these two level inverters, however, have some limitations in operating losses and device ratings. Now a days, multilevel inverters are utilized in high and medium power applications such as flexible AC transmission system (FACTS) [16], industrial motor drives [17], traction electric vehicle applications, drive systems [18] and so on. If the no. of levels in output voltage increases, which is approximately equals to sinusoidal wave with less harmoniccontent, also improves the performance of the drive presentedin [19]. The workpresented in [20] generates multiple voltage levels by switchingthe load current through capacitors. Here, the voltage through the capacitors can be maintained at desired value by changing the direction of load current through the capacitor by choosing the redundant states for the same pole voltage.

In this present paper, a new structure of 9-level inverter is formed by cascading three-level inverter with floating capacitors. This inverter can produce more no. of levels by using minimum number of diodes, IGBTs and gate driver circuits.

2. CONVENTIONAL NINE-LEVEL INVERTER

The structure of conventional nine-level inverter is shown in Figure 1. In this topology, every switch having an IGBT and one anti-parallel diode. The output voltage wave form of conventional system is shown in Figure 2.By on and off the IGBT switches in an appropriate sequence we were produce a synthesized ac output waveform from the input dc. There are five different modes are possible every half cycle based on which switches are in conduction. The output current depends on the type of load like RL or R.

Mode 1: During this mode the switches S_1, S_2, S_5, S_6, S_9, S_{10}, S_{13} and S_{14} are in on state. The load is short circuited i.e. output voltage is zero.

$$V_o = 0 \tag{1}$$

Mode 2: During this mode the switches S_1, S_4, S_5, S_6, S_9, S_{10}, S_{13} and S_{14} are in on state. And the load current flows in the upper first bridge.

$$Vo = V \tag{2}$$

Mode 3: During this mode the switches S_1, S_4, S_5, S_8, S_9, S_{10}, S_{13} and S_{14} are in on state. And the load current flows in the upper two bridges through on state switches.

$$Vo = 2V \tag{3}$$

Mode 4: During this mode the switches S_1, S_4, S_5, S_8, S_9, S_{12}, S_{13} and S_{14} are in on state. And the load current flows in the upper three bridges through on state switches

$$Vo = 3V \tag{4}$$

Mode 5: During this mode the switches S_1, S_4, S_5, S_8, S_9, S_{12}, S_{13} and S_{16} are in on state. And the load current flows in all bridges through on state switches

$$Vo = 4V \tag{5}$$

Mode 6: During this mode the switches S_2, S_3, S_5, S_6, S_9, S_{10}, S_{13} and S_{14} are in on state. And the load current flows in the upper bridge through on state switches.

$$Vo = -V \tag{6}$$

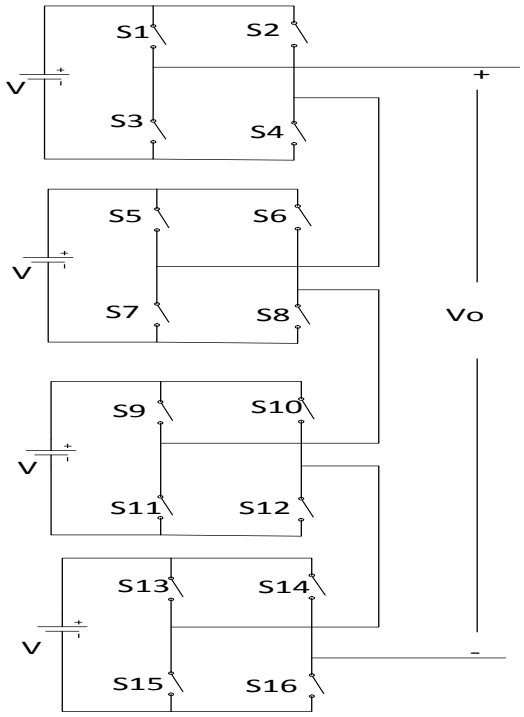

Figure 1. The Conventional System Arrangement.

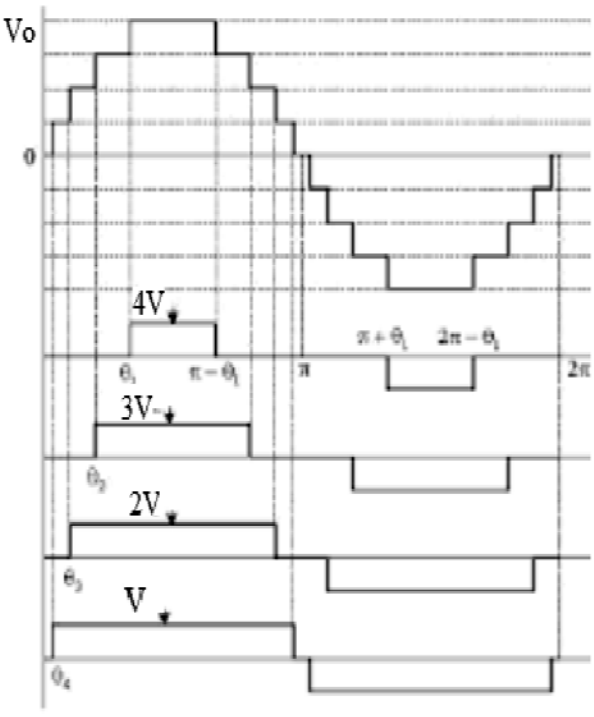

Figure 2. Conventional System Output Wave Form

In a same manner the negitive output voltages we will get from negative of input voltage state and zerovoltage states obtained by turning on the appropriate opposite switches.

The Table 1 defines the various switching states of conventional nine-level inverter. Switches S1 and S3 or (S2 and S4) should not be turned on simultaneously. Otherwise, the dc source is shorted for a certain period i.e. dead zone period takes place.

Table 1.
Conventional Nine-level inverter Switching states

Mode	*On state switches*	*Output voltage*
1	S1,S2,S5,S6,S9,S10,S13,S14	0
2	S1,S4,S5,S6,S9,S10,S13,S14	V
3	S1,S4,S5,S8,S9,S10,S13,S14	2V
4	S1,S4,S5,S8,S9,S12,S13,S14	3V
5	S1,S4,S5,S8,S9,S12,S13,S16	4V
6	S2,S3,S5,S6,S9,S10,S13,S14	-V
7	S2,S3,S6,S7,S9,S10,S13,S14	-2V
8	S2,S3,S6,S7,S10,S11,S13,S14	-3V
9	S2,S3,S6,S7,S10,S11,S14,S15	-4V

3. PROPOSED NINE-LEVEL INVERTER

The proposed topology of nine-level inverter is shown in Fig. 3. In this network topology, every switching device having one diode and an IGBT (or anti-parallel diode) also for one leg of any one H-Bridge re connecting the one capacitor and one small resistor are connected across each switch. The proposed structure gives a quality output current and voltage with less ripple content. For reactive power compensation also this proposed structure is used.

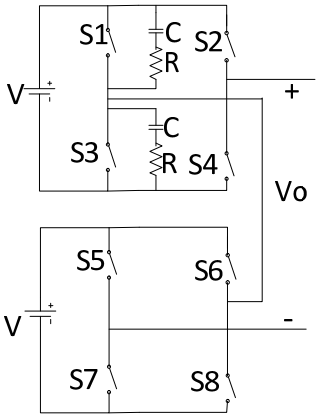

Figure 3. Proposed topology of Nine-level inverter,

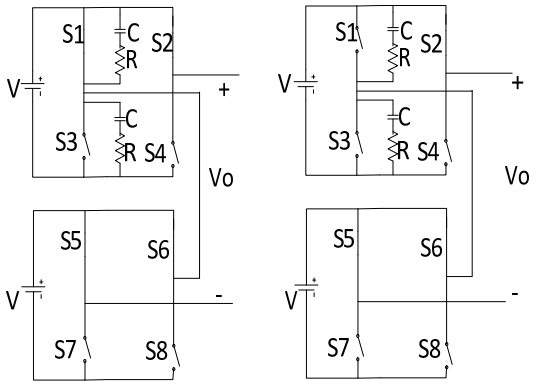

Figure 4. Equivalent networks of Mode1 and Mode 2

By producing more number of levels in this proposed converter, the power rating of inverter can be improved without any need of high ratings power electronic devices. The unique topology of this proposed nine-level inverter is help full to generating high voltages with reduced harmonic content without any use of cascade connected switching devices or transformers. As the no of output levels increases, the harmonic content of the output voltage reduces symmetrically. The proposed network output voltage wave form is follows as in Figure 3. The output of proposed system is same as conventional system with less magnitude and limited to 2V. Here also nine various modes depends on their switches are operated. The equivalent nine modes of this topology are followed by Figure 4 to Figure 8. The output current depending on the type of load like as R or RL.

Mode 1: During this mode the switches S_1, S_2, S_5 and S_6 are in on state. The load is short circuited i.e. output voltage is zero.

$$Vo = 0 \tag{7}$$

Mode 2: During this mode the switches S_2, S_5 and S_6 are in on state and remaining are in off state. And the load current flows through C- S6-S5-Load-S2-C.

$$Vo = V/2 \tag{8}$$

Mode 3: During this mode the switches S_2, S_3, S_5 and S_6 are in on state and remaining are in off state. And the load current flows through S2-V-S3-S6-S5 -Load-S2.

$$Vo = V \tag{9}$$

Mode 4: During this mode the switches S_2, S_6 and S_7 are in on state and remaining are in off state. And the load current flows through S2-C-S6-V-S7-Load-S2.

$$Vo = 3V/2 \tag{10}$$

Mode 5: During this mode the switches S_2, S_3, S_6 and S_7 are in on state and remaining are in off state. And the load current flows through S2-V-S3-S6-V-S7-Load-S2.

$$Vo = 2V \tag{11}$$

Mode 6: During this mode the switches S_4, S_5 and S_6 are in on state and remaining are in off state. And the load current flows through C-S4-S5-S6-Load-C.

$$Vo = -V/2 \tag{12}$$

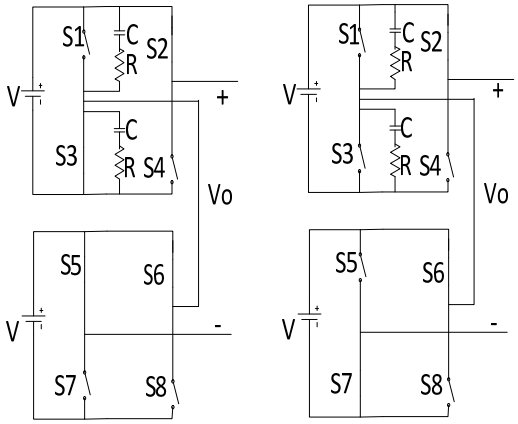

Figure 5. Equivalent networks of Mode 3 and Mode 4.

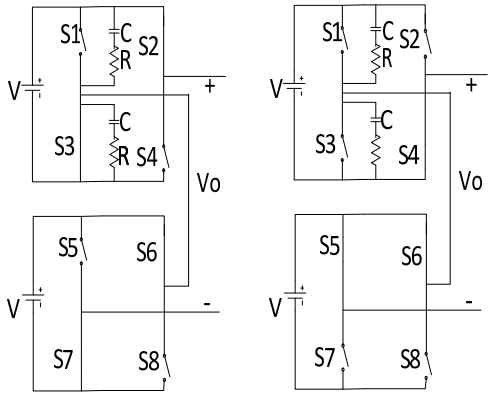

Figure 6. Equivalent networks of Mode 5 and Mode 6

Mode 7: During this mode the switches S_1, S_4, S_5 and S_6 are in on state and remaining are in off state. And the load current flows through S4-V-S1-S6-S5-Load-S4.

$$Vo = -V \tag{13}$$

Mode 8: During this mode the switches S_4, S_5 and S_8 are in on state and remaining are in off state. And the load current flows through S4-V-C-S8-V-S5-Load-S4.

$$Vo = -3V/2 \tag{14}$$

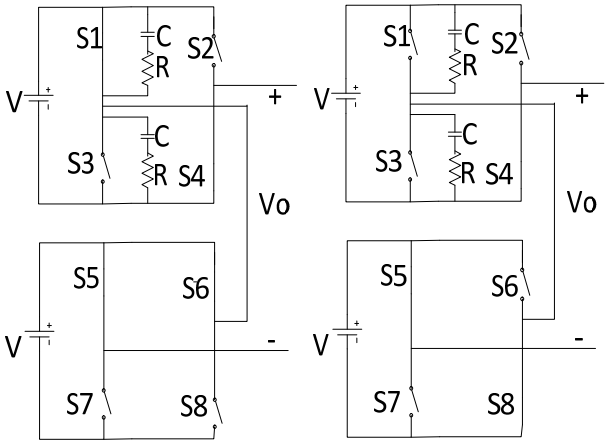

Figure 7. Equivalent Networks of Mode 7 and Mode 8

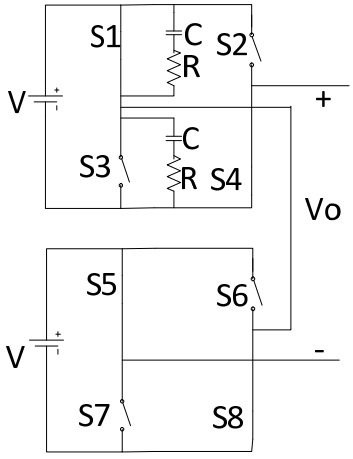

Figure 8. Equivalent Network of Mode 9

Mode 9: During this mode the switches S_1, S_4, S_5 and S_8 are in on state and remaining are in off state. And the load current flows through S4-V-S1-S8-V-S5-Load-S4.

$$Vo = -2V \quad (15)$$

And this output cycle will comes continuously. The table 2. Defines the various switching modes of proposed nine-level inverter.

Table 2
Proposed nine-level inverter Switching states

Mode	*On state switches*	*Output voltage*
1	S1,S2,S5,S6	0
2	S2,S5,S6	V/2
3	S2,S3,S5,S6	V
4	S2,S6,S7	3V/2
5	S2,S3,S6,S7	2V
6	S4,S5,S6	-V/2
7	S1,S4,S5,S6	-V
8	S4,S5,S8	-3V/2
9	S1,S4,S5,S8	-2V

4. COMPARISON OF PROPOSED NINE-LEVEL TOPOLOGY WITH CONVENTIONAL TOPOLOGY

The conventional nine-level converter generates the quality current and voltage waveform with reduce amount of ripples, However in high-power applications, these conventional topologies have certain limitations like switching conduction losses and power electronic device ratings. The proposed nine-level inverter topology gives a improved voltage and current output with minimum amount of ripple content by using only two sources and eight switches. Also proposed converter is helping for reactive power compensation. With the help of this proposed structure it's easier to generate a high power, high voltages due to the voltage stress across each and every switch is controlled. The drawbacks of conventional nine-level converter are overcome with the help of proposed structure. Table 3 defines the comparison of both proposed and conventional topologies.

Table 3 .Comparison of both conventional and proposed nine-level network topologies

Parameters	*Conventional Topology*	*Proposed topology*
Number of output levels of voltage	9	9
THD	30%	22%
Voltage stresses across switches	high	Low
No of dc sources	4	2
No of switches	16	8
Electromagnetic interference	high	Low
dv/dt ratio	high	Low
Switching losses	high	Less

5. SIMULATION RESULTS

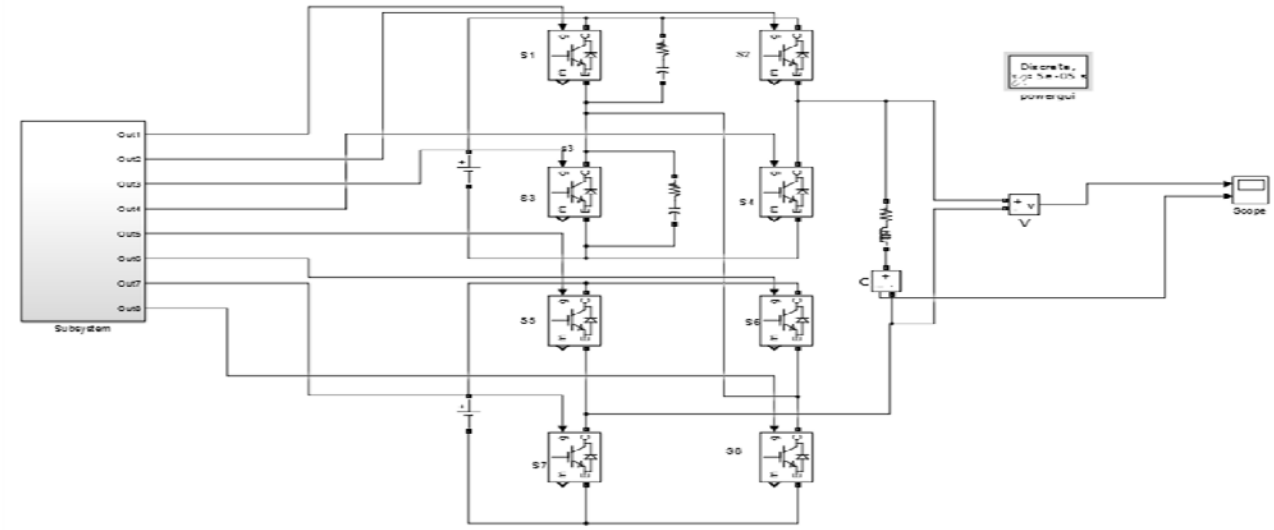

Figure 9. Simulation model of proposed nine-level inverter

In this part, the MATLAB software is used for simulation and design of proposed nine-level topology. Figure 9, Figure 10 and Figure 11 gives the results of proposed inverter i.e. output current and output voltage respectively. The total harmonic distortion (THD) is a popular performance index which estimates the amount of harmonic content is presented in the output waveform for the power converters. The proposed inverter is having two supply sources as DC with a magnitude of 100V. A load which have been taken as the R-L load (R = 1Ω and L = 100mH) for simulation purpose. The switches are IGBT's with internal diodes and having internal resistance of 1m Ω.

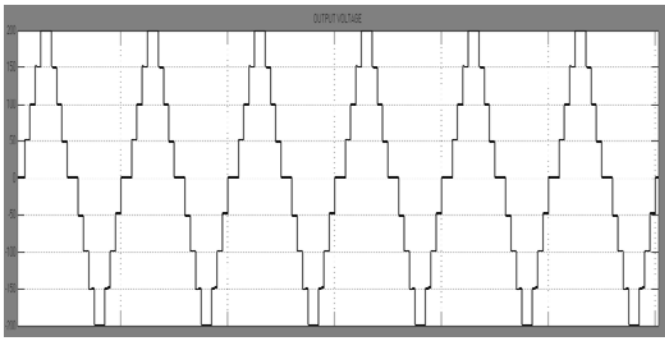

Figure 10. Output voltage wave form of proposed topology

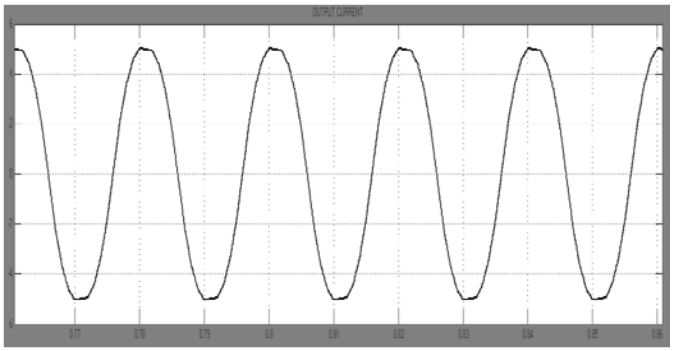

Figure 11. Output current wave of proposed nine-level converter

There are various modulation techniques introduced for multilevel inverters like stepped modulation, space vector PWM, SPWM, trapezoidal modulation and modified reference with multi carrier waveforms, Genetic algorithms, Hysteresis modulation method. The Figures 12 & 13 are defines the harmonic spectrums of output voltage and output currents of proposed structure.

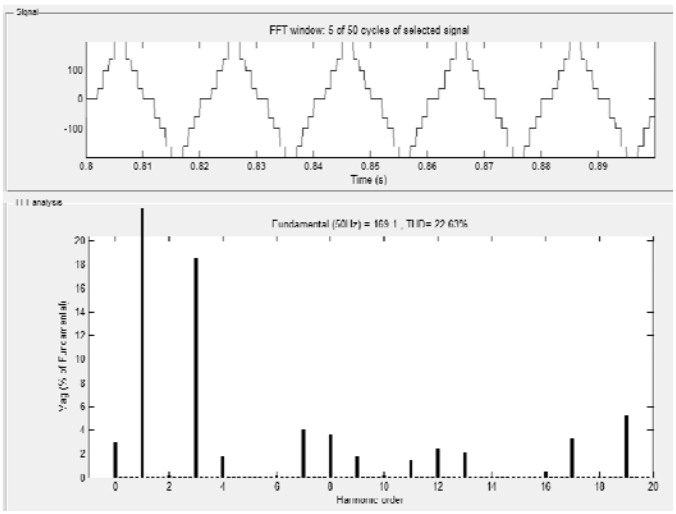

Figure 12. Output Voltage THD Spectrum of Proposed Technology

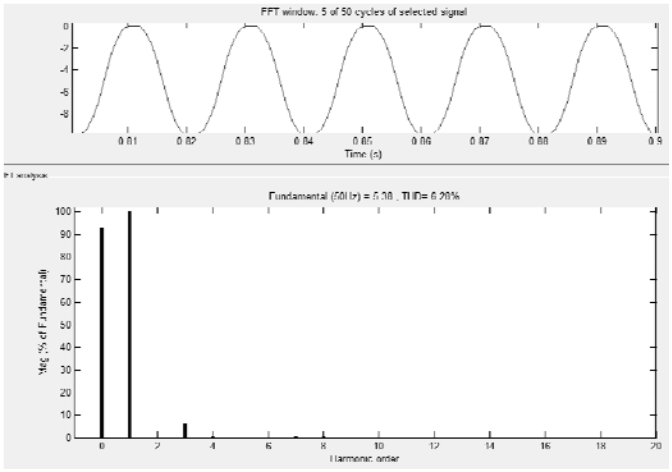

Figure 13. Output Current THD Spectrum of Proposed Topology

6. CONCLUSION

In this paper, a novel 9-level multilevel inverter has been proposed. For the proposed structure, each switch consists of an IGBT and one anti-parallel diode also one capacitor and one resistor are connected across the switch. The proposed inverter gives a qualitative output voltage and current waveform with reduced amount of ripple content. Also this inverter is help full in reactive power compensation. The simulation results have been presented for the proposed inverter using the SPWM technique. From the results of the proposed system THD value is reduced when compare to conventional system. The proposed inverter used in FACTS, UPS, ASDs, and Var compensators.

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