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Harmonic Analysis of 3-Level and 5-Level Diode Clamped Multilevel Inverter based on Sinusoidal PWM Control

Mohammed Annas[1] and J.E. Muralidhar[2]
[1]M.E. Final Semester (Power Electronic Systems), Muffakham Jah College of Engineering and Technology, Hyderabad, Telangana.
[2]Associate Professor, Electrical Engineering Department, Muffakham Jah College of Engineering and Technology, Hyderabad, Telangana.
Email:- [1]anas.muhd3545@gmail.com. [2]muralidhareed@mjcollege.ac.in

ABSTRACT
The multilevel began with three level converters. The elementary concept of a multilevel converter is to achieve higher power by using a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. The output voltage is smoother and has multiple possible values based on number of levels which results in smaller harmonics. In this paper, 3-Phase diode clamped multilevel inverter topology is analyzed by employing SPWM technique which controls the switching operation. This paper also shows the comparison of %THD between three level and five level diode clamped multilevel inverter. Circuit configuration and theoretical operation are also discussed. The performance of the topology is investigated through MATLAB-R2008b based simulation results.
Key Words: Diode Clamped Multilevel Inverter, Sinusoidal PWM Technique, Total Harmonic Distortion.

1. INTRODUCTION

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, enhanced quality of product, better maintenance, and so on.

A multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, blowers, fans, compressors, and so on[1]. As a cost able solution, multilevel converter not only obtain high power ratings, but also allow the use of low power application in renewable energy sources such as fuel cells, photovoltaic, and wind which can be easily interfaced to a multilevel converter system for a high power application.

The most frequent primary application of multilevel converters has been in traction, both in locomotives and track-side static converters. More new applications

have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission, and most newly for medium voltage induction motor variable speed drives. Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems. The inverters in such application areas as stated above should be able to handle high voltage and large power. Therefore, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off Thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems, namely, non-equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices. As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. Diode clamped inverter is the most commonly used multilevel topology[2] , in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Nabae, Takahashi, and Akagi were proposed neutral point converter in 1981 it was essentially a three-level diode-clamped inverter.

2. DIODE CLAMPED MULTI LEVEL INVERTER TOPOLOGY

In this topology there are two pairs of switches and two diodes are consists in a three-level diode clamped inverter. All switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage[3]. The DC bus voltage is dividing into three voltage levels with the help of two series connections of DC capacitors, C1 and C2. With the help of the clamping diodes D_{c1} and D_{c2} the voltage stress across each switching device is partial to V_{dc}. It is supposed that the total dc link voltage is V_{dc} and mid-point is synchronized at half of the dc link voltage, the voltage across each capacitor is $V_{dc}/2$ ($V_{c1}=V_{c2}=V_{dc}/2$). In a three level diode clamped inverter, there are three different feasible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. At any time a set of two switches is on for a three-level inverter, and in a five-level inverter, a set of four switches is on at any given time and so on. Switching states of the three levels inverter are summarized in table-1.

Table 1 Switching states in one leg of the three-level diode clamped inverter

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON S_1=OFF,S_2=OFF	S=+ve	V_{ao}=Vdc/2
S_1=OFF,S_2=ON S_1=ON,S_2=OFF	S=0	V_{ao}=0
S_1=OFF,S_2=OFF S_1=ON,S_2=ON	S=-ve	V_{ao}=-Vdc/2

Figure1 shows a three-level diode-clamped converter in which the dc bus consists of two capacitors C_1 and C_2. For dc-bus voltage E, the voltage across each capacitor is E/2 and each device voltage stress will be limited to one capacitor voltage level E/2 through clamping diodes. To explicate how the staircase voltage is synthesized, the neutral point **n** is considered as the output phase voltage reference point.

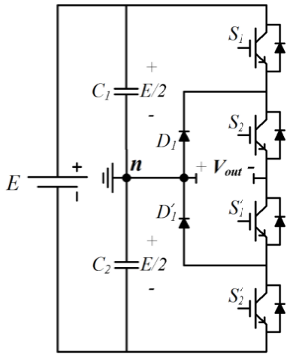

Figure 1 3-Phase Three level diode clamp multi-level inverter (one leg)

Table 2 Switching states in one leg of the five-level diode clamped inverter.

Voltage Vao	Switch state							
	S1	S2	S3	S4	S1'	S2'	S3'	S4'
Vao=Vdc	1	1	1	1	0	0	0	0
Vao=Vdc/2	0	1	1	1	1	0	0	0
Vao=0	0	0	1	1	1	1	0	0
Vao=-Vdc/2	0	0	0	1	1	1	1	0
Vao=-Vdc	0	0	0	0	1	1	1	1

Figure 2 shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For dc-bus voltage V, the voltage across all

capacitor is V/4 and each device voltage stress will be limited to one capacitor voltage level V/4 through clamping diodes[4].

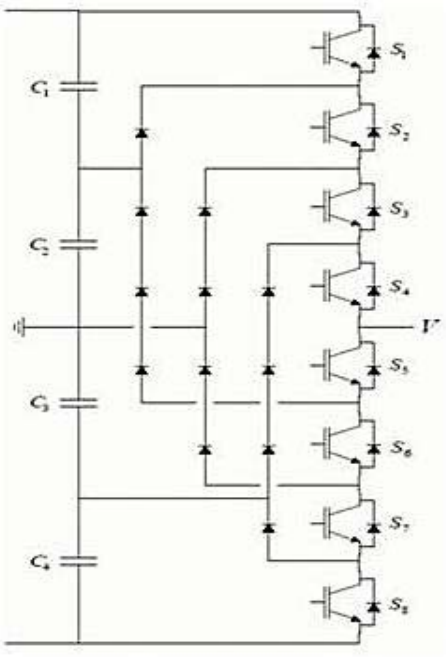

Figure 2 Five level diode clamp multi-level inverter (one leg)

3. CONTROL TECHNIQUE OF DIODE CLAMPED MULTILEVEL INVERTER

The sinusoidal PWM technique is very popular for industrial converters. In this technique, an isosceles triangle carrier wave of frequency fc is compared with the fundamental frequency f sinusoidal modulating wave and the points of intersection determines the switching points of power devices.

Two important parameters of the design process are amplitude modulation index $m_a = V_r/V_c$, where V_r is the peak amplitude of reference control signals, V_c is the peak amplitude of the carrier wave, and the frequency modulation index $m_f = f_c/f_r$, where f_c is the frequency of the carrier wave and f_r is the reference sinusoidal signal frequency.

m_a and f_r determines the magnitude and frequency of output voltage, f_c determines switching frequency of power semiconductor devices.

Multilevel converters are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: Level Shifted (LS-PWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) or they can be Phase Shifted (PS-PWM). In present topology PD is used.

3.1 SPWM Generation for 3-Level Inverter

Three level pulse width modulated waveforms can be generated by sine-carrier PWM. Sine carrier PWM is generated by comparing the three reference control signals (one for each phase) with two triangular carrier waves[5].

$$V_{io} = \begin{cases} V_{dc}/2 & , \ V_{ref,i} > V_{tri,1} \\ 0 & , \ V_{tri,1} > V_{ref,i} > V_{tri,2} \\ V_{dc}/2 & , \ V_{tri,2} > V_{ref,i} \end{cases}$$

Where i =a, b or c phase

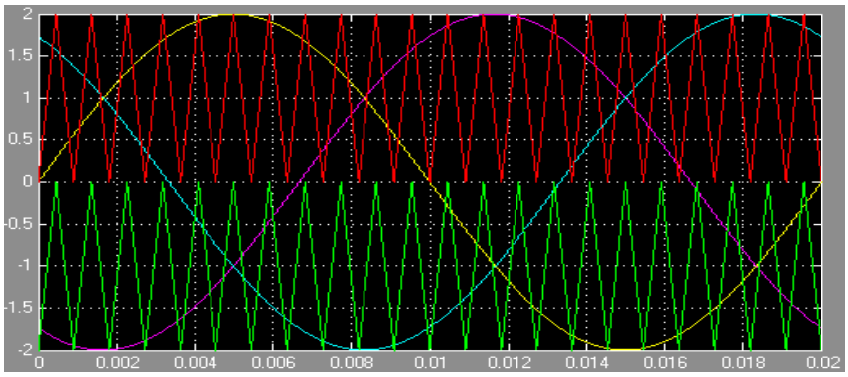

Figure 3 Control Pulse Generation in Three Level SPWM

3.2 SPWM Generation for 5-Level Inverter

Five level pulse width modulated waveforms can be generated by sine-carrier PWM by comparing the three reference control signals (one for each phase) with four triangular carrier waves[6].

$$Vio = \begin{cases} V_{dc}/2 & , \ V_{ref,i} > V_{tri,1} \\ V_{dc}/4 & , \ V_{ref,i} > V_{tri,2} \\ 0 & , \ V_{tri2} > V_{ref,i} > V_{tri,3} \\ -V_{dc}/4 & , \ V_{tri,3} > V_{ref,i} \\ -V_{dc}/2 & , \ V_{tri,4} > V_{ref,i} \end{cases}$$

Where i =a, b or c phase

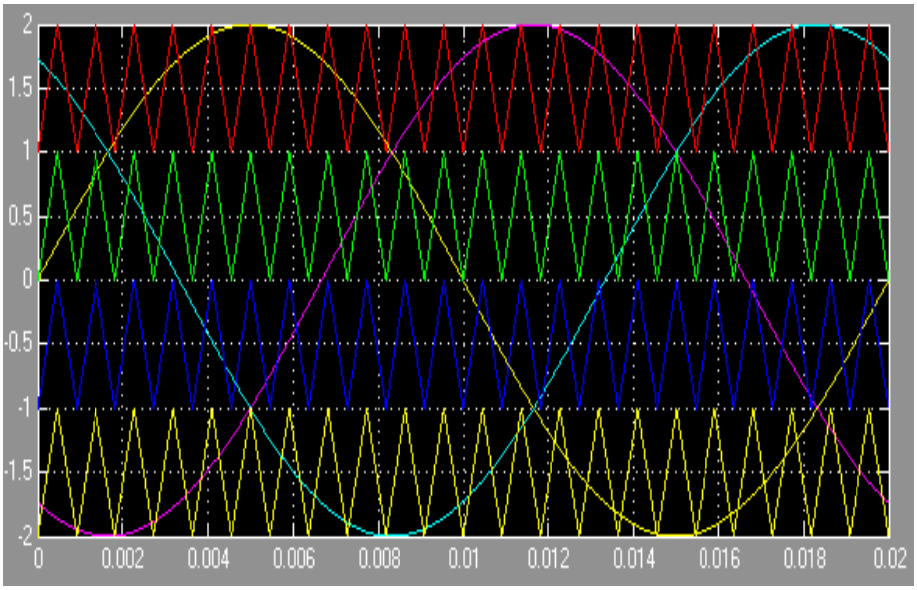

Figure 4 Control Pulse Generation in Three Level SPWM

In both 3-Level and 5-Level Diode Clamped Inverters, The three reference control signals are phase shifted by 120° from each other with same amplitude and Phase Disposition Pulse width modulation (PDPWM) is employed where in all carrier waves are in phase with each other.

4. CIRCUIT CONFIGURATION

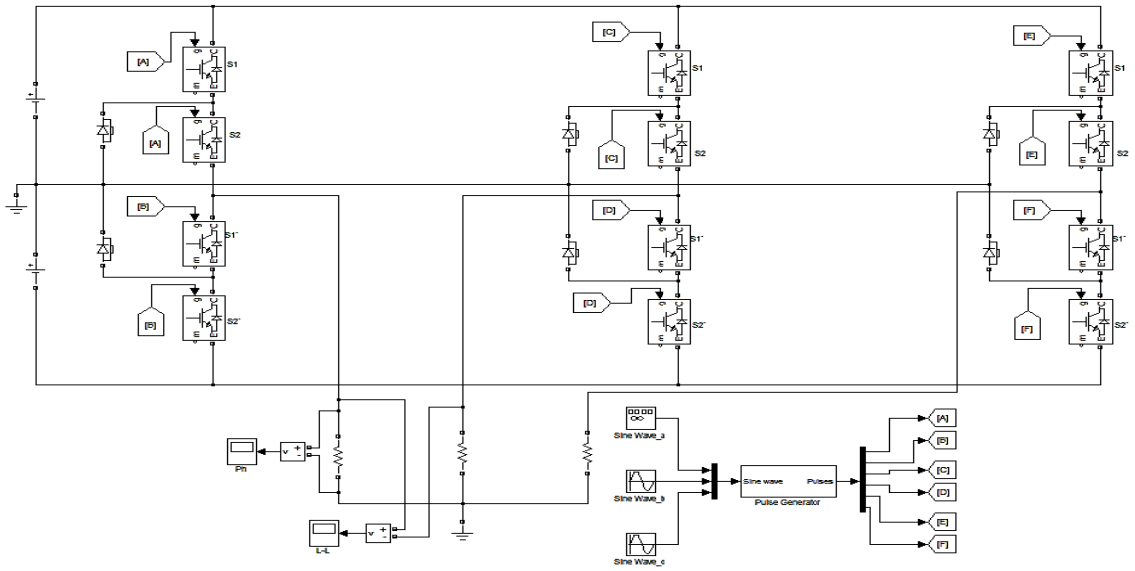

Figure 5 Simulink Model of Three Level Diode Clamped SPWM Inverter

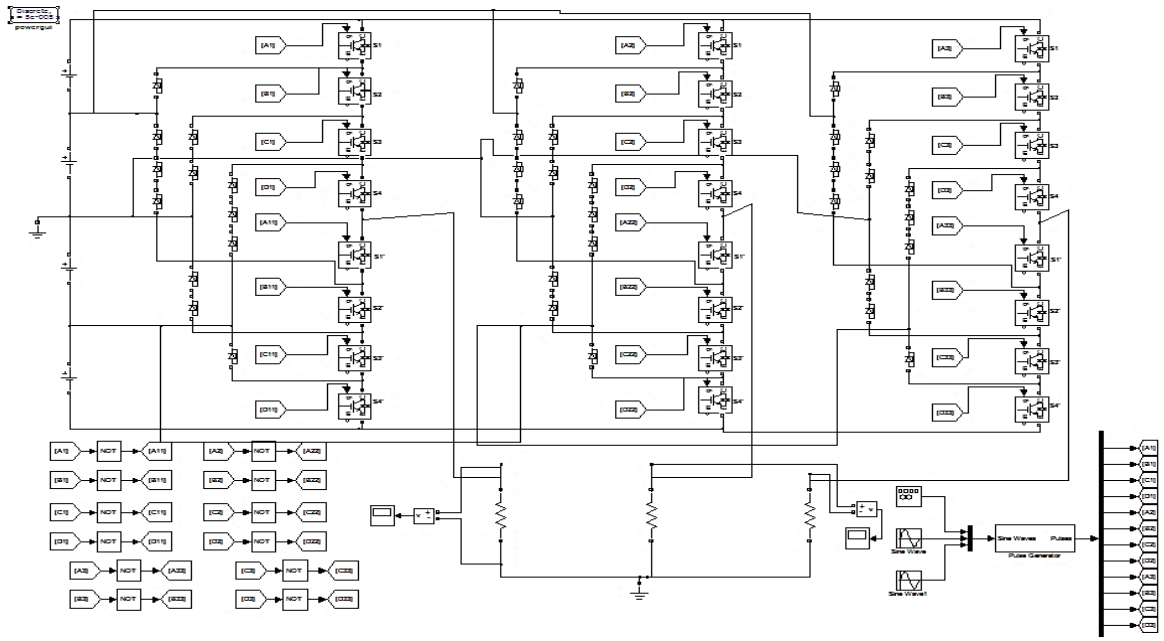

Figure 6 Simulink Model of Three Level Diode Clamped SPWM Inverter

Specifications (for both 3-Level and 5-Level Inverter):

Supply Voltage = 200V

Fundamental Frequency (f_r) = 50 Hz

Switching Frequency (f_s) = 1.1 KHz

Amplitude Modulation Index (m_a) = Variable

Frequency Modulation Index (m_f) = 22

5. SIMULATION RESULT

Simulation of Three phase diode clamped inverter using sinusoidal pulse width modulation was carried out with the help of "MATLAB R2008b". Simulation was carried out to observe the improvement in the line voltage THD and Harmonic spectrum as the inverter level increases from 3-Level to 5-Level.

Following qualities have been observed:

1. Line voltage waveform for R Load for three level inverter.
2. Line voltage waveform for R load for five level inverter.
3. Substantial decrease in the line voltage THD as the magnitude of Modulation index (ma) is increased.

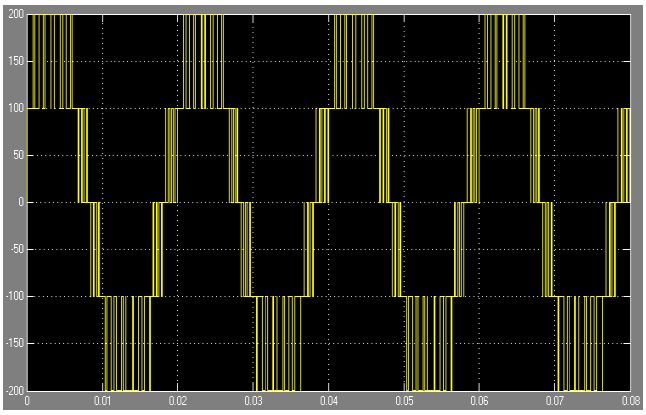

Figure 7(a) Simulated Line voltage of 3-Level diode clamped inverter

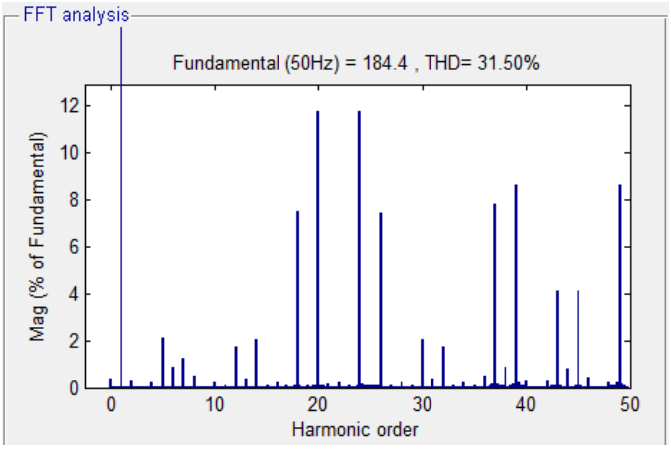

Figure 7(b) Harmonic Spectrum of 3-Level diode clamped inverter for R= 25Ω/phase and m_a=1.

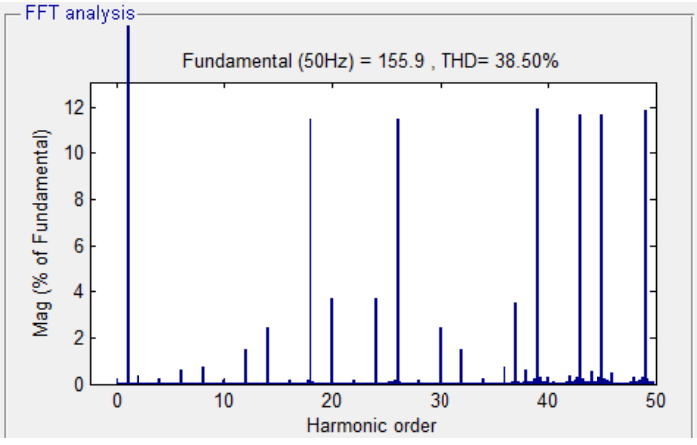

Figure 7(c) Harmonic Spectrum of 3-Level diode clamped inverter for R= 25Ω/phase and m_a=0

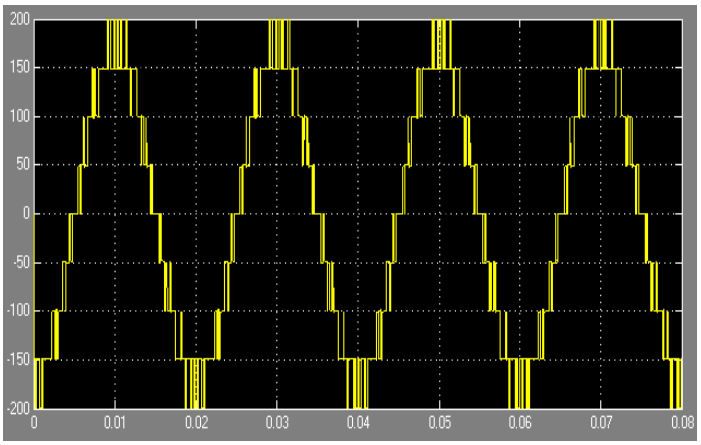

Figure 8(a) Simulated Line voltage of 5-Level diode clamped inverter

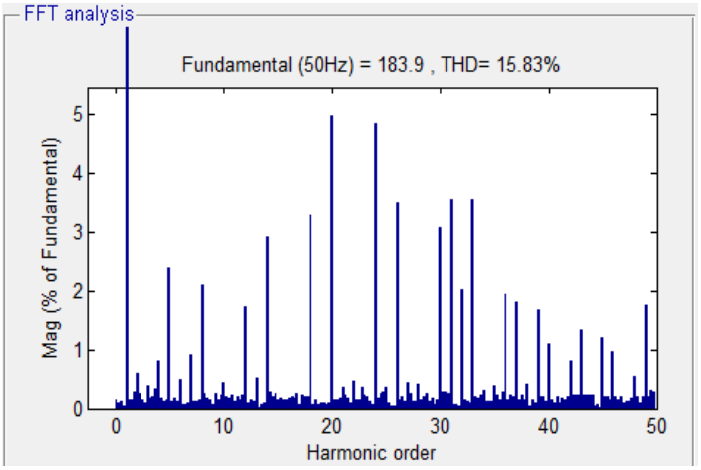

Figure 8(b) Harmonic Spectrum of 5-Level diode clamped inverter for R= 25Ω/phase and m_a=1.1

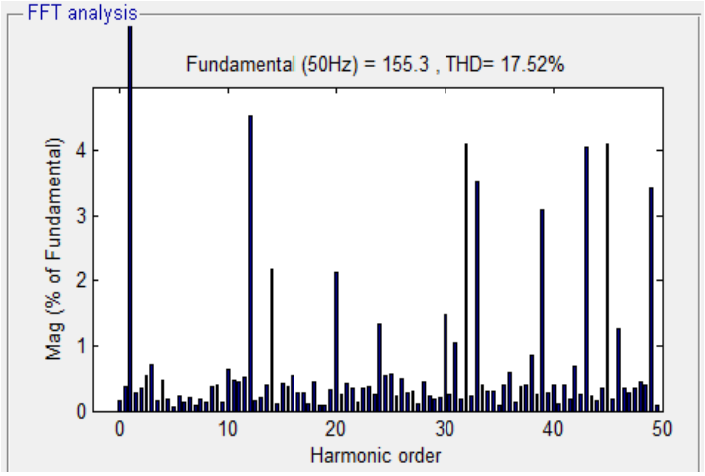

Figure 8(c) Harmonic Spectrum of 5-Level diode clamped inverter for R= 25Ω/phase and m_a=0.9

Table 3 Comparison of the calculated Line voltage THD for fixed R Load

Modulation Index (ma)	% THD 3-Level	% THD 5-Level
1.1	31.94	15.93
1	35.25	17.23
0.9	39.20	17.45
0.8	42.03	21.73
0.7	44.30	24.18
0.6	49.17	26.43
0.5	68.54	35.29

6. CONCLUSION

The simulation of 3-Level and 5-Level Diode clamped multilevel inverter was carried using sinusoidal pulse width modulation (PWM). This paper briefly explains the theory of phase disposition sinusoidal pulse width modulation (PDSPWM) for three and five level inverter. It has shown that reduction in line voltage THD takes place as we move from three level inverter to five level inverter and performance of both inverters were investigated using R Load. Also a comparison of %THD for both the inverters has been tabulated for different values of amplitude modulation index (m_a).

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