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Design and Implementation of an Efficient Fft Processor using Modified Booth Multiplier

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Abstract : The FFT plays an important role in OFDM regarding its performance. An efficient multiplier is needed to perform butterfly operation in FFT. This multiplier is related to area, power and time. The performance of OFDM depends upon the multiplier. The proposed multiplier is developed by using Verilog HDL and implemented by using Model Sim 6.3*c* for stimulation and Xilinx 12.4 for synthesis. The proposed multiplier reduce the number of slices, LTU(look up tables) and hence area and delay got reduced.

Keywords: *CSLA, Modified Booth, Slices , LUT(look up tables) , Delays, PPG.*

1. INTRODUCTION

[2] In OFDM is an efficient wireless standard that falls under the category of multi carrier modulation technique where sub carriers are orthogonal to each other. The orthogonality condition helps to eliminate cross talk between the sub channels. It simplifies the design of transmitter and receiver unlike conventional FDM.

[1] The block diagram of OFDM is shown in the fig.1.The cyclic encoding is done initially on the input data then the serial input data is converted to parallel data by using serial to parallel convertor and then send to signal mapper which is executed by performing modulation techniques[11],[3] such as 32-QAM,64-QAM and 128-QAM. The interleaver block reduces the error bit to the encoder and also increase resistance to fading. To spread the errors out in the bit stream that is presented to the error correction decoder. [5] Now, the interleaved symbol is modulated into subcarrier by Inverse Fast Fourier Transform(IFFT) followed by cyclic pefix.The cyclic prefix serves two purposes –as a guard interval, it eliminates the intersymbol interference from the previous symbol and also input the synchronization.[6] The original output is extracted for the receiver by demodulation process which is the reverse of all the above process.

[4],[8]The advantages of using OFDM instead of single carrier is that it has the ability to cope with severe channel condition [10]such as attenuation of high frequency in long copper wire, interference narrow band, fading due to multi path without equalization filters.

[9] OFDM is used in certain application like digital audio broadcasting [4], digital video broadcasting, IEEE 802.11 and so on.

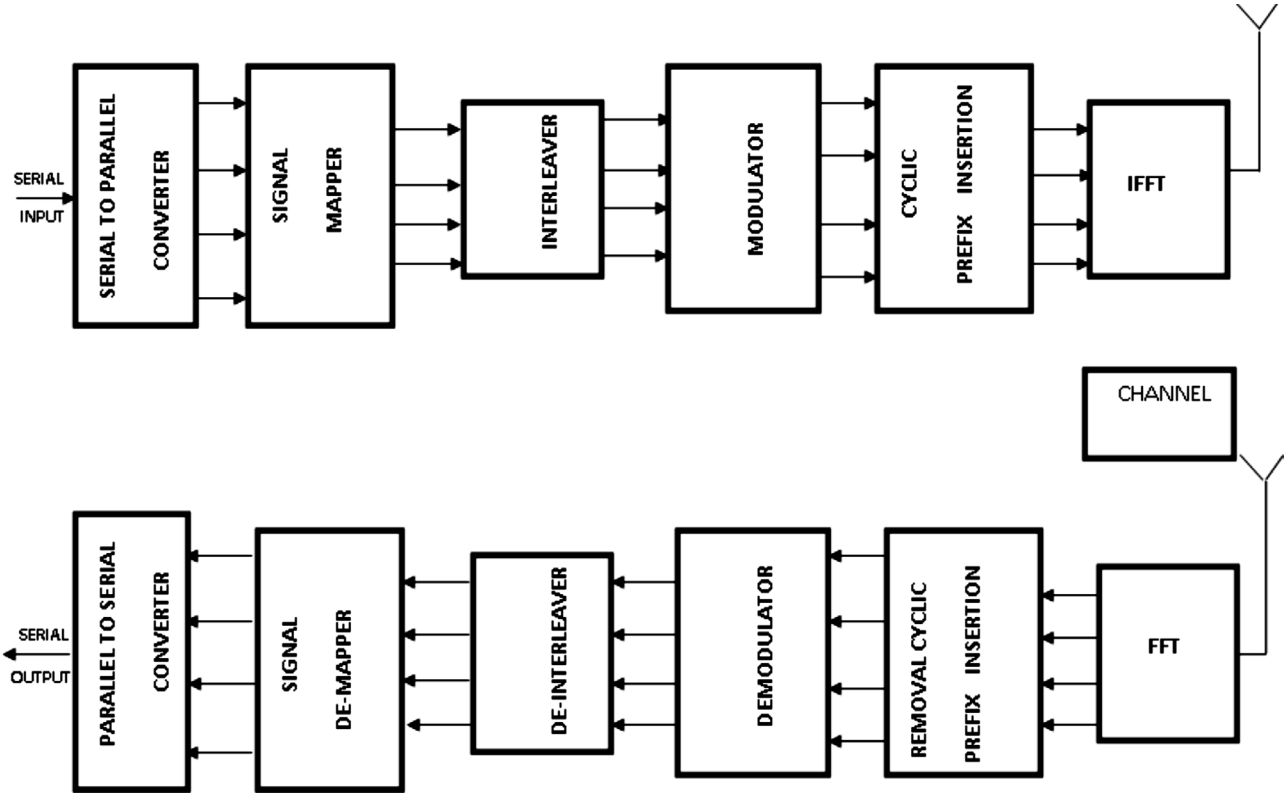

Figure 1: OFDM modem

2. PROBLEM IDENTIFICATION

The power and speed of the Orthogonal Frequency Division Multiplier (OFDM) modem are dominated by IFFT/FFT [2] [3]. In specific, the performance of the Fast Fourier Transform (FFT) is degraded if the multiplier used in the FFT consumes more power , area and delay. Many works have been contributed such as pipelined FFT [12], parallel FFT [13], parallel-pipelined FFT [14] and serial FFT [7]. The entire works on FFT suggest an architectural level development that will improve the performance FFT. [15] But a trivial solution is given to improve the performance of the FFT based on computational components (*i.e*. multipliers, adders and Partial Product Generator (PPG) architecture. This paper contributes to the improvement of FFT by developing an efficient multiplier to compute the butterfly operation, thereby improving the overall performance of OFDM.

3. PROPOSED MULTIPLIER

The proposed multiplier drive out the complexity of multipliers and adders present in the FFT which plays a critical component in OFDM that consumes more area and power. The layout the proposed efficient multiplier is shown in figure 2.

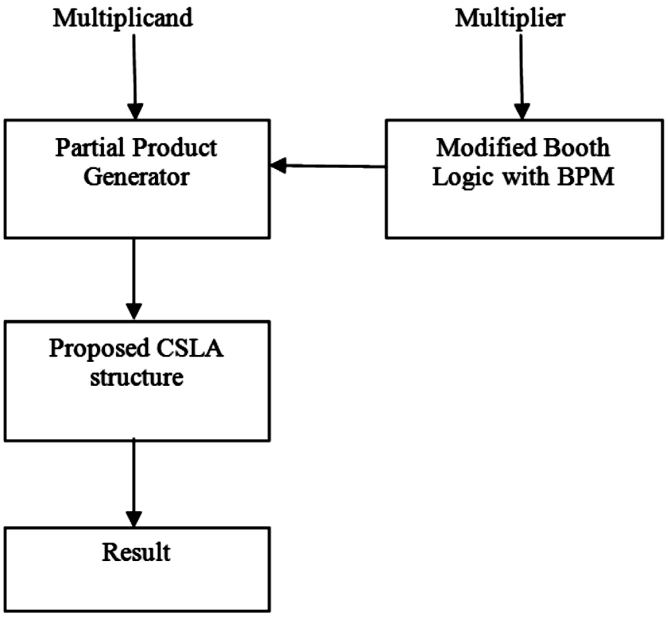

Figure 2: Proposed Multiplier

This multiplier comprises of carry select adder (CSLA), partial product generator (PPG) and enhanced logic of modified Booth logic with bit parallel multiplication (BPM) concept.

Let us consider M is the number of multiplier bit and N is the multiplicand bit then (MXN) produces M partial product and (M + N) product.

The proposed 16 bit multiplier produces 16 partial products which can be reduced to 8 by using booth encoder logic there by reducing area and power. The enhanced logic of carry select adder will overcome the problem of propagation delay and place and route.

Thus by utilizing various logics such as CSLA, Booth, BPM we have developed an efficient multiplier interms of area, power and delay.

3.1. Booth logic with BPM

The logic behind the modified booth is to reduce the partial product. Consider the basic table for the booth implementation as shown in Table 1.

Table 1
Table for booth logic

X	*X–1*	*Action*
0	0	No action, >>1
0	1	(U + Y) & >>1
1	0	(U – Y) & >>1
1	1	>>1

Consider that X is the input to the multiplier. U is the initial value . Y is the value which is taken from the BPM module that is the twiddle factor value. Each twiddle factor is designed individual by the basic of BPM (bit parallel multiplication) concept. The output of BPM undergoes further multiplication on booth logic which reduces the complexity of booth multiplication .

The reduction in area is achieved by reducing the partial product using booth logic and in addition the carry select adder is used to reduce the propagation delay.

Let us consider $X = 0100$,

$Y = 1010$

Table 2

U	*V*	*X*	*X–1*
0000	0000	0100	0
0000	0000	0010	0
0000	0000	0001	0
0110	0000	0001	0
0011	0000	0000	1
1101	0000	0000	1
1110	1000	0000	0

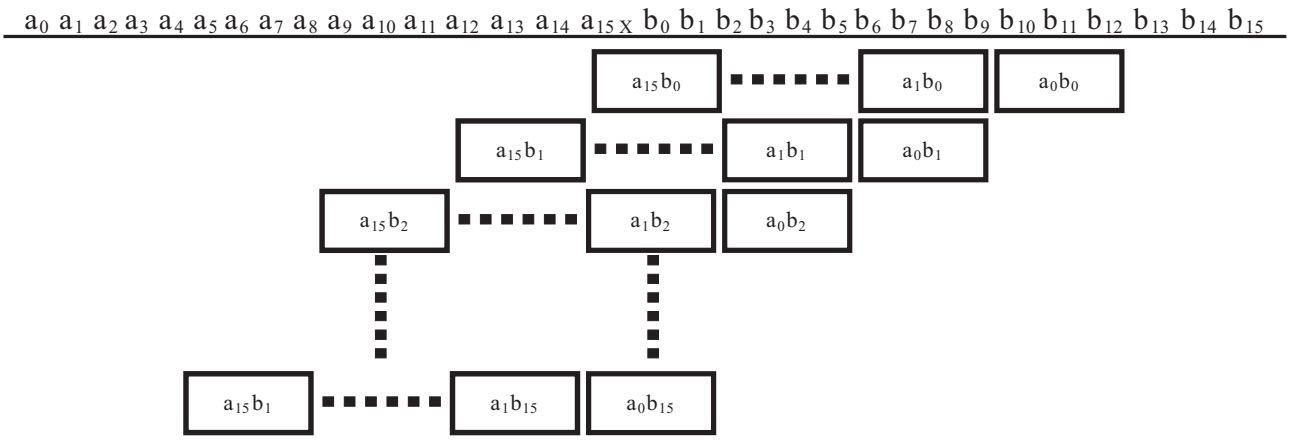

Figure 3: PPG for 16-bit Multiplier

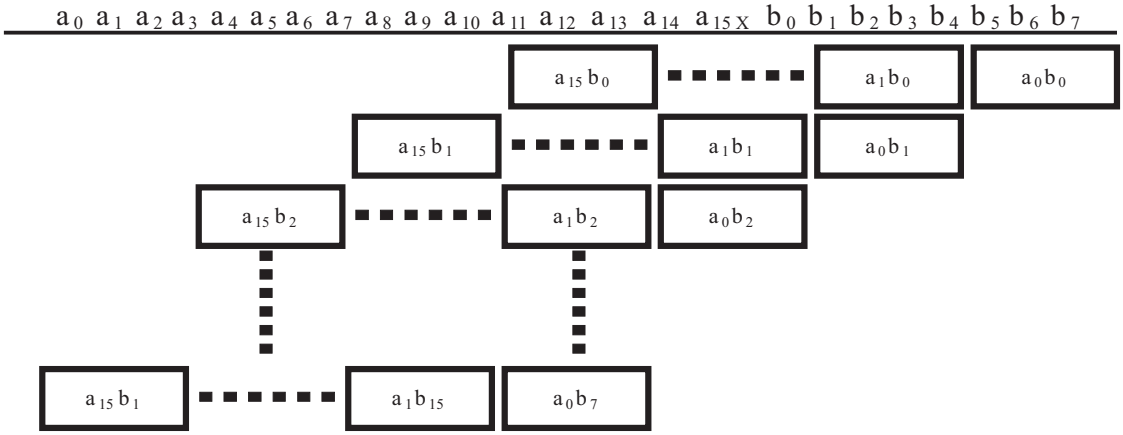

Figure 4: PPG reduced by booth multiplier

3.2. Partial Product Generator

Here, the booth logic is utilized to generate the reduced partial product . The figure 3 shows the partial product generator for the proposed 16- bit multiplier. A total of 16 partial products is present in the diagram as an output of multiplication without booth logic .Further a total of 8 partial products are produce by using combined logic of booth and BPM. Thus the 16 partial products are reduced to 8 as show in the figure 4.

3.3. Carry Select Adder

The final stage of the partial product is added by using carry select adder which can compute the addition of two binary numbers at high speed. The novel logic behind the CSLA adder is that reduce the propagation delay.

The addition process carried by using adders such as ripple carry adder , CLA, CSA produces 'n' propagation delay for 'n' bits. By using CSLA , ($\sqrt{}$ n-1) propagation delay occurs for 'n' bits.

4. IMPLEMENTATION OF PROPOSED MULTIPLIER IN FFT

The Fast Fourier Transform (FFT) architecture comprises of input and output buffer , FFT unit , butterfly unit, control unit and twiddle factor.

The proposed efficient multiplier is a multiplier which is implemented in butterfly unit as shown in figure 5.

The butterfly unit computes the twiddle factor multiplication, where the twiddle factor is stored and retrieved from the buffer whenever it is required. The FFT unit is made up of butterfly unit where the proposed efficient multiplier is implemented the combination of booth logic with BPM module, CSLA adder will increase the speed of FFT operation.Here the input and output buffer is used to store the input bits and computed output bits respectively.

The control unit which plays a vital role in FFT operation that controls the whole FFT processor. Clk_in, enable, FFT, start, ready, D_valid are the various signals used in the control unit. The input buffer is loaded when the start signal is high in the same manner the computed output is stored in the output buffer while the D_valid is high.

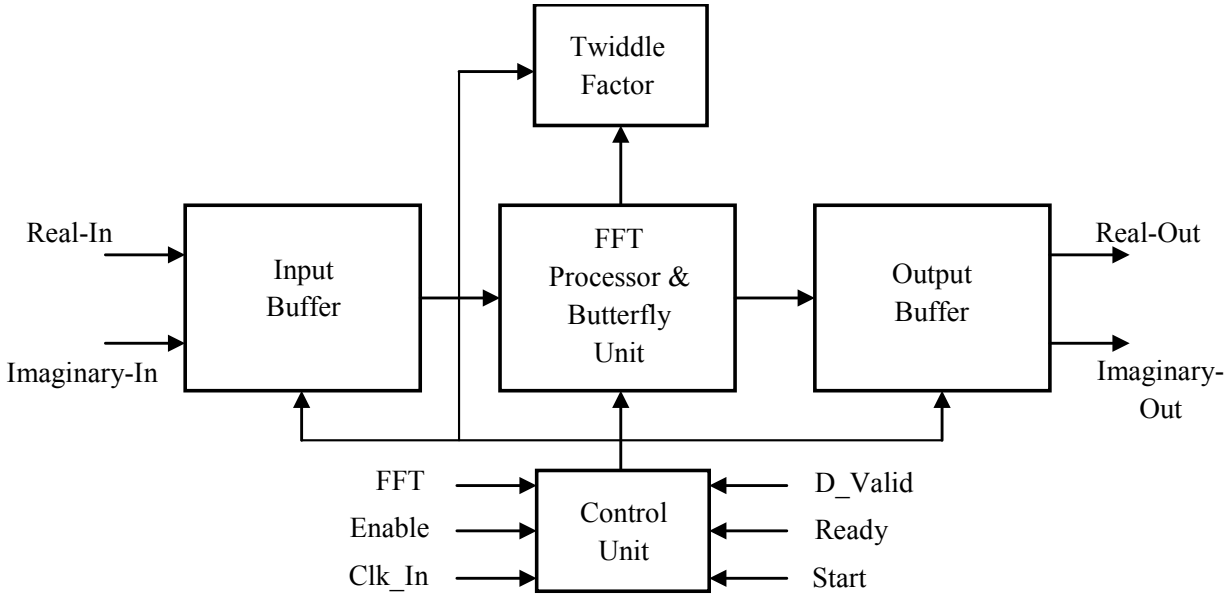

Figure 5: FFT processor

5. PERFORMANCE EVALUATION

The proposed multiplier and the fast fourier transform(FFT) core is developed using verilog HDL, implemented in software for simulation Model Sim 6.3C and for synthesis Xilinx 12.4

In this performance evaluation we analyzed the slices, LUTs(Look Up tables) and delay for various twiddle factor values and the whole FFT processor.

Table 3
Performance Evaluation

Twiddle factor/ FFT	*Slice*		*LUTs*		*Delays*	
	Existing	*Proposed*	*Existing*	*Proposed*	*Existing*	*Proposed*
0.707	22	21	43	41	19.162*ns*	19.140*ns*
0.707 inv	24	19	45	37	19.682*ns*	18.377*ns*
0.9239	27	15	51	29	20.792*ns*	17.969*ns*
FFT	917	899	1662	1528	23.295*ns*	23.280*ns*

Slices refers to the statement condition, if slice reduces the number of wires used in the coding also get reduced. LUTs is the gate count.

By comparing the existing system without modified multiplier and the proposed multiplier, the slices and LUTs get reduced compare to the design in [11]. So that the overall propagation delay and the power consumption are also reduced.

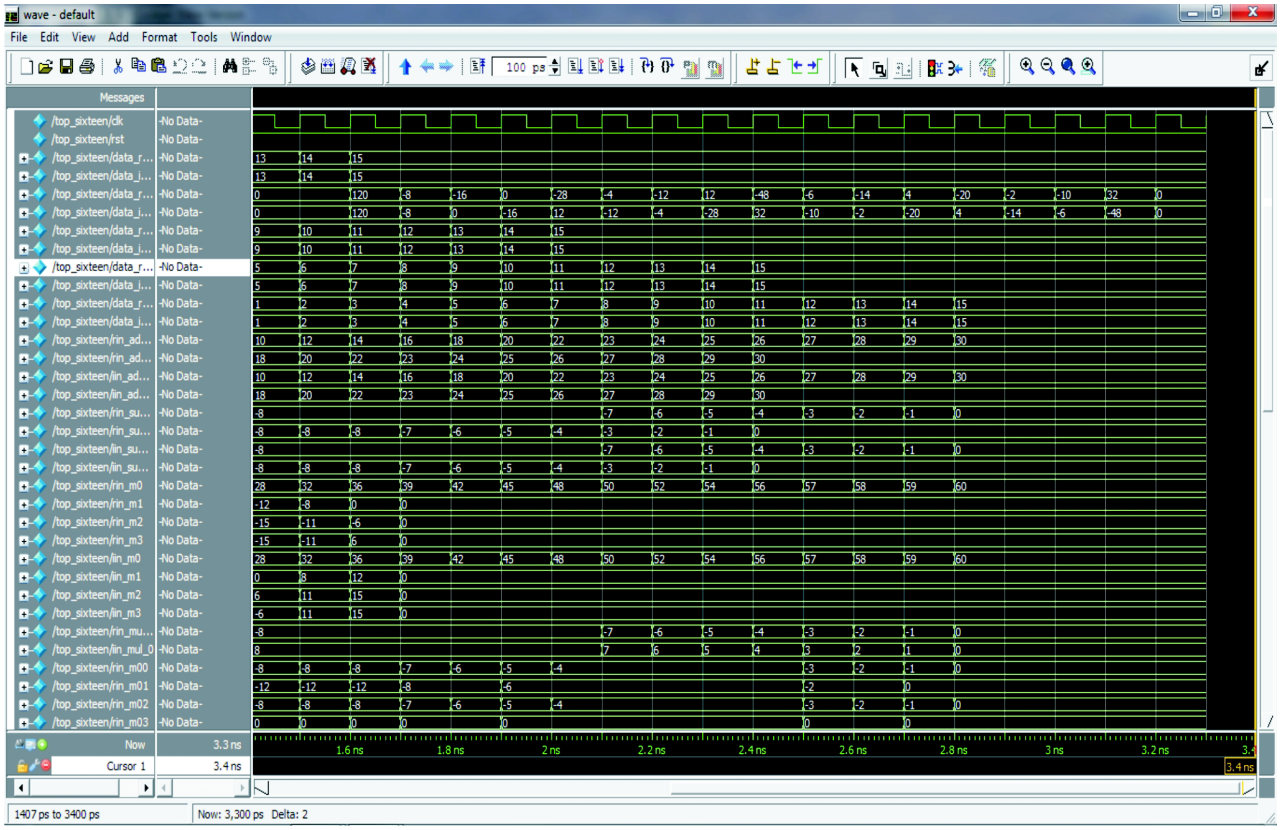

Figure 6: The simulation output of FFT processor

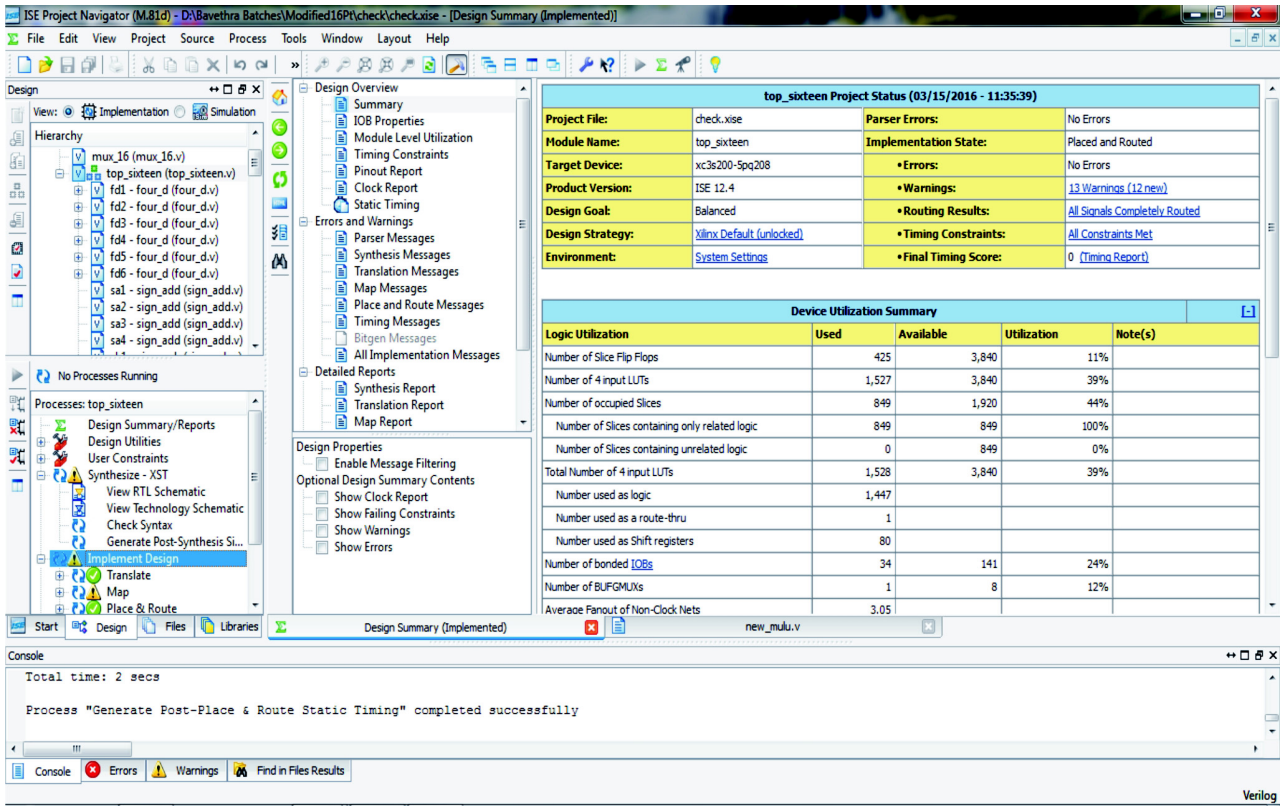

Figure 7: The output of FFT processor which shows reduction of area

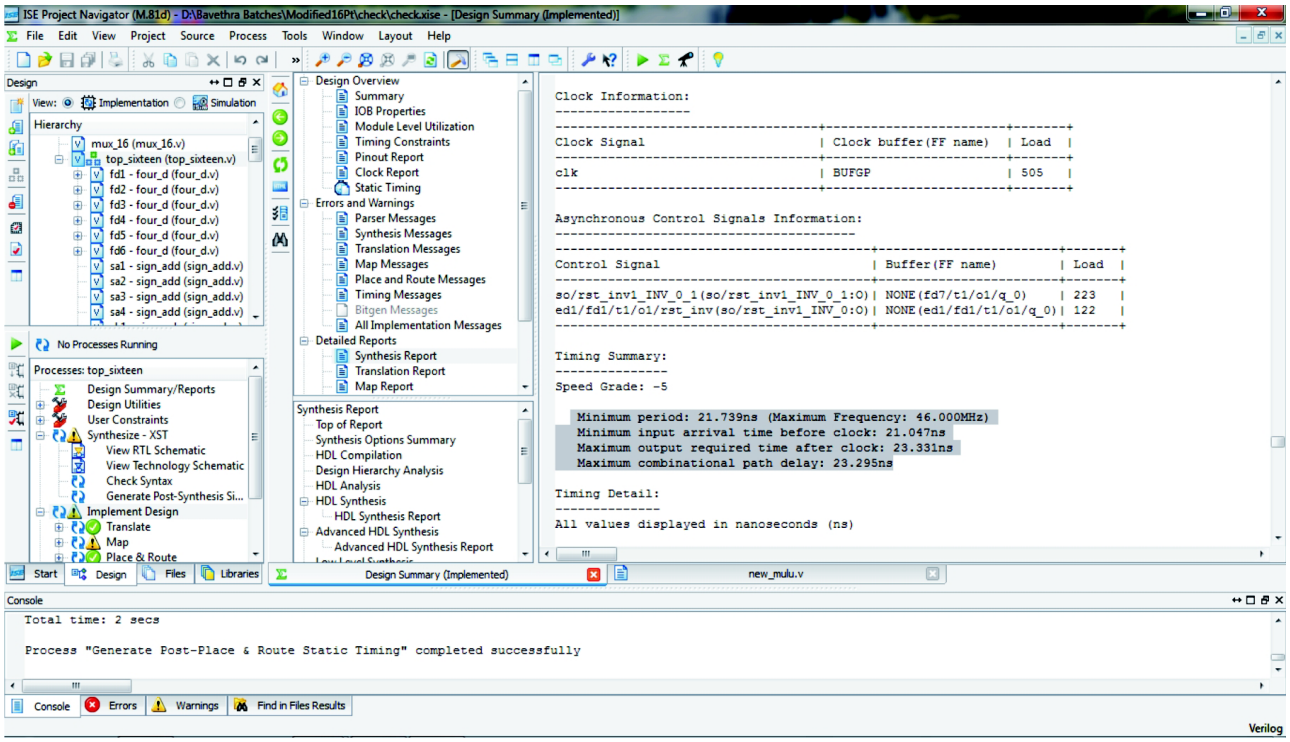

Figure 8: The output of FFT processor which shows the reduction in delay

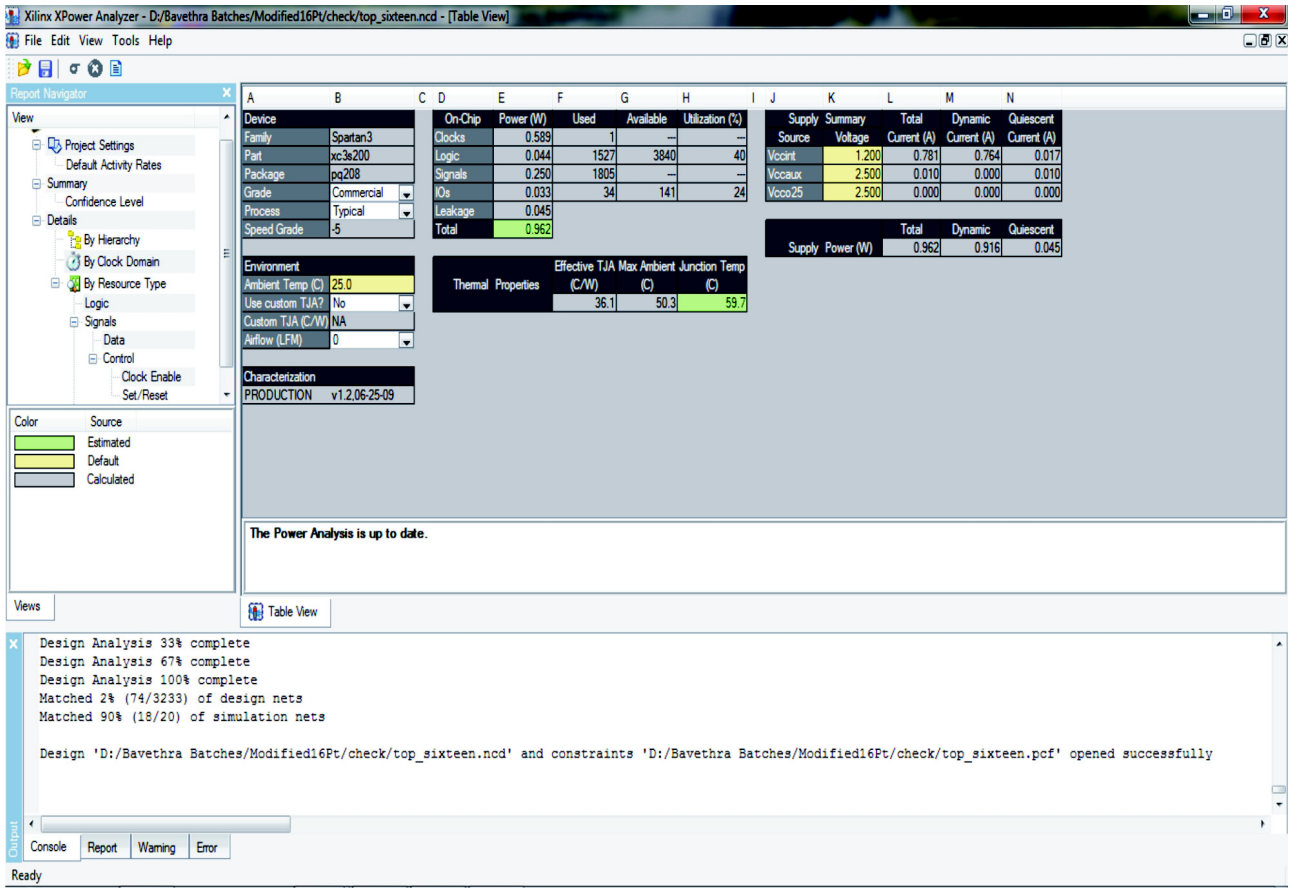

Figure 9: The output of FFT processor which shows the reduction in power

6. CONCLUSION

The Fast Fourier Transform with efficient multiplier design is proposed in this paper. The proposed multiplier improves the performance of FFT interms of area, power and speed.The proposed multiplier reduces the delay and area which in turn improves the overall performance of OFDM as OFDM depends upon the FFT processor. Hence the proposed FFT processor outperforms the conventional FFT architecture. The proposed FFT processor is developed by using Model Sim-6.3C and Xilinx-12.4 interms of verilog HDL. In future the multiplier proposed in this paper can be implemented in various architecture.

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