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Novel Designs for Efficient PFD and Charge Pump Designs for Phase Locked Loop

Supraja Batchu[1], Ravi Nirlakalla[2] and Jayachandra Prasad Talari[1]
[1]Department of Electronics and Communication Engineering,
[2]Department of Physics,
RGM College of Engineering & Technology (Autonomous), Nandyal-518501 AP, India.
(batchusupraja, ravi2728, jp.talari@gmail.com)

ABSTRACT

Phase Locked Loop (PLL) usual replicated problems are different requirements like small acquisition time, maximum locking range and minimum phase error variance. To meet these requirements with low power applications various phase frequency detector (PFD) designs are proposed. The current mismatch is one of the essential problems in PLLs which generates spurs. A charge pump (CP) is designed to reduce mismatch in the currents. A small delay is created in the critical path of the CP to reduce the current mismatch. The results are carried out using HSPICE.

1. INTRODUCTION

CMOS technology continues device scaling for high integration. However, as the feature size shrinks and chip designers attempt to reduce supply voltage to meet power targets in large multi-processors, parameter variations are becoming a severe problem. Parameter variations can be broadly classified into device variations incurred due to imperfections in the manufacturing process and environmental variations and on-die temperature and supply voltage Modern CMOS nanometer technologies are very proficient, in terms of power consumption and speed, for the design of ICs; the power consumption could be negatively affected by current leakage only in large circuits. However, the performances of analog circuits are considerably degraded due to the small transistor gain, signal range, low supply voltage, and high variability of device parameters [1]. The significance of analog circuits using low supply voltage is extremely increasing in the recent past. The large component densities particularly in VLSI stress, lower power consumption. The low power consumption is a key issue in modern portable devices to increase the battery life, performance, the packaging density and circuit reliability.

Phase locked loops (PLLs) are widely used in microprocessors and digital systems for clock generation and as a frequency synthesizer in communication systems for clock extraction and generation of a low phase noise local oscillator. The PLLs was first described in the early 1930s, where its application was in the synchronization of the horizontal and vertical scans of television. Later on with the development of integrated

circuits, it found uses in many other applications. A PLL is a feedback control circuit, and is operated by trying to lock to the phase of a very accurate input through the use of its negative feedback path. A basic form of a PLL consists of four fundamental functional blocks namely:

1. Phase Frequency Detector (PFD)
2. Charge Pump (CP)
3. Voltage Controlled Oscillator (VCO)
4. Frequency Divider (FD)

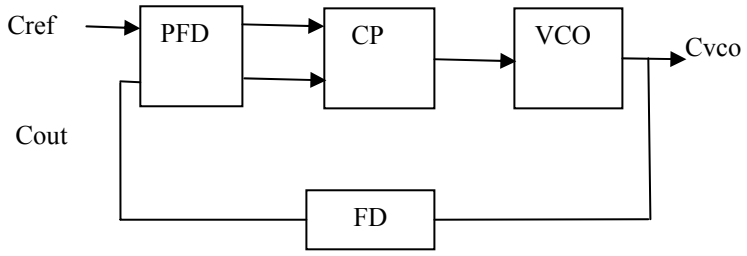


Figure 1. Block diagram of Phase Locked Loop

2. PHASE FREQUENCY DETECTOR

The phase frequency detector (PFD) acts as a comparator to compare signals Cout and Cref. This comparator is responsible for generating control signals (Up and Down), which commands the charge-pump (CP) circuit to charge or discharge current. The phase detector has two input signals Cref and Cout. Cout signal is the feedback signal, which is the output of divider and Cref is coming from an input divider or crystal oscillator. Two conditions are realized at the input of PFD block: first Cref leads Cout i.e as Cref goes high, the output Up goes high. When the leading edge of Cout comes, Up goes to zero while Down does not show any change and remains low. Exactly opposite mechanism happens in second case when Cout leads Cref . If both Cref and Cout are in same phase the outputs Up and Down are zero.

The UP and DOWN signals control the CP block in its charging and discharging process [2]. The states of the PFD as shown in fig 2 are represented by the logical output signals Up and Down and can be defined with:

- Up=0 and Down=1 then current is drawn from the loop.
- Up=0 and Down=0 then no change in current
- Up=1 and Down=0 then current is driven into loop filter

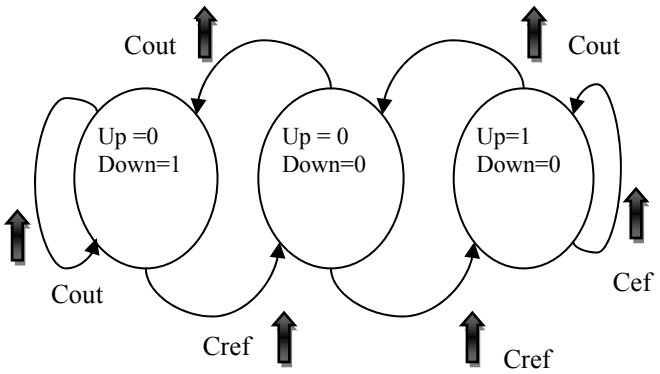


Figure 2. State Diagram of PFD

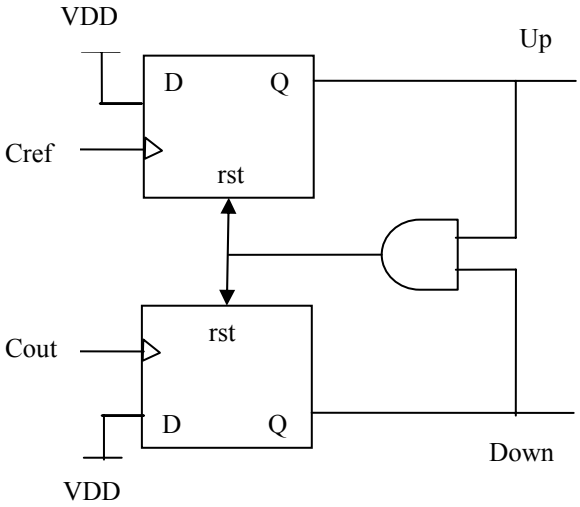


Figure 3. Conventional PFD

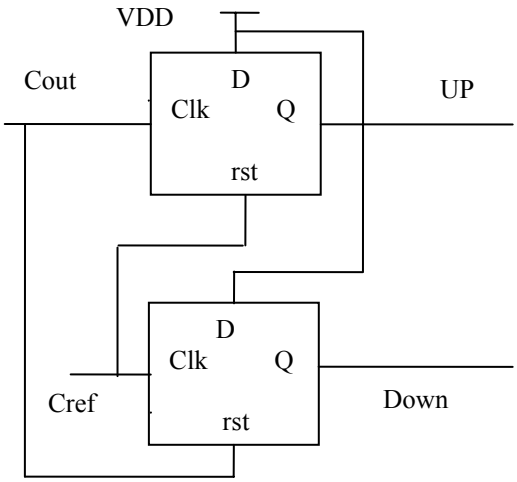


Figure 4. PFD with No Gate (DFFPFD)

Figure 3. shows a detailed design for PFD with input/output terminals. A simple design of PFD consists of two D flip flops and AND gate. The D input of the flip-flops is connected to VDD and the input signals (Cref, Cout) are applied to the clock input. When the status of the clock changes to high, this flip-flop will charge and its output goes to high. The use of AND gate is to avoid both flip-flops to be high at the same time. The inputs of the AND gate are, the Up and DOWN signal from both flip-flops, and the output of the AND gate is connected to the reset input of the flip-flops. As soon as both outputs (Up, Down) are high the AND gate will generate a high signal that will reset both flip-flops avoiding the situation of both high at the same time [3-4].

Due to the AND reset path, the time desired to charge the AND gate and reset both flip-flops will be added to the reset delay time in the internal components of the flip flops and produce a large dead zone The change is to remove the reset path and reduce the delay time that causing the dead zone problem. Figure 4 represents the PFD

with No Gate (DFFPFD). As shown in Figure.7, the D flip-flop schematic design had few changes from the D flip flop used in traditional PFD shown in Figure. 6. These changes are allowed in getting rid of the reset path and applying the CLK signal directly to the RST input for each flip-flop to reset them momentarily both flip-flops have high output at the same time. The PFDNG functions exactly like Conventional PFD but has a large propagation delay, so to reduce the delay PFDs are proposed using NOR gate and another design DFFPFDCONAND is proposed which is designed using AND gate but because of W/L aspect ratio delay & power are reduced.

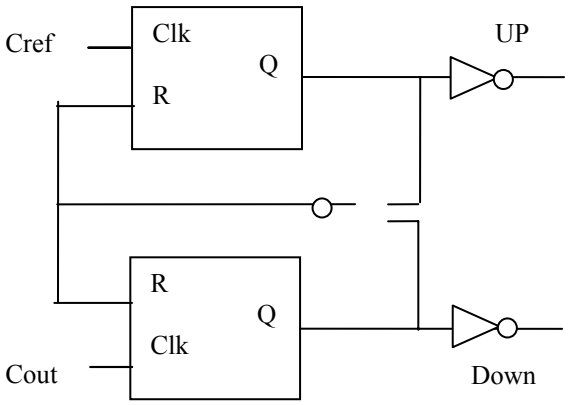


Figure 5. PFD using NOR gate

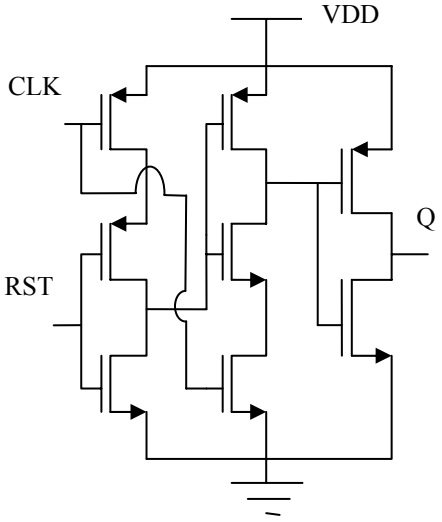


Figure.6 DFF for Traditional PFD[4]

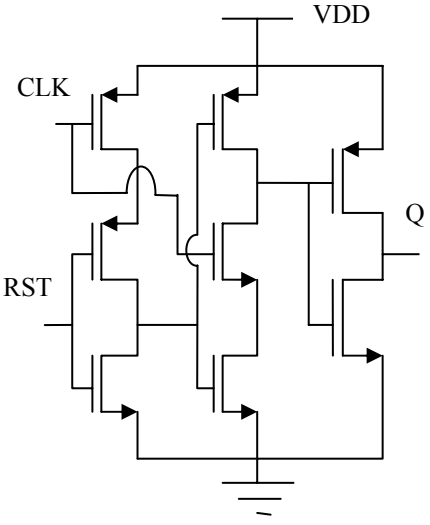


Figure.7 Modified DFF [4]

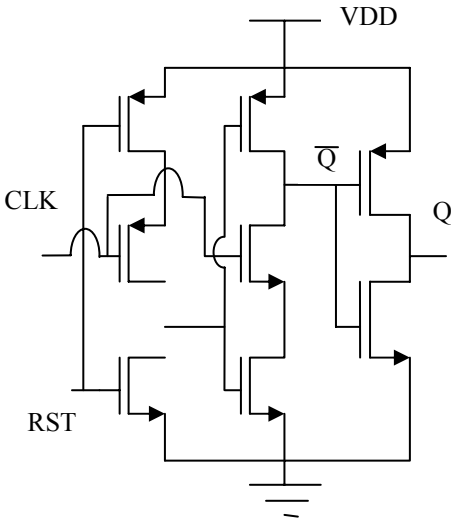


Figure. 8 DFF used in Dynamic PFD

3. CHARGE PUMP

Charge Pump controlled with three states of a PFD is an essential building block of PLLs. Charge Pump PLLs are frequently used in diverse applications, such as on chip clock synthesis, symbol timing recovery for serial data streams and generation of frequency agile high frequency carrier signals**.**

CP injects a constant current to the LF for a certain period of time while charging and during discharging the current drawn from the LF or a capacitive load. This current creates an output voltage variation in the LF circuit. The association of the CP circuit and the LF converts the logic states generated by PFD into an analog voltage V_{ctrl} for controlling the VCO. The resulting output voltages are then converted into frequency values by the VCO [5-8]. A basic charge pump architecture is shown in the Figure. 9.

The requirements of an effective CP are as follows:

- Equal charge/discharge current at any CP output voltage
- Minimal charge-injection and feed-through (due to switching) at the output node
- Minimal charge sharing between the output node and any floating node, i.e. MOS switches at off position.

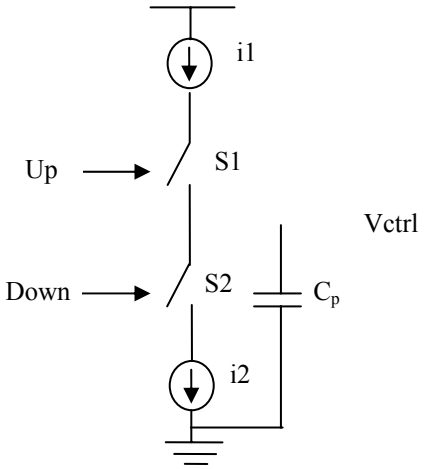


Figure. 9 Basic architecture of Charge Pump

Figure. 9 shows the combined architecture of the CP and LF. Current sources i1 and i2 are identical. The two outputs of PFD are given to the UP and DOWN inputs of CP respectively. Capacitor Cp serves the purpose of the loop filter.

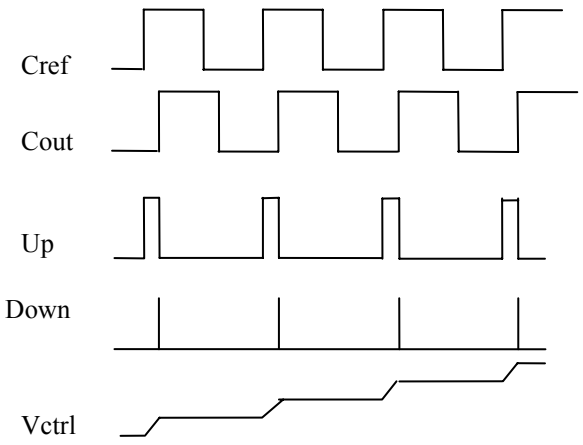


Figure.10 Operation of PFD with Charge Pump

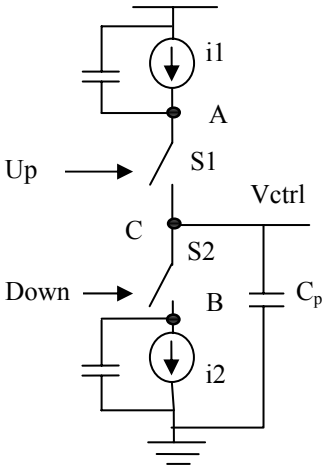
Charge pump is driven by a PFD. The PFD controls the switches of CP such that the output voltage of PFD is converted into the current. PFD is driving the CP where phase of Cref is leading phase of Cout. In that case PFD generates longer UP signals than DN signals and voltage across capacitor C_P (Vctrl) increases. The combined operation of PFD with charge pump, the input and its corresponding output is as shown in the Figure. 10.

4. PROPOSED CHARGE PUMP

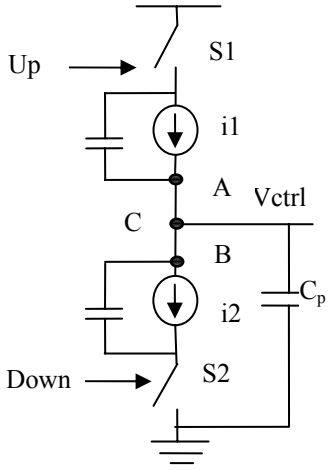
In addition to the power and delay the other major defy while designing PLL is the reduction of reference spurs.Reference spurs are due to the current mismatching which refers to the magnitude difference of charging and discharging currents. Three main factors causing the mismatches are as given below.

- Asymmetry of the current sources of the charging and discharging loop filter
- Current source mismatches caused by different output voltages
- Current pulses occurring randomly once the UP/Down switches are turned on.

Usage of common current source reduces the first two factors. The S1 and S2 are the MOS switches. The non-ideal behaviour of MOS switches brings about charge injection and clock feed through errors that cause periodic ripples on the control line. Smaller sized MOS switch can be used to reduce the effects of clock feedthrough and charge injection.

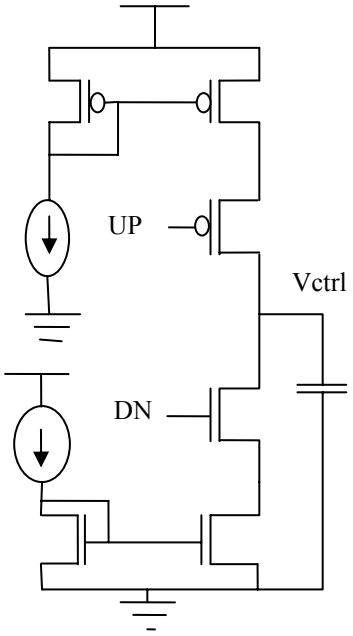


(a)

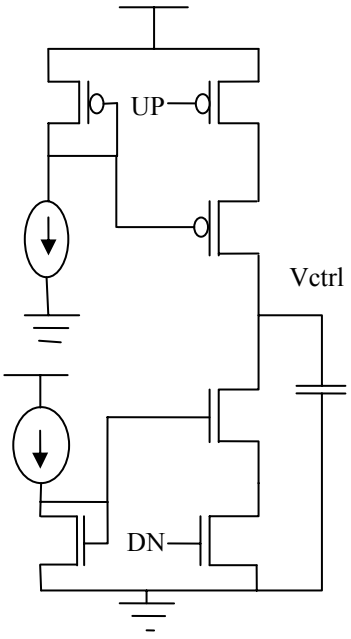


(b)

Figure. 11 (a) Position of switches in CP [9] (b) Position of switches in proposed CP



(a)



(b)

Figure. 12(a) Charge Pump [9] (b) Proposed Charge Pump

In addition to above two problems, charge sharing is another crucial problem that causes current mismatch. Current sharing originates from the finite capacitance at the

Current Source and Current sink sources. The Figure. 11 (a) and (b) shows that A and B represent the current source terminals of charge pump, and C is the load terminal node. Whenever both switches (S1 and S2) are off, neither i1 nor i2 outputs the current resulting in different voltages at nodes A, B and C. Because when both the switches are off voltage at A is charged to Vdd and a voltage at B discharges to ground. The switches are then turned on again, the charges on Cp are redistributed to the parasitic capacitances of the current source and current sink leads to the ripples on the output voltage of Cp (Vctrl) and directly causes serious jitters to the VCO.

The non-ideal effects of the CP shown in Figure. 12 (a) can be reduced by choosing the position of switches carefully. In the proposed charge pump design we exchange the positions of switches and current sources .The Figure. 12(b) represents the proposed charge pump in which the position of switches and current sources are switch overed. It also represents that charge injection and clock feedthrough caused by switches will not directly influence the output voltage. In addition, as the terminals A, B and C are at the same point the charge sharing phenomenon is also decreased.

5. RESULTS AND DISCUSSIONS

All the conventional and proposed PFD and CP designs are simulated using Tanner EDA tool to verify their functionality. The power and propagation delay of the designs are valuated using H-Spice at a supply voltage 2.0V using 180 nm standard technology.

DFFPFD consume less power among all PFD i.e 79 μW but the propagation delay of the design is more. Therefore the power delay product (PDP) of this design is high among them.

DFFPFDCONAND shows lowest PDP value among all the PFDs. The propagation delay of this design is 32.81 ps.

The structure of the PFDs using AND gate is same as Figure. 3 uses different flip flops. The structure of the PFDs using NOR gate is same as Figure. 4 uses different flip flops and NOR gate is designed using different technologies like CMOS, TGCMOS, MUX and GDI Technique.

The power and delay analysis of various Conventional and Proposed PFDs is tabulated in Table 1. It also gives the information of D- Flip flops and Logic gates are used in different PFDs. Every PFD design has its own advantage and disadvantage. Based on requirement designers may choose the suitable one.

The simulation results of CP PFD are given in Table 2. The proposed CP PFD has little more propagation delay than existing. Therefore the lagging creates to reach the outputs at same time which avoids the mismatch currents of CP.

Table 1 Power and delay of the different PFD designs

DESIGN NAME	Power (W)	Delay (sec)	PDP	Flip flop	Logic Gate	No.of MOS Devices
DFFPFD[4]	7.9089E-05	2.0859E-08	1.6497E-12	7(Modified DFF)	NO GATE	16
DFFNOR (PROPOSED)	5.6422E-04	1.1031E-10	6.2239E-14	7(Modified DFF)	NOR	20
PFDNORGATEUSINGGDI (PROPOSED)	5.0674E-04	2.3184E-10	1.1748E-13	8(DFF used for Dynamic PFD)	NOR	20
DYNPFD	8.1215E-04	4.8158E-10	3.9112E-13	8(DFF used for Dynamic PFD	NOR	20
DFFPFDCONAND (PROPOSED)	3.2379E-04	3.2815E-11	1.0625E-14	7 (Modified DFF)	AND	22
DYNAND (PROPOSED)	2.9854E-04	8.4208E-11	2.5139E-14	8(DFF used for Dynamic PFD	AND	22
TRDPFD[4]	3.4374E-04	3.0517E-10	1.0490E-13	6 (DFFFORTRD PFD)	AND	22
TGCMOS PFD (PROPOSED)	7.0651E-04	2.8203E-10	1.9926E-13	8(DFF used for Dynamic PFD	NOR	24
DYNPFDMUX (PROPOSED	8.1448E-04	3.0183E-10	2.4583E-13	8(DFF used for Dynamic PFD	NOR	28

Table 2 Simulation results of PFD using TGCMOS and Charge Pump

Design	POWER (mW)	DELAY (ns)	Delay to Up (ns)	Delay to Down (ns)
TGCMOS PFD+CP	79.243	30.908	32.117	29.549
TGCMOS PFD+ Proposed CP	80.036	44.474	32.358	29.027

6. CONCLUSIONS

Phase Frequency Detector is the one of the vital block of the PLL design. PFD broadly affects the performance and power consumption of the PLL. To meet the low power and high speed PLL, different PFDs performance are evaluated. The PFDs are proposed with the above said specifications using AND and NOR gates with different flip flops. The proposed PFDs with W/L ratio show power optimized than the conventional designs.

One of the major nonlinearity mechanisms in charge pump is the mismatch of the up and down currents due to device mismatch and finite output impedance. Hence, a design with a simple added delay in the charge pump with PFD is proposed and simulated. The results show that the proposed CP shows a little more propagation delay with the existing CP. This leads to overcome the currents mismatch between UP and Down currents.

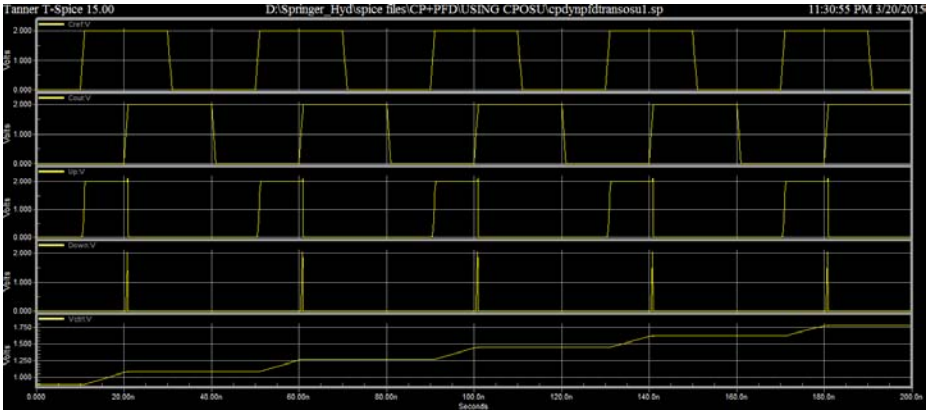


Figure.13 Cref leads Cout-Charging

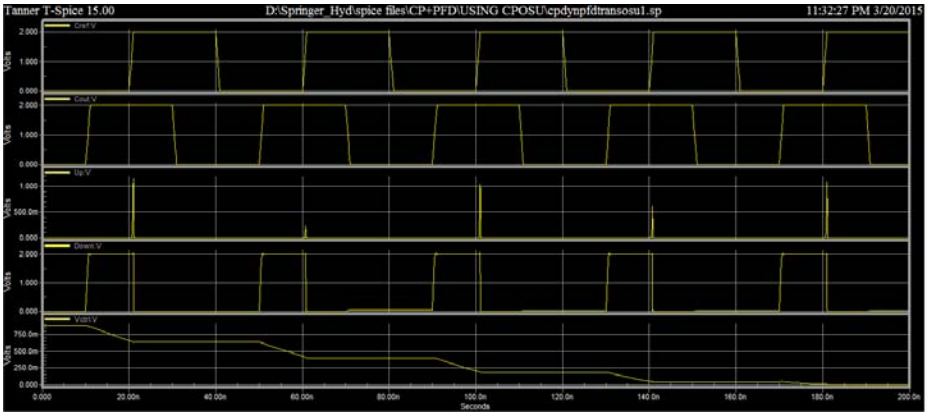


Figure.14 Cout leads Cref-discharging

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