IJCTA, 10(02), 2017, pp. 217-225

Modified Nine Level Inverter with Reduced Number of Switches

Thiyagarajan V.* and Somasundaram P.**

Abstract : Multilevel inverters are used in high power and medium voltage applications as it offers less distortion and electro-magnetic interference. This paper proposed a new symmetric multilevel inverter with reduced number of switches and DC voltage sources. The proposed inverter topology produces nine level output voltage waveform using two DC sources and seven switches. The advantage of this topology is it reduces the size and cost as it uses minimum number of components. The proposed inverter is simulated using MATLAB/Simulink software. It is analysed for different switching angle calculation methods and the results are presented.

Keywords : Multilevel inverter; PWM; THD; H-bridge; Symmetric.

1. INTRODUCTION

Multilevel inverters has been introduced in 1975 [1]. The multilevel inverters uses power switches with several DC voltage sources. The multilevel inverters are grouped into two categories, namely, symmetric and asymmetric multilevel inverters. In symmetric, the magnitude of all DC voltage sources are same. However, in asymmetric, it is different. The DC voltage sources may be renewable energy resources, capacitors or batteries. Multilevel inverters has various advantages such as low distortion, high power quality, low dv/dt stress and minimum switching losses [2]. The major drawback of the multilevel inverter is it requires greater number of power semiconductor switches to achieve higher number of output voltage levels. Consequently, it also increases the number gate driver circuits. The multilevel inverter was started with three-level inverter topology and then several topologies have been developed in recent years. The most popular topologies of multilevel inverters are diode-clamped, flying capacitor and cascaded H-bridge inverters[3-5]. Nowadays, many researchers has focused on developing new topologies of multilevel inverters and modified pulse width modulation (PWM) techniques.

The Ref. [6-11] presented different PWM techniques based multilevel inverters. The different PWM techniques used for multilevel inverters are carrier based pulse-width modulation (PWM) [6], space vector modulation (SVM) [7], staircase modulation (SM) [8], selective harmonic elimination pulse width modulation (SHE-PWM) [9] and selective harmonic mitigation PWM (SHM-PWM) [10,11].

The Ref. [12-15] proposed different topologies of multilevel inverter. A symmetric five level inverter has been presented in [12]. This topology uses two DC voltage sources and eight switches to generate five level output. The main drawback of this topology is it has not been extended to higher voltage levels. Another type of multilevel inverter is proposed in [13]. This topology produces multilevel output voltage by using the series and parallel connection the DC voltage sources. This topology lowers the number of power switches compared with the cascaded H-bridge inverter. In [14], sub-multilevel inverter units are connected in series to achieve multilevel output. This inverter can be used as symmetric and asymmetric

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modes. Three different algorithms has been proposed for the determination of magnitudes of DC voltage sources. This topology uses fewer switches and gate driver circuits but the major drawback is it require multiple DC sources and high peak inverse voltage. A symmetric multilevel inverter consists of isolated DC voltage sources is presented in [15]. In this topology, the DC sources are alternately connected in opposite polarities through power switches. However, the maximum number of output levels depends on the number of sources.

This paper proposes a modified symmetric nine level inverter with reduced number of switches. The proposed multilevel inverter uses two DC voltage sources, three main switches and four switches for full bridge inverter. Section I explains the modes of operation of the proposed nine level inverter. The different methods of calculating the switching angles are given in Section III. The simulation results obtained using MATLAB/Simulink are presented in Section-IV.

2. PROPOSED MULTILEVEL INVERTER

The proposed nine level inverter is shown in Fig. 1. It consists of two DC voltage sources, three main switches and four switches of full bridge inverter. The proposed inverter consists of two parts: level creator part and polarity changing part. The function of level creator part is to generate different output voltage levels in same direction. The direction of this output is changed by the polarity changing part. Here, full bridge inverter is acted as a polarity changer. The MOSFETs are used as main switches.

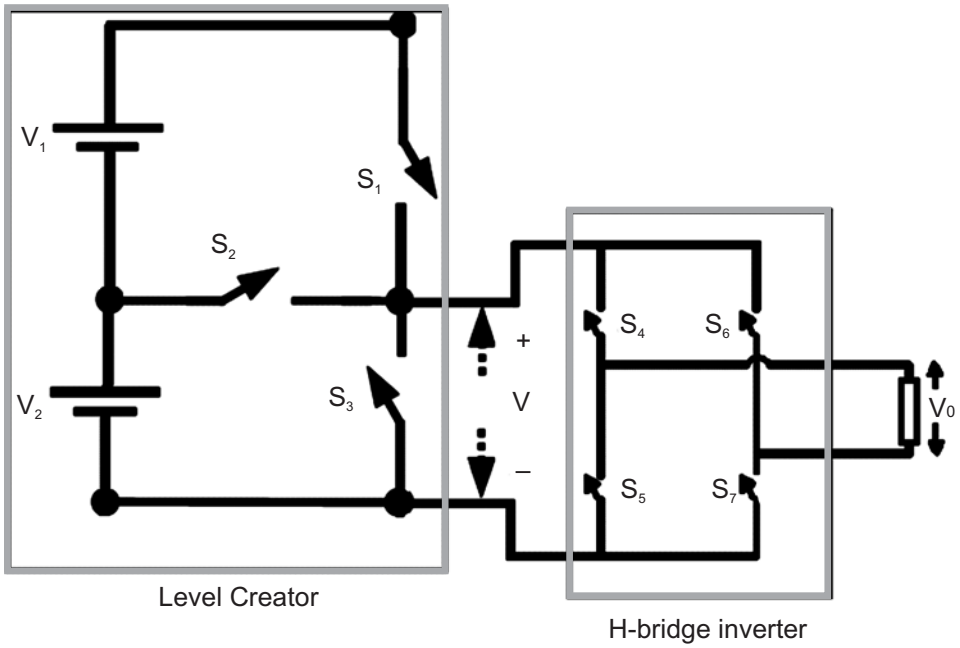


Figure 1: Proposed Nine-level Inverter

The switching states for the proposed nine level symmetrical inverter is given in Table 1.

3. CALCULATION OF SWITCHING ANGLES

The switching angles corresponding to the period 0 to $\pi/2$ are called as main switching angles. For nine level inverter, there are four main switching angles given by θ_1, θ_2, θ_3 and θ_4. The other switching angles are easily obtained using the following relations[16].

1. For the time period 0 to $\pi/2$ $= \theta_1$, θ_2, θ_3 and θ_4.
2. For the time period $\pi/2$ to $\pi = \pi - \theta_1$, $\pi - \theta_2$, $\pi - \theta_3$ and $\pi - \theta_4$.
3. For the time period π to $3\pi/2$ $= \pi + \theta_1$, $\pi+\theta_2$, $\pi + \theta_3$ and $\pi + \theta_4$.
4. For the time period $3\pi/2$ to $2\pi = 2\pi-\theta_1$, $2\pi-\theta_2$, $2\pi - \theta_3$ and $2\pi - \theta_4$.

Table 1

Switching states

Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$2V_{dc}$	1	0	0	1	0	1	0
$3V_{dc}/2$	1	1	1	1	0	1	0
V_{dc}	0	1	0	1	0	1	0
$V_{dc}/2$	0	1	1	1	0	1	0
0	0	0	1	1	0	1	0
$-V_{dc}$	1	0	0	0	1	0	1
$-2V_{dc}$	1	1	1	0	1	0	1
$-3V_{dc}$	0	1	0	0	1	0	1
$-4V_{dc}$	0	1	1	0	1	0	1

The switching angles of proposed nine level inverter is shown in Fig. 2. The different methods used to calculate the four main switching angles of the proposed nine level inverter are given below[16].

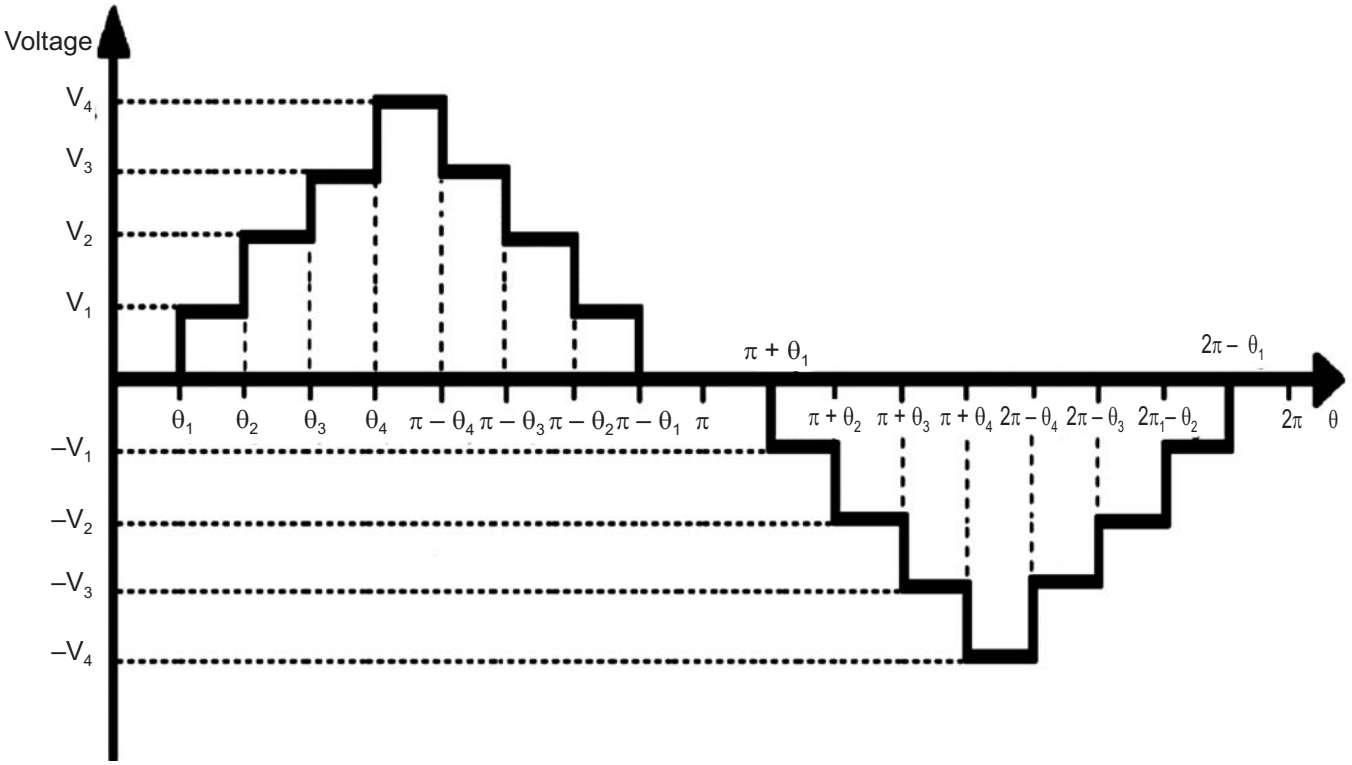


Figure 2: Nine Level output waveform

Method – 1 $$\theta_j = \frac{1}{2}\sin^{-1}\left(\frac{2j-1}{n-1}\right)$$

where, j = 1, 2, 3 and 4

Method – 2 $$\theta_j = j\frac{180^\circ}{n}$$

where, j = 1, 2, 3 and 4

Method – 3 $\theta_j = j\frac{180^\circ}{n+1}$

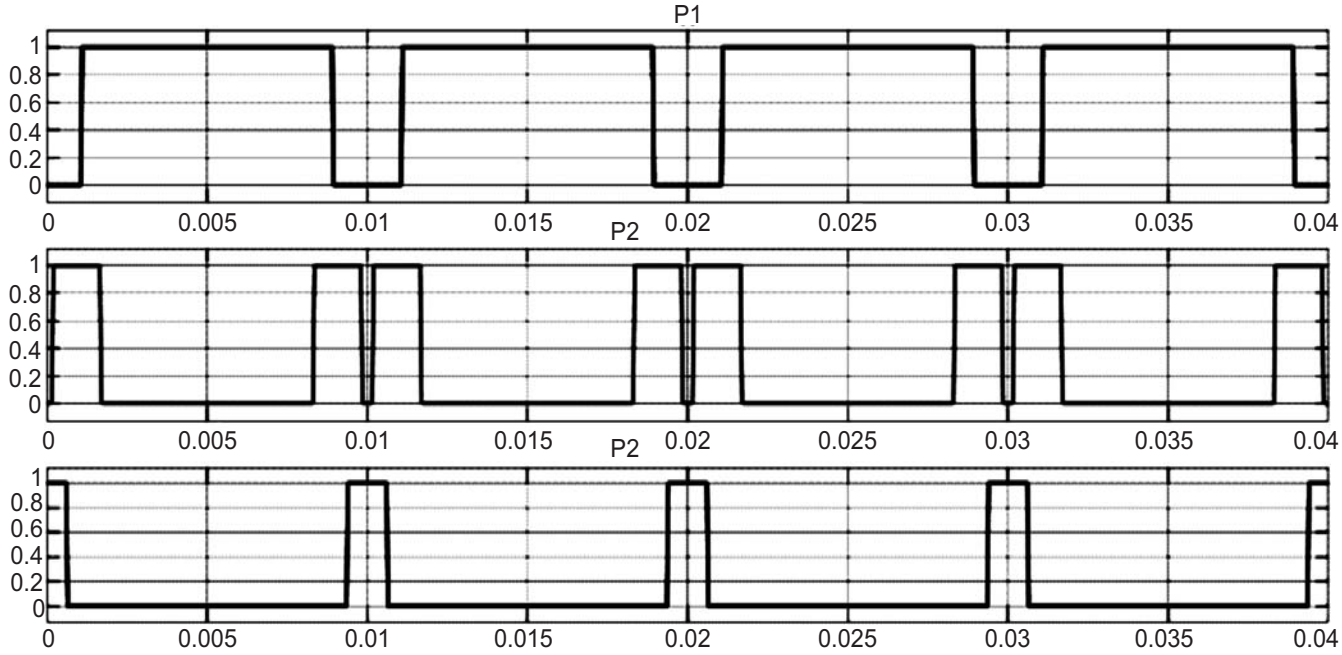
where, j = 1, 2, 3 and 4

Method – 4 $\theta_j = \sin^{-1}\left(\frac{2j-1}{n-1}\right)$

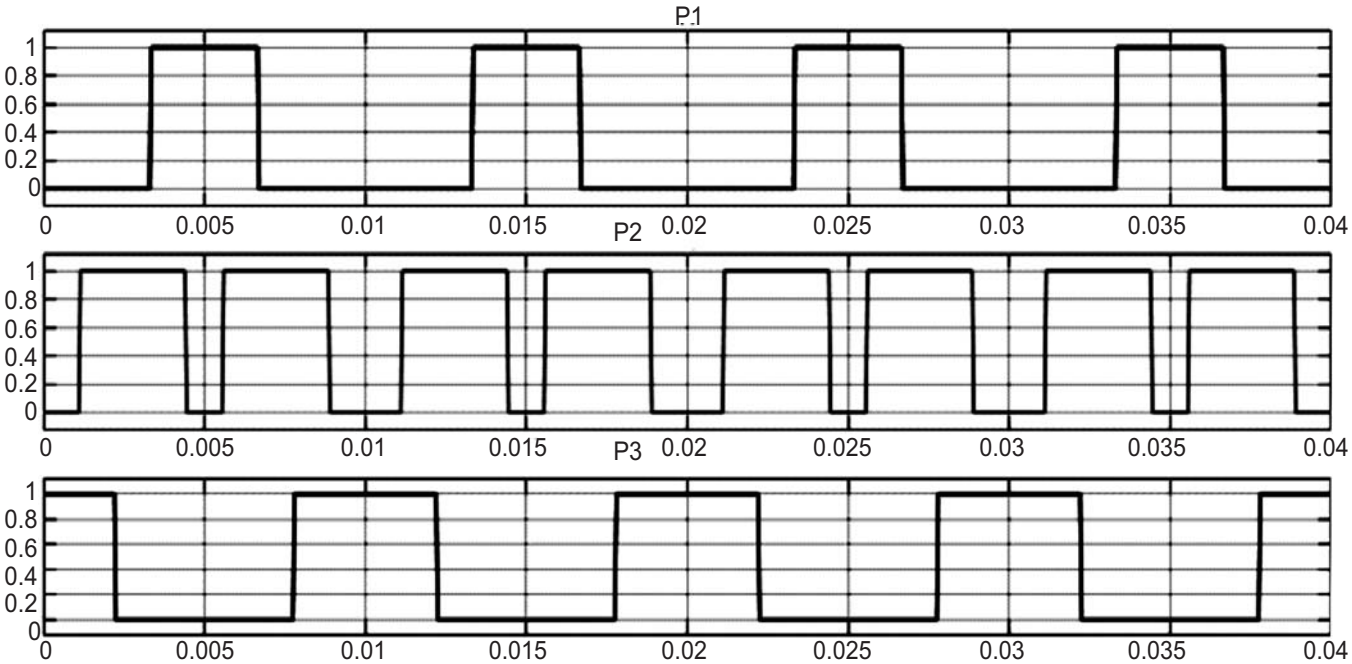
where, j = 1, 2, 3 and 4

The output voltage of the proposed nine level inverter is shown in Fig. 2.

The switching pulses obtained using the different methods are shown in Fig. 3.



(*a*)



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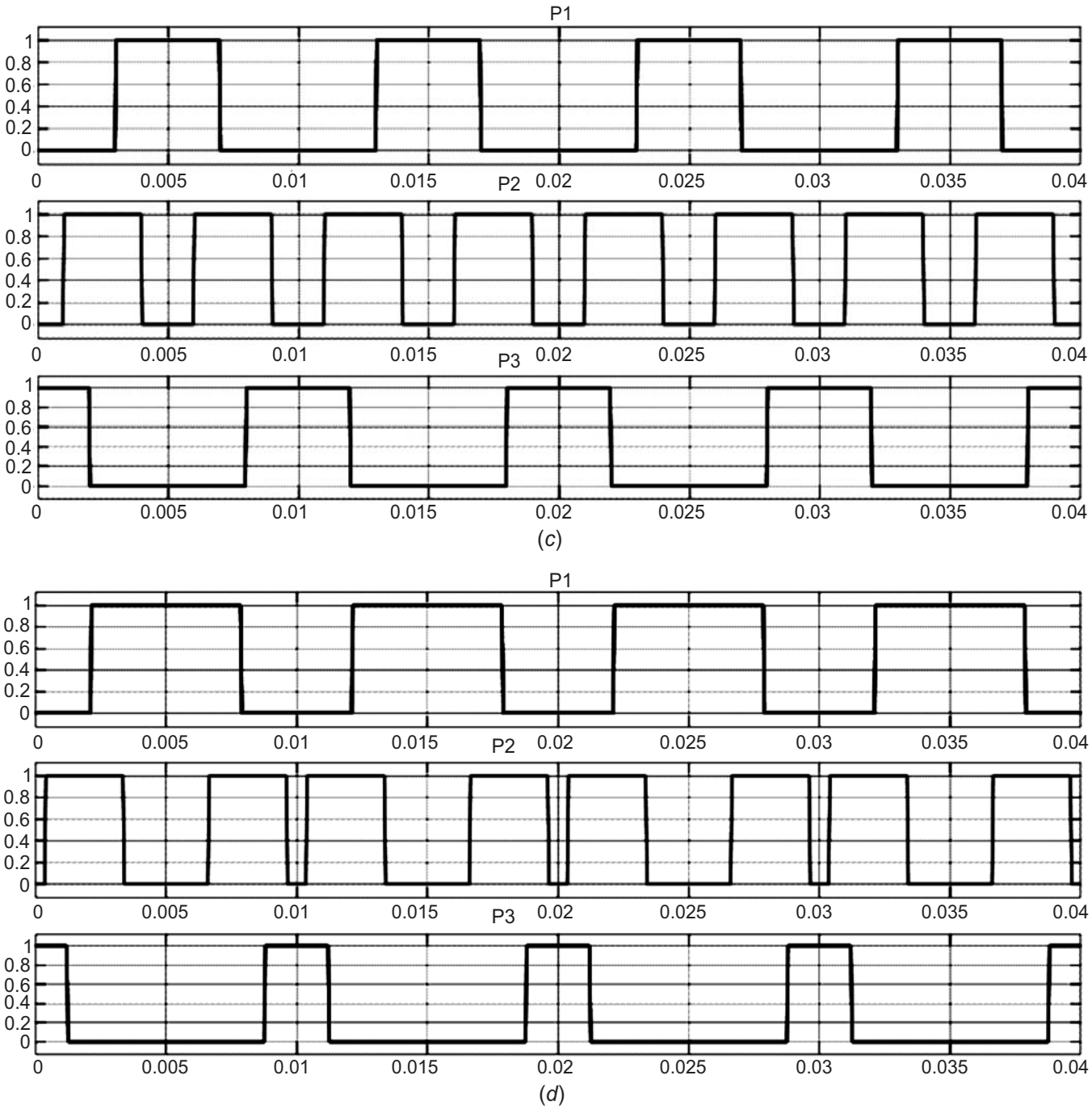
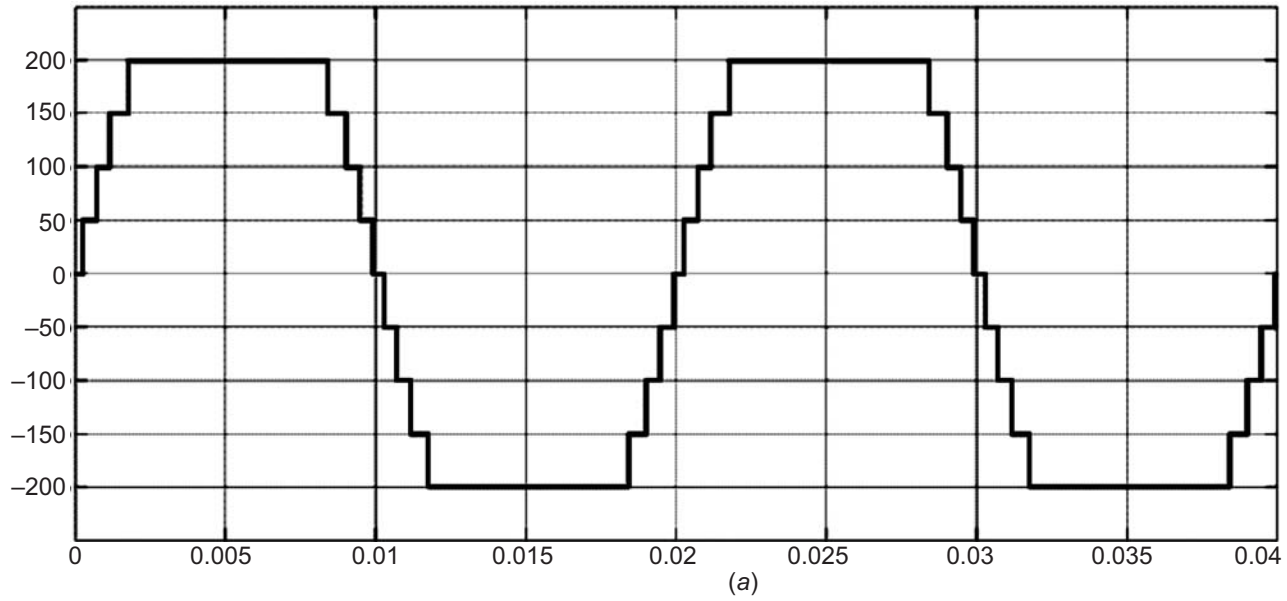


Figure 3 : Switching Pulses (*a*) Method – 1 (*b*) Method – 2 (*c*) Method – 3 and (*d*) Method – 4

4. SIMULATION RESULTS

The simulation results of the proposed nine level inverter are presented in this section. The proposed inverter consists of two DC voltage sources of values $V_1 = V_2 = 100$ V. The output voltage obtained for different switching methods of the proposed inverter are shown in Fig. 4. It is observed that the maximum voltage is obtained as 200 V (*i.e.*,$V_1 + V_2$) for all methods.

The result shows that the output voltage of the inverter is the staircase waveform. Fig. 5 shows the FFT analysis of the output voltage waveform for different switching techniques**.** The result shows that the harmonic content of the output voltage waveform for the switching method - 4 is less when compared with the other methods and the results are compared in Table 2.


200
150
100
50
0
–50
–100
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–200
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0.005
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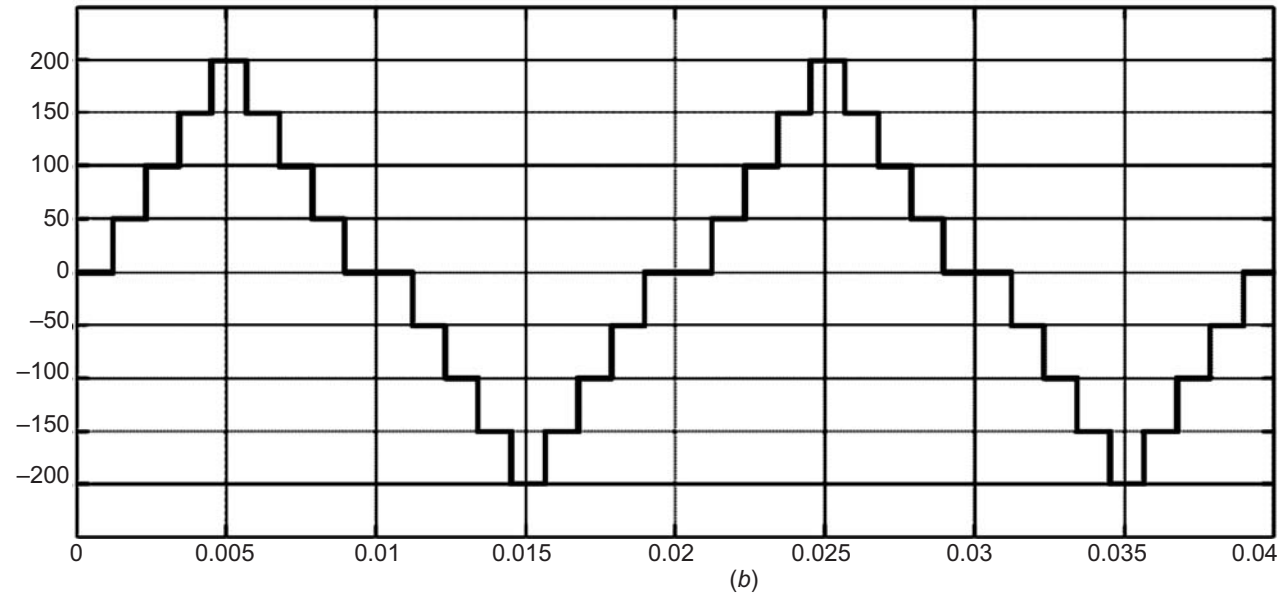
0.025
0.03
0.035
0.04

(*a*)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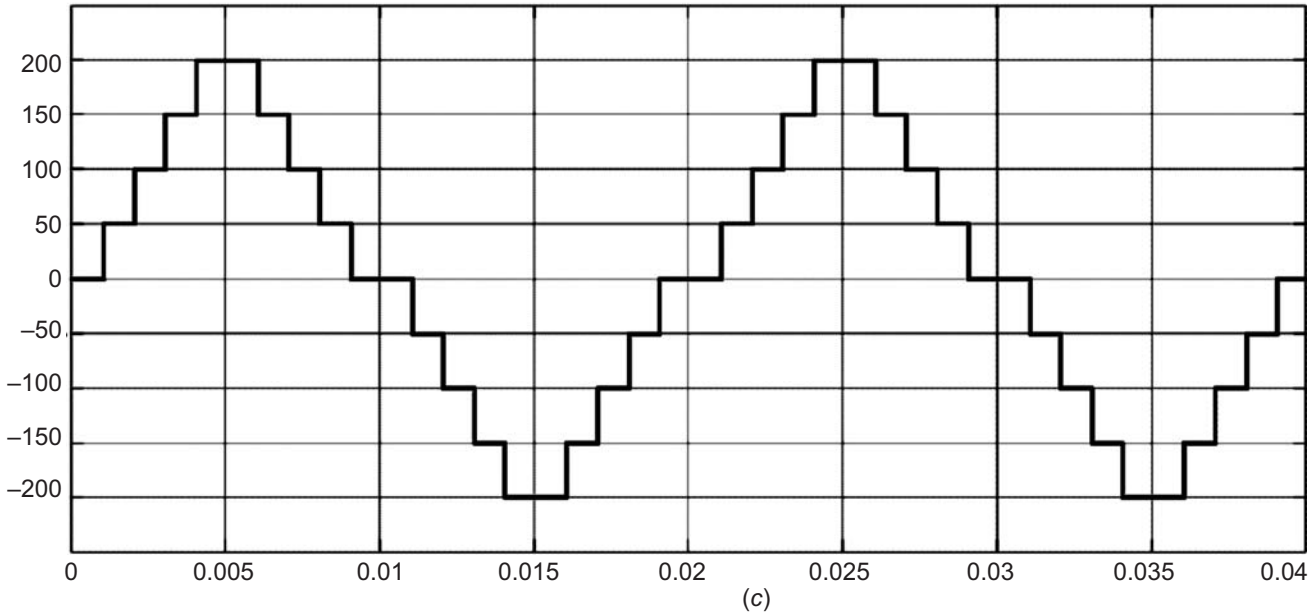
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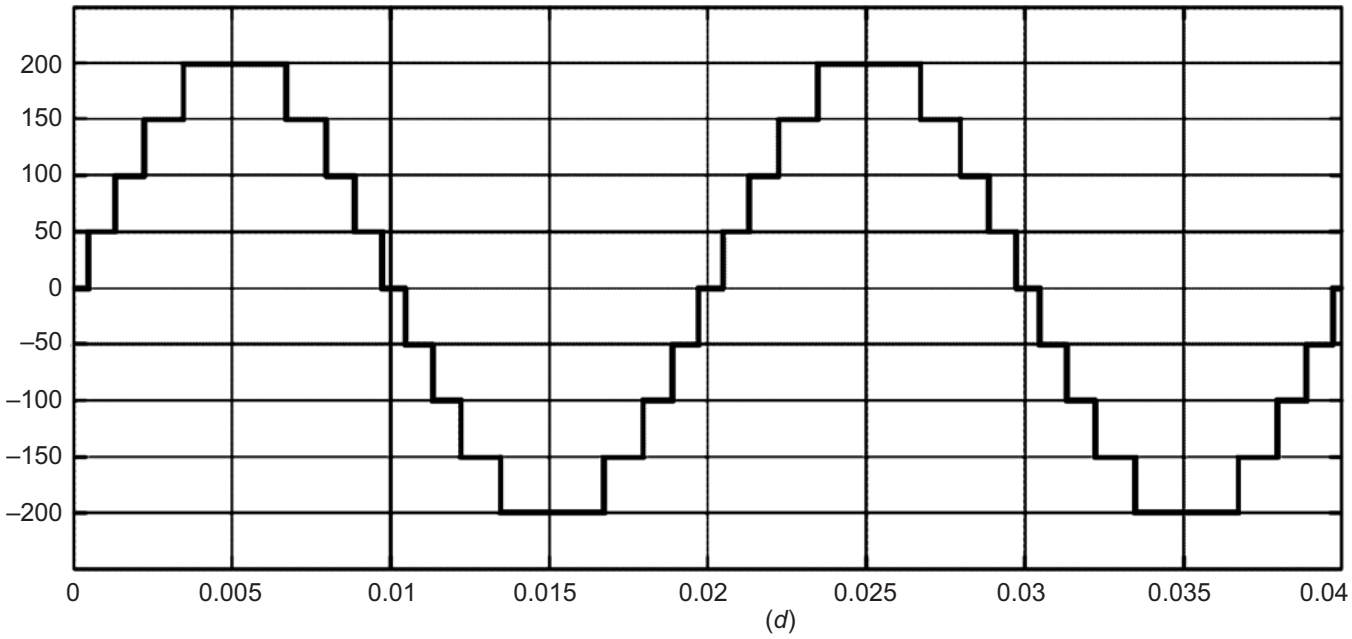


Figure 4: Output Voltage (*a*) Method - 1 (*b*) Method - 2 (*c*) Method -3 and (*d*) Method - 4

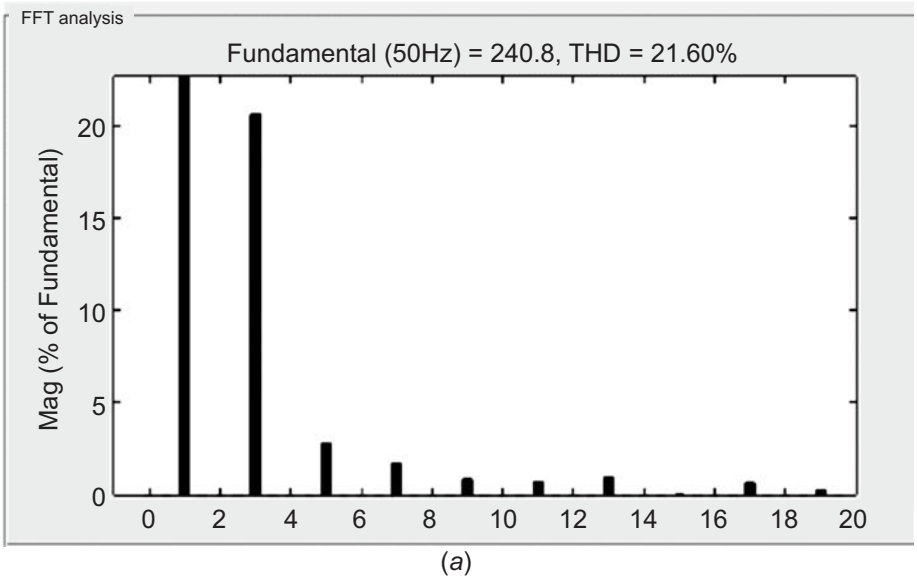
Table 2

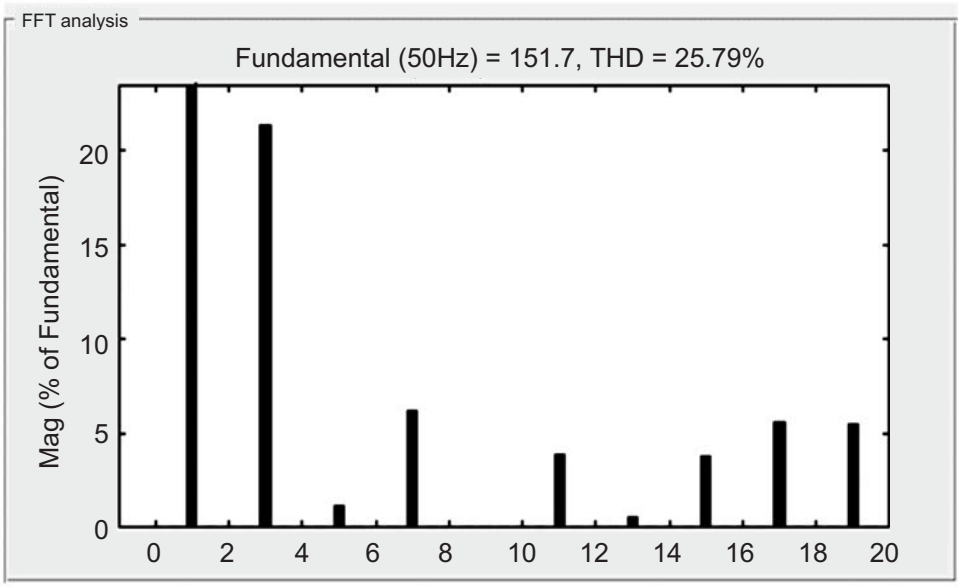
Comparison of Total Harmonic Distortion

Method	*THD (%)*
Method - 1	21.60
Method - 2	25.79
Method - 3	22.04
Method - 4	9.29

5. CONCLUSION

This paper proposed a new nine level inverter with the reduced number of switches. The main advantage of this inverter topology is it uses only two DC voltage sources to achieve nine level output voltage as compared with other conventional topologies. The four different methods are presented to calculate the switching angles. The proposed inverter is simulated for these four different methods and the results are presented. The result shows that the method - 4 achieves less THD compared with other methods. The number of level creator part can be added in series to increase the output voltage levels.





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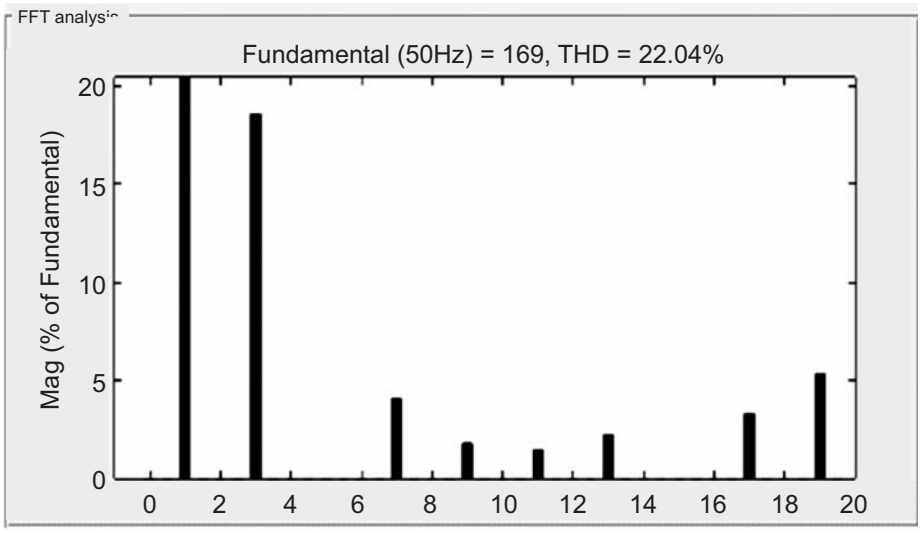

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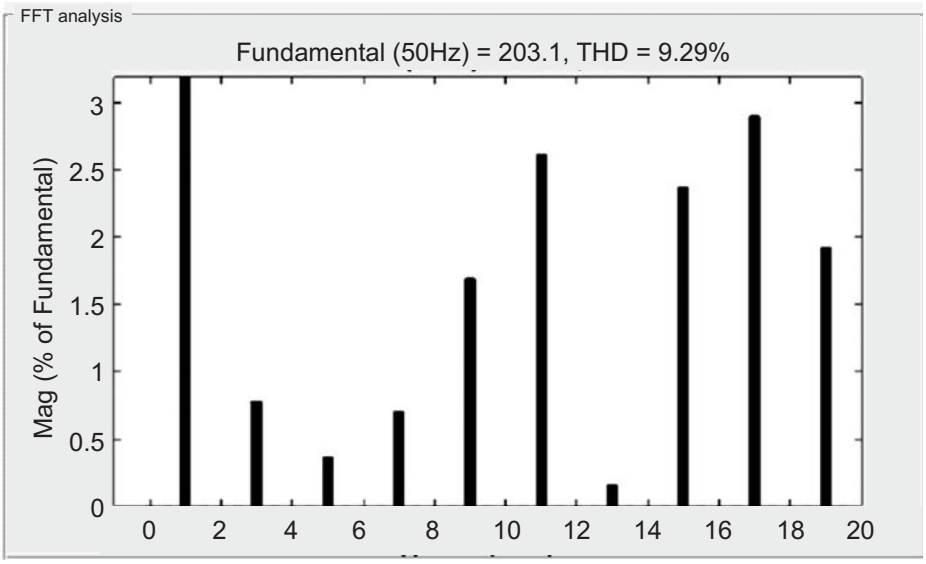

(*d*)

Figure 5: FFT Analysis (*a*) Method - 1 (*b*) Method - 2 (*c*) Method - 3 and (*d*) Method - 4

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