An Efficient and Low Power Reconfigurable Network-on-Chip

Venkata Sridhar Thatiparthi[1] and G. Chenchu Krishnaiah[2]

[1] *PhD Scholar, ECE Department, Visvesvaraya Technological University, Belgaum, India*
E-mail: venkatasridhar.thatiparthi@gmail.com
[2] *Professor of ECE, Gokula Krishna College of Engineering, Sullurpeta, India, E-mail: krishna.rakesh4@gmail.com*

Abstract: Network on Chips (NoC) were turning the main state- of-art in designing with scalable System on Chips with large band-width applications. Presently available Network on Chips are not much enough flexible for supporting advanced communications which timely changing their behavior (capacity, concurrency) innate with the increasing majority of today's embeddedsystems. Only a limited number of solutions exist in the field of Network on Chip with reconfigurability in different techniques, but, to the maximum of our understanding, many of them have clear and reconfigurable design methods. Firstly, in this paper, we will present a survey of reconfigurable chip existing methods as our starting interest in this area for research, then we propose a suitable methodology. Hence, to distribute with current scenario we start with the explanation of dynamic(timely) reconfigurable modle for Network on Chip. And list many outstanding research topics organized in 3-discussions as: (1) The Dynamic_reconfigurable_Administrations, (2) The Network rules(Protocols) reconfiguration and (3) The Network_Infrastructure_Reconfigurations.

Keywords: NIU: Network_Interfacing_Unit; NoC: Network on Chip; SoC: System_on_Chip; OSI: Open_System_Interconnect ; CAD: Comuter_Aided_Design; DR: Dynamic_Reconfiguration; NA: Network_ Adaptor; TDMA: Time_Division_Multiple_Access; SDMA: Space_Division_Multiple_Access.

I. INTRODUCTION

Earlier any network connection and sharing of data can be done through the external medium (modem, wired). Mostly, if one wants to connect to the internet, he/she is required to go with a modem/router to do so. As the demand for the use of electronic appliances drastically increasing the need for maintaining a number of hardware modules also increases tentatively. As one cannot maintain many hardware modules in the limited place in a single time, the requirement of making them on a single chip is the basic idea behind designing for System on Chip(SoC)[2,3,4]. And network on chip will provide the basic connections between different modules inside SoC. But the concept of multiple network maintenance and connecting to same had become a challenging job for networking engineers/developers. Now to maintain many individual bodies (modules or circuits) in a single system and connecting them with various networks is a tedious task. The Reconfigurable NoC architecture provides a better solution to the same. Hence support many programmable devices(PD) can be integrated on a single chip.

Many manufacturers were already approved to accept Reconfigurable NoC(RNoC) [5]for dynamic characterization of a communication network. Designing such NoC based on (using) CAD may, subject to increase the cost of the device. Hence, proper justification is required for worst case considerations. Thus the new design of NoC will provide a better solution to the above stated problem, as it can be configured to the maximum possible changes in the communication network dynamically. Hence, it is assumed to be a new window is opened for researchers with reconfigurable, flexible networks and PDs as a platform. The main theme of this write-up is to enlist some fundamental discussions on RNoC design, in accordance with OSI dynamic requirements, proposing a model for dynamically reconfigurable (DR) NoC[1, 5-8]. In this write-up firstly we present a novel model for dynamically reconfigurable NoC, later we come up with superlative research topics and recommend few open complications.

II. NOC RECONFIGURABLILITY METHODOLOGY

In continuity with the introduction, we now present OSI (Open System Interconnect) required RNoC based on dynamic reconfiguration and explain the layered concept based view.

(A) Driving model for reconfiguration

The word Embded-System became most predominant term in the field of communications now a days. As truly speaking the term embedded system in which both hardware and software are physically separate, but both depend on each other for functionality. At the time of manufacturing an embedded communicating hardware, it may not be possible to assume all operating conditions of (timely behavior of communication networks) communication network provider. Sometimes it is required to dynamically update the protocol of a particular network for efficient usage. Thus the embedded communicating device architecture should be in a position to support the timely updating softwares. As an example, adapting to both 1G, 2G, 3G to 4G on an LTE enabled communicating terminal equipment (antenna has to be matched to bandwidth availability dynamically).

Thus the developer/designer should keep in mind while designing, that to allow the architecture for dynamic adaptation of Hardware (Reconfigurable PDs) and Software (protocols) running conditions without degrading the system performance. This idea is the base for Dynamic Reconfiguration (DR)[9-11].
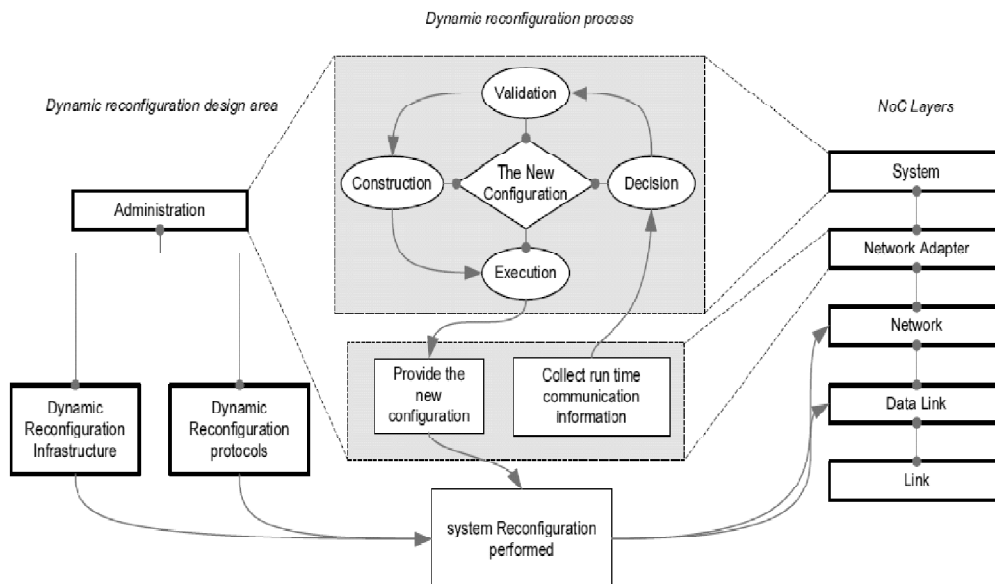

Figure 1: Shows dynamic reconfiguration working principle and procedure for RNoC as per OSI-layers

(a) *Explaining The Possibility*: A system can be defined as a combination of many elements (complex circuit as per hardware) connected together, which may work with individual or group data (inputs), might be logical or physical (binary or voltage). Thus reconfiguration means changing its architectural connections or protocol execution process (example, an addition operation with or without carry in ALU), which require additional hardware or software. Hence, the possibility of the above is the main concern with the design of architecture (Reconfigurable PDs).

Thus the reconfiguration is achieved according to the variations in the specifications, like summing a component and configuring or subtracting it.

(b) *The Layout Administration (Management)*: The layout administrator (configuration manager) interprets the required specifications need to change according to parameters and hardware structure. Thus the interpreter requires the current status of the system. Hence, updates may be read from the administrator and modify continuously according to the different subsystem of the system.

(c) *The Running Procedure*: In general the OS configure, develop and install all modifications and requirements in a system, as per the directions given by the layout administrator (Configuration Manager). But the finalization(decision-making) cannot be achieved by this DR method, since it depends on the decision of developer blueprint of Dynamic Reconfiguration (DR).

As to make it completely independent and decision-making, we include a state-of-the-art level concept to this (b), by combining a decision process of DR. The above Fig. 1. Shows our idea of DR for Network on Chip. By this we expect the system (layout administrator) will become, decision making, according to the dynamic changes in the communication network and reference inputs tentatively.

(B) Design based on OSI- Layers

The study of computer networks, modified OSI-layer model (simplified) and with respect to the study form references (survey), it is clear that no new protocols are required for all layers to communicate amongst with the interface as NoC. That means the simplified model of OSI will easily adopt the NoC usage with much flexibility. But it is required to specify what attain by the network at all levels. We expect this type of a system to use, as it can be easily interconnected miscellaneous (heterogeneous) systems according to the changes in the communication networks. This can be achieved only with the modification of some OSI-layer protocols[13-15]. Thus, Dynamic Reconfiguration of Network on Chip can be achieved. The above Fig. 1. Illustrate the process of achieving DR on NoC with respect to the characterization and operating conditions of different NoC layers.

System: This is the main functioning unit of reconfiguration. With its universal network architecture and wide comprehension of applications, it can achieve the decision-making for new configurations with validation and implementation.

Network-Adapter: The dynamic updating between Network and IP can be handled by this. The big cache which it contain, allow it to implement the newly happened changes in the network (communication) to allow or block & reject to DR.

Network: This is the path provider for the communication (routing) according to the type of connection (topology) of the network. Thus DR can modify these layers:

(i) Topology.

(ii) Routing procedure.

(iii) Switching method.

The Dat-Llink: Handling of data packets for transceiver operation is the main task of this link. And DR at this level can manage data swap protocol across routers. Multiplexing methods like Time division and Space

division (TDMA & SDMA) [16]multiple access, with error detection techniques like hamming or cyclic redundancy check. Here we propose a DR model for NoC, shown on the left hand side of fig. 1. with three dimensions. Firstly the management method (dynamic design, evaluation and running) of DR, which can be combined at different levels of the system or NA. Secondly, and finally justify (analyze) the changes that happened with respect to DR introduction.

III. DYNAMIC RECONFIGURATION

(A) Denotation

The major work carried by this administrator is to maintain each and every element in the connected network, with respect to public (global) configuration. The fulfillment of this administration is achieved when meeting the constraints of QoS, which indirectly controlling the output and capacity of the network with priority. This layout administrator plays a critical role as it is accountable for management. Hence, it has to satisfy the following for keeping the DR & running time reconfigurations:

(i) The QoS is the most important aspect along with consistency. The design has to give an assurance that the DR will not lead to incoherence or degrade the network.

(ii) When a system meets a requirement to update or DR required for multiple components parallel, it should withstand assuring QoS. Hence, the implementation of multiple DRs may require more time. The execution and implementations with decision-making has to be dynamically maintained.

(iii) As DR will allow hardware expansion, at the same time updating of associated software/firmware also required to run that added hardware efficiently. And the same has to be updated in the network for data exchange.

(iv) Errors/Disturbances should be kept minimum possible. The DR design should be friendly to reduce the hardware complexity without overloading the existed elements of the network.

(B) Existing Methods Presently

Except a very few approaches as studied from references, most of the existing methods do not combine the administration (management) module to the system for RNoC. Some methods studied will allocate few protocols, which reduces the number of standing data (packets) in NoC. So an extra manager (module) is required to be implemented for for maintaining this constrain at NoC.

The stack manager of the communication network permit the operating system to control the slot (time) allotted to them in their packet for transceiver function. Further the NoC path can also be controlled by the OS. But there is a problem with this DR at runtime. As it is implemented at runtime of a network, it may cause termination of total traffic, which leads the network to be idle for the whole period of reconfiguration. And also burdon (cost) over the system design also increases as a separate module has to be maintained for collecting and holding the traffic updates from NIU, as shown in Fig. 2. So we can conclude that no specific assumption is made in configuring the size of the modules which access the communication network.

(C) Scope for Research

The so called DR is worthy if it follows the protocol of consistency, QoS, deputation and interface (at channel). For achieving above said, it is required to share credentials between the administrator (like Operating System) and components in the network (like Network Adaptor). Accordingly administrator will have to perform observation, control, and involve only incomplete reconfiguration of the communication network.
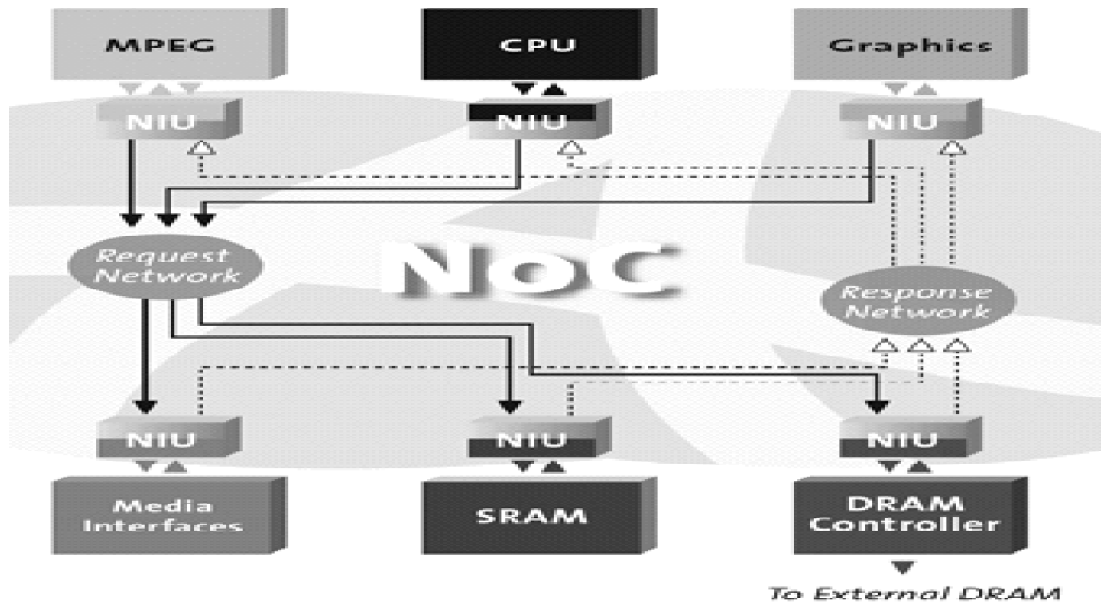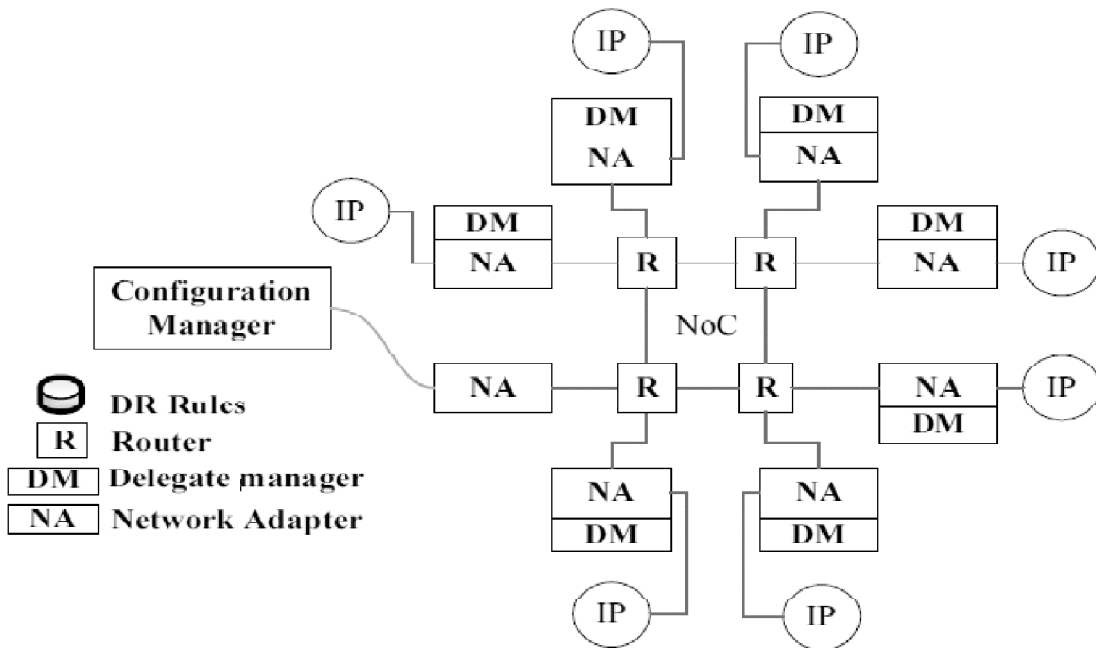
Figure 2: Dynamic Network Interface via NoC

Figure 3: Layout administration bifurcation for DR of Network on Chip

The network elements (components) sometimes can handle, reconfigurating certain procedures (like holding capacity, ordering, multiple access arrangement). Hence, this method of dynamic reconfiguration management contains dispensation and deputation of administration. With reference to above Fig. 3. The DM resolve, ratify and attain a certain level of reconfiguration in accordance with the conditions given by the master (supervisor), also gives the status of the communication network.

Depending on the status of the network CM arranges the managing conditions for each DM. And it is the most beauty that a portion of the communication network can be configured, which proposed in the basic platform of security managements studied in the survey of literature. Hence, with respect to this, it is an efficient & a low power technique if we combine DR manager (administrator) for reconfigurable NoC (RNoC) development. Moreover, effective and low budget maintaining of RNoC, is still exist as an unsolved issue.

IV. DR FRAMEWORK

The Network on Chip framework consists of many elements such as data-links, router and NIU/NI which defines the communication network structure (architecture). During the running process of a system, if one wishes to add or subtract hardware elements of RNoC's structure and modifying parameters for CN, require, a "dynamically communicating framework", which gives the benefit of adoption of topology, concurrent buffering capacity, and dynamically connecting frame width expansion.

(A) Existing Methods Presently

The circuit switching was an earlier used technique, which reconfigurates the network topology according to the adopted NoC architecture. In this method the elements can have a direct connection over a communication link via multiplexers. Hence, the wishing elements can communicate easily. Some other methods studied have, a separate and individually located switches to the DR when the elements were added or removed (like a telephone exchange office). The outcome or usage of these methods are directly depends on the parameters of the defined hardware. Hence, to achieve this at network topology level, a reconfigurable FPGA is required and can be configured dynamically at LB (logic block) level.

(B) Scope for Research

The process of reconfiguration of NoC at runtime yields, the ability of dynamic communication in accordance with the new feeds (updates). The solution available till, is using an individual switching (according to location), which require to adopt a reconfigurable Programmable Devices (PDs) for both addition and deletion of hardware[17-19]. But it complicates the implementation on the other end. Some methods like, live circuit-switching combined with packet-switching make the task easier and pliable for topology configurations. Hence, more research has to be done in maintaining the switch at low power and reduce the area consumption on silicon. And further it is required to keep in mind that RNoC is the major task to implement on new network topology. Hence, it should be investigated. In accordance with the design of buffer, a wide open platform for researchers in the area like power and area confinement. Many solutions are available to size the buffer according to the scale of the design. But it is time to start researching to size the buffer dynamically as per network parameters.

V. DR PROTOCOLS

The major requirement of the Network on chip is to provide point to point communication amongst DTE of the network with assured QoS. To achieve the best quality the NoC[12, 20-21] should never compromise in designing specific protocols of the network, that define the data transferring method, the specific location and paths, the multiplex schemes, the point to point congestion, and the direction control plans.

(A) Existing Methods Presently

The dynamic reconfiguration of a network on chip implicit a modification in the quality of service needs. With respect to protocol, this modification foists the investigation and counting of a new paths(routing), and latest muxing methods for time-slot dispensation. Many investigations have advised algorithms and dynamic methods for calculating route or slot tables. According to one of the references, the investigator described one special

RNoC model, with step by step procedure of model for handling multiple tasks onto the network on chip, with assured QoS. This method tends to many restrictions. Firstly, it deals with only static tasks, determined at design slot. Pre calculated combinational configurations of NoC are limited to select at runtime secondly. Studies with respect to reference some researchers proposed energetic and swift routing procedure depends on selfrouting procedure for multi-processor architecture with intermix between connections. This procedure consumes only one clock pulse to calculate the least possible path. Excepting its principle of network topology, which is a 'phit' transmission, causes limitations for wide usage, and suits only for applications of turbo-communications. Another study provides a assured Qos based on TDMA method, except limited with its topology of mesh type.

(B) Scope for Research

All these studies conclude that the design of RNoc is, only developed for known and pre-calculated network configurations. This gives us a scope to identify two types of conditions: primarily it deals with changes in mode, in this situation conversation with a defined group of implementations or degree with other generally propose a chance, for occurrence depends on the prediction and beginning stage, to float runtime trail and error for calculating new routes and timeslot allotment. Secondly, this situation is timely changing internally with respect to the natural changes that happened in communications for a particular group of applications. For correct modification of RNoC to unexpected changes and uninterrupted/ guaranteed communication, we should build some procedures that yielding safe and undisturbed modification process to attain low cost resolutions for runtime time and space allocations with a job of routing and timesloting.

Table I
Existing Research Methods for RNOC & Collating Them in Accordance with Dr-management,
Framework and Protocols

Method of research design	*Abstraction*	*DR- Management/ Administrarion*	*DR- Infrastructure/ framework*	*DR- Protocols*
OS-regulatedNoC	In this the OS masters the communication between different DTE. And NoC is under OS control.	OS.	NA.	Dynamic_Injection_ rate_control_and_ routing_adaptation.
Dynamic_Time-Slot_Allocation.	This method works based on TDMA, that provides assured communication and QoS dynamically.	Expanded Iterative_Deepening _Algorithm. (IDA)	NA.	Dynamic_Timeslot_ allocation_and_ routing_adaptation.
Dynamic_Network_ on_Chip.	With the help of a large number of switches, processing elements can be controlled. During runtime, turning off these switches, and reusing them for dynamically inserted hardware elements. Routing can be achieved as an expansion of the XY-algorithm, which having the ability of neighboring barriers.	NA.	Re-Network Topology	Update_the_ routing_protocol.
Configurable_ NoC	During runtime, it globally changes the network topology with respect to position, number and capacity of the presently configured physical hardware elements.	Whole_reign_ Occurance_of_ the_system.	Re-Network Topology	Update_the_ routing_protocol.

contd. table I

Method of research design	Abstraction	DR- Management/ Administrarion	DR- Infrastructure/ framework	DR- Protocols
Virtual_Channel_ Regulator.	Depending on the routing traffic, the centralized_Buffer allots virtual channels and buffer-slots in real time.	Unified_Control_ Logic (UCL).	NA.	Dispensing_ dynamically_a_ variable_of_ VCs_on_demand.
Unaltered QoS during RNoC.	With a guaranteed QoS, many applications can map over NoC, based on partial reconfiguration.	Unified_mapping & configuration_ algorithm.	NA.	Dispensing_ dynamically_a_ variable_of_ VCs_on_demand.-
Re-NoC.	With the help of packet and circuit switching techniques, this construct a new topology on the real programmable architecture, based on NoC architecture of an application.	NA.	Re-Network Topology	Dynamic_ combination_ of_packet_ switching_and_ circuit_switching

VI. DISCUSSIONS AND CONCLUSION

To fulfill our survey over the Recongigurable Network on Chip, an investigation report summarized in the above Table 1. Comparing these techniques depends on the constraints discussed in the above, like, Dynamic Reconfiguration management/administration, framework and protocols. In the study, we understood that many of these techniques doesn't satisfy the three constraints, which we propose in our DR model. But some studies in the reference mentioned might cover these three constraints, which limited in management is following the global controlling case in architecture. Even some approaches were already implemented with complete management/administration of architecture with the help of OS, but still suffering with chip area and high power consumptions. Hence, it is a need, to welcome a new unfolding.

We approached with this writeup, the huge scope of research with Reconfigurable Network on Chip as a platform. In accordance with a simplified model of OSI-layers, we have suggested NoC layer topology/connection based DR model of RNoC. We also suggested a design method based on three discussions: reconfiguration management, reconfiguration of network protocols and reconfiguration of the framestructure. We tried our level best in fulfillment of these and further suggested scopes for research in this field.

REFERENCES

[1]   Arteris. A comparison of network-on-chip and busses. White paper., 2005.

[2]   L. Benini and G. De Micheli. Powering networks on chips. System Synthesis, 2001. Proceedings. The 14th International Symposium on, pages 33–38, 2001.

[3]   T. Bjerregaard and S. Mahadevan. A survey of research and practices of network-on-chip. ACM Computing Surveys, 38, 2006.

[4]   C. Bobda, A. Ahmadinia, M. Majer, J. Teich, S. Fekete, and J. van der Veen. Dynoc: A dynamic infrastructure for communication in dynamically reconfugurable devices. Int. Conf. on Field Programmable Logic and Applications, Aug. 2005.

[5]   L. Braun, M. Hubner, J. Becker, T. Perschke, V. Schatz, and S. Bach. Circuit switched run-time adaptive network-on-chip for image processing applications. Field Programmable Logicand Applications, 2007. FPL 2007. International Conference on, pages 688–691, Aug. 2007.

[6]   C. Francalanci and P. Giacomazzi. High-performance self-routing algorithm for multiprocessor systems with shuffle interconnections. Parallel and Distributed Systems, IEEE Transactions on, 17(1):38–50, Jan. 2006.

[7]   J-Ph.Diguet, S.Evain, R.Vaslin, G.Gogniat, and E.Juin. Noccentric security of reconfigurable soc. In 1st ACM/IEEE Int. Symp. on Networks-on-Chips, Princeton, USA, may 2007.

[8]   J. Kramer and J. Magee. Dynamic configuration for distributed systems. IEEE Transactions on Software Engineering, 11(4):424–436, April 1985.

[9]   Jeff Kramer and Jeff Magee. The evolving philosophers problem: Dynamic change management. IEEE Trans. Softw. Eng., 16(11):1293–1306, 1990.

[10] T. Marescaux, B. Bricke, P. Debacker, V. Nollet, and H. Corporaal. Dynamic time-slot allocation for qos enabled networks on chip. Embedded Systems for Real-Time Multimedia, 2005. 3rd Workshop on, pages 47–52, Sept. 2005.

[11] H. Moussa, A. Baghdadi, and M. Jezequel. Binary de bruijn on-chip network for a flexible multiprocessor ldpc decoder. Design Automation Conference, 2008. DAC 2008. 45th ACM/IEEE, pages 429–434, June 2008.

[12] V. Nollet, T. Marescaux, P. Avasare, D. Verkest, and J.-Y. Mignolet. Centralized run-time resource management in a network-onchip containing reconfigurable hardware tiles. Design, Automation and Test in Europe, 2005. Proceedings, pages 234–239 Vol. 1, March 2005.

[13] Vincent Nollet, Th´eodore Marescaux, Diederik Verkest, Jean- Yves Mignolet, and Serge Vernalde. Operating-system controlled network on chip. In DAC '04: Proceedings of the 41st annual conference on Design automation, pages 256–259, New York, NY, USA, 2004. ACM.

[14] Thilo Pionteck, Roman Koch, and Carsten Albrecht. Applying partial reconfiguration to networks-on-chips. In FPL, pages 1–6, 2006.

[15] A. Radulescu, J. Dielissen, K. Goossens, E. Rijpkema, and Paul Wielage. An efficient on-chip ni offering guaranteed services, shared-memory abstraction, and flexible network configuration. In IEEE TCAD, 2004.

[16] S.Evain and J-Ph.Diguet. Efficient space-time noc path allocation based on mutual exclusion and pre-reservation. In 17th ACM Great Lakes Symposium on VLSI (GLSVLSI), Italy, mar 2007.

[17] M.B. Stensgaard and J. Sparso. Renoc: A network-on-chip architecture with reconfigurable topology. Networks-on-Chip, 2008. NoCS 2008. Second ACM/IEEE International Symposium on, pages 55–64, April 2008.

[18] R.Dafali, J-Ph.Diguet, M.Sevaux, "Key Research Issues for Reconfigurable Network-on-Chip" 2008 International Conference on Reconfigurable Computing and FPGAs, IEEE/ DOI 10.1109/ReConFig.2008.72

[19] P. Dong, W. Qian, H. Liang, R. Shafiiha, N.-N. Feng, D. Feng, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Low power and compact reconfigurable multiplexing devices based on silicon microring resonators," Opt. Express, vol. 18, pp. 9852–9858, 2010.

[20] N. Ophir, N. D. Mountain, C. Mineo, and K. Bergman, "Silicon photonic microring links for high-bandwidthdensity, low-power chip I/O," IEEE Micro,s vol. 33, pp. 54– 67, 2013.

[21] X. Xiao, H. Xu, X. Li, Z. Li, Y. Yu, and J. Yu, "High-speed on-chip photonic link based on ultralow-power microring modulator," in Optical Fiber Communication Conf., 2014, paper Tu2E.6.