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Implementation of Network Fault Tolerant VSC HVDC Transmission System by Using Fuzzy Logic Controller

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Abstract: The present converter technology, DC fault current comprises the ac networks contribution through converter free-wheeling diodes and discharge currents of the dc side capacitors. Hence in this paper proposes a new breed of network fault tolerant high-voltage dc (HVDC) transmission systems based on a hybrid multilevel voltage source converter (VSC) with ac-side cascaded H-bridge cells. The proposed HVDC system offers a unique feature of dc fault blocking capability(ability to block power exchange between the ac and dc sides during the dc side faults, hence no current flows in converter switches), operational flexibility in terms of active and reactive power control, black start capability, in addition to improve ac fault ride through capability. In this project assesses its dynamic performance during steady-state and network alternations, including its response to AC and DC side faults. In this proposed system PI controller is replaced with a fuzzy logic controller.

1. INTRODUCTION

The continuous growth of electricity demand and ever increasing society awareness of climate change issues directly affect the development of the electricity grid infrastructure. The utility industry faces continuous pressure to transform the way the electricity grid is managed and operated. On one hand, the diversity of supply aims to increase the energy mix and accommodate more and various sustainable energy sources. On the other hand, there is a clear need to improve the efficiency, reliability, energy security, and quality of supply. With the breadth of benefits that the smart grid can deliver, the improvements in technology capabilities, and the reduction in technology cost, investing in smart grid technologies has become a serious focus for utilities. Advanced technologies, such as flexible alternating current transmission system (FACTS) and voltage-source converter (VSC)-based high-voltage dc (HVDC) power transmission systems, are essential for the restructuring of the power systems into more automated, electronically controlled smart grid.

A VSC-HVDC transmission system is a candidate to meet these challenges due to its operational flexibility, such as provision of voltage support to ac networks, its ability to operate independent of ac network strength therefore makes it suitable for connection of weak ac networks such as offshore wind farms, suitability for multi terminal HVDC network realization as active power reversal is achieved without dc link voltage polarity change, and resiliency to ac side faults (no risk of commutation failure as with line-commutating HVDC systems).

In the last decade, voltage-source-converter high-voltage dc (VSC-HVDC) transmission systems have evolved from simple two-level converters to neutral-point clamped converters and then to true multilevel converters such as modular converters. This evolution aimed to lower semiconductor losses and increase

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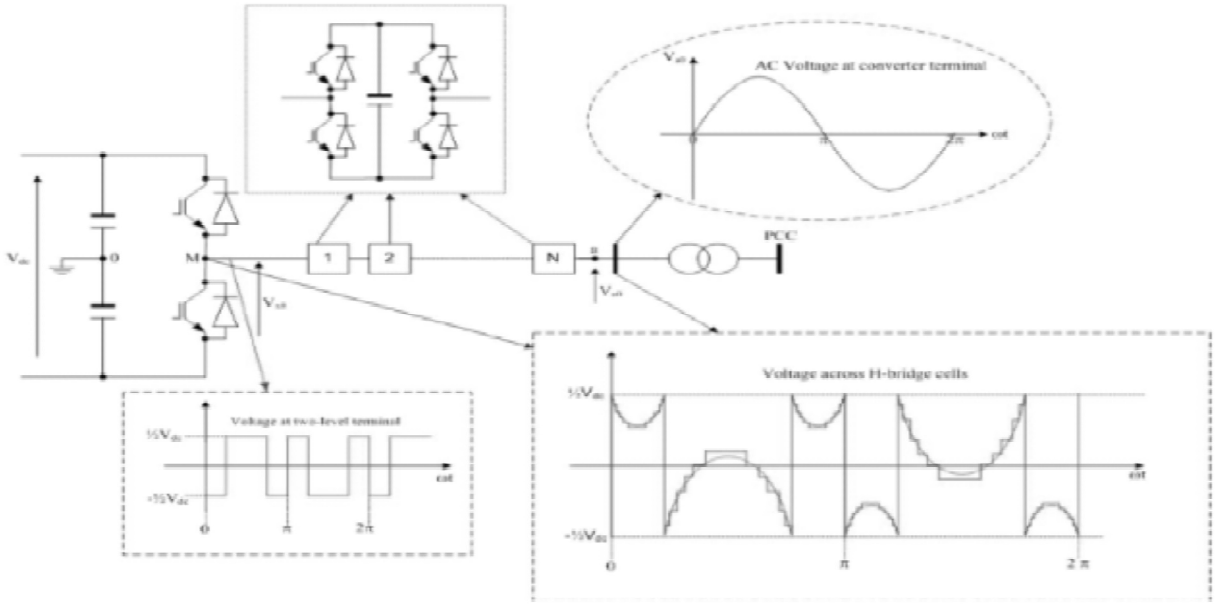


Figure 1: Hybrid voltage multilevel converter with ac side cascaded H-bridge cells.

power-handling capability of VSC-HVDC transmission systems to the level comparable to that of conventional HVDC systems based on thyristor current-source converters, improved ac side waveform quality in order to minimize or eliminate ac filters, reduced voltage stresses on converter transformers, and reduced converter overall cost and footprint.

This project presents a new HVDC transmission systems based on a hybrid voltage-source multilevel converter with ac side cascaded H-bridge cells. The adopted converter has inherent dc fault reverse blocking capability, which can be exploited to improve VSC-HVDC resiliency to dc side faults. With coordination between the HVDC converter station control functions, the dc fault reverse-blocking capability of the hybrid converter is exploited to achieve the following:

- eliminate the ac grid contribution to the dc fault, hence minimizing the risk of converter failure due to uncontrolled over current during dc faults;
- facilitate controlled recovery without interruption of the VSC-HVDC system from dc-side faults without the need for opening ac-side circuit breakers;
- simplify dc circuit breaker design due to are duration in the magnitude and duration of the dc fault current; and, improve voltage stability of the ac networks as converter reactive power consumption is reduced during dc-side faults.

2. A NEW HVDC TRANSMISSION SYSTEMS BASED ON A HYBRID-VOLTAGE-SOURCE CONVERTER WITH AC-SIDE CASCADED H-BRIDGE CELLS HVDC.

High voltage direct current (HVDC) is used to transmit large amounts of power over long distances or for interconnections between asynchronous grids. When electrical energy is required to be transmitted over very long distances, it is more economical to transmit using direct current instead of alternating current. For a long transmission line, the value of the smaller losses, and reduced construction cost of a DC line, can offset the additional cost of converter stations at each end of the line.

Advantages:

- Ground can be used as returned conductor, Less corona loss and radio interference
- No charging current,No skin and Ferranti effect.

Applications of HVDC:

1. Back-to-back converters are used to connect two AC systems with different frequencies – as in Japan – or two regions where AC is not synchronized – as in the US.
2. HVDC links can stabilize AC system frequencies and voltages, and help with unplanned outages.

3. HYBRID MULTILEVEL VSC WITH AC-SIDE CASCADED H-BRIDGE CELLS

Fig. 1 shows one phase of a hybrid multilevel VSC with H-bridge cells per phase. It can generate voltage levels at converter terminal "a" relative to supply midpoint"0." Therefore, with a large number of cells per phase, the converter presents near pure sinusoidal voltage to the converter transformer as depicted in Fig. 1 The two-level converter that blocks high-voltage controls the fundamental voltage using selective harmonic elimination (SHE) with one notches quarter cycle, as shown in Fig. 1. Therefore, the two-level converter devices operate with 150-Hz switching losses, hence low switching losses and audible noise are expected. The H-bridge cells between "M" and "a" are operated as a series active power filter to attenuate the voltage harmonics produced by the two-level converter bridge. These H-bridge cells are controlled using level-shifted carrier-based multilevel pulse width modulation with a 1-kHz switching frequency. To minimize the conversion losses in the H-bridge cells, the number of cells is reduced such that the voltage across the H-bridge floating capacitors sum to. This may result in a small converter station, because the number of H-bridge cells required per converter with the proposed HVDC system is one quarter of those required for a system based on the modular multilevel converter. With a large number of cells per phase, the voltage waveform generated across the H-bridge cells is as shown in Fig. 1, and an effective switching frequency per device of less than 150 Hz is possible. The dc fault reverse-blocking capability of the proposed HVDC system is achieved by inhibiting the gate signals to the converter switches, therefore no direct path exists between the ac and dc side through free wheel diodes, and cell capacitor voltages will oppose any current flow from one side to another. Consequently, with no current flows, there is no active and reactive power exchange between ac and dc side during dc-side faults. This dc fault aspect means transformer coupled H-bridges cannot be used. The ac grid contribution to dc-side fault current is eliminated, reducing the risk of converter failure due to increased current stresses in the switching devices during dc-side faults. From the grid stand point, the dc fault reverse-blocking capability of the proposed HVDC system may improve ac network voltage stability, as the reactive power demand at converter stations during dc-side faults is significantly reduced. The ac networks see the nodes where the converter stations are connected as open circuit nodes during the entire dc fault period. However, operation of the hybrid multilevel VSC requires a voltage-balancing scheme that ensures that the voltages across the H-bridge cells are maintained at under all operating conditions, where is the total dc link voltage. The H-bridge cells voltage balancing scheme is realized by rotating the H-bridge cell capacitors, taking into account the voltage magnitude of each cell capacitor and phase current polarity.

4. CONTROL SYSTEMS

A HVDC transmission system based on a hybrid multi level VSC with ac-side cascaded H-bridge cells requires three control system layers. The inner control layer represents the modulator and capacitor voltage-balancing mechanism that generates the gating signals for the converter switches and maintains voltage balance of the H-bridge cell capacitors. The intermediate control layer represents the current controller that regulates the active and reactive current components over the full operating range and restraints converter station current injection into ac network during network disturbances such as ac and dc side faults. The outer control layer is the dc voltage (or active power) and ac voltage (or reactive power) controller that provide set points to the current controllers.

The inner controller has only been discussed to a level appropriate to power systems engineers. The intermediate and outer control layers are presented in detail to give the reader a sense of HVDC control system complexity.

The current, power, and dc link voltage controller gains are selected using root locus analysis, based on the applicable transfer functions. Some of the controller gains obtained using root locus analysis give good performance in steady state but failed to provide acceptable network disturbance performance. Therefore, the simulation final gains used are adjusted in the time domain to provide satisfactory performance over a wide operating range, including ac and dc side faults. Fig. 2 summarizes the control layers of the hybrid multilevel VSC.

Current Controller Design: The differential equations describing the ac-side transient and steady-state are

$$\frac{di_d}{dt} = -\frac{R}{L}\bar{L}_d + \frac{1}{L}\left(V_{cd} - V_d + \omega L i_q\right) \tag{1}$$

$$\frac{di_q}{dt} = -\frac{R}{L} i_q + \frac{1}{L}\left(V_{cq} - V_q - \omega L i_d\right) \tag{2}$$

Assume

$$\lambda_d = V_{cd} - V_d + \omega L i_q \text{ and } \lambda_q = V_{cq} - V_q - \omega L i_d$$

$$\frac{di_d}{dt} = -\frac{R}{L} i_d + \frac{1}{L}\lambda_d \tag{3}$$

$$\frac{di_q}{dt} = -\frac{R}{L} i_q + \frac{1}{L}\lambda_q \tag{4}$$

The new control variables and can be obtained from two proportion-integral controllers (PI) having the same gains:

$$\lambda_d = K_p(i_d^* - i_d) + K_i \int (i_d^* - i_d)dt \tag{5}$$

$$\lambda_q = K_p(i_q^* - i_q) + K_i \int (i_q^* - i_q)dt \tag{6}$$

Where i_d^* and i_q^* represent reference direct and quadrature current components.

To facilitate control design in state space, the integral parts of λ_d and λ_q are replaced by $W_d = K_i \int (i_d^* - i_d)dt$ and $W_q = K_i \int (i_q^* - i_q)dt$, rearranged in the following form:

$$\lambda_d = K_p(i_d^* - i_d) + W_d \tag{7}$$

$$\lambda_q = K_p(i_q^* - i_q) + W_q \tag{8}$$

The integral parts, in differential equations form, are

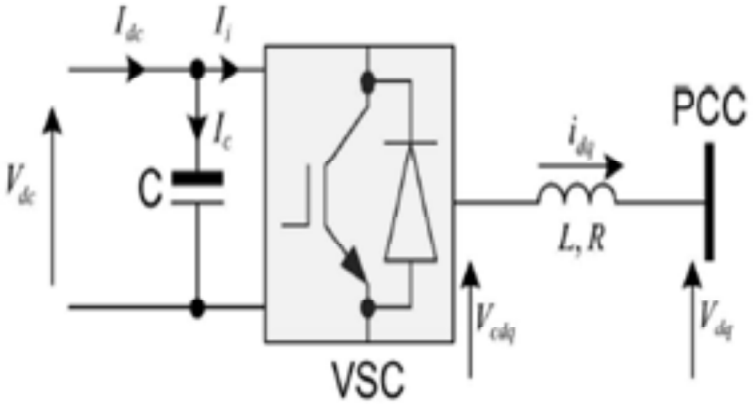
$$\frac{dw_d}{dt} = -K_i \bar{i}_d + K_i i_d^* \tag{9}$$

$$\frac{dw_q}{dt} = -K_i i_q + K_i i_q^* \tag{10}$$

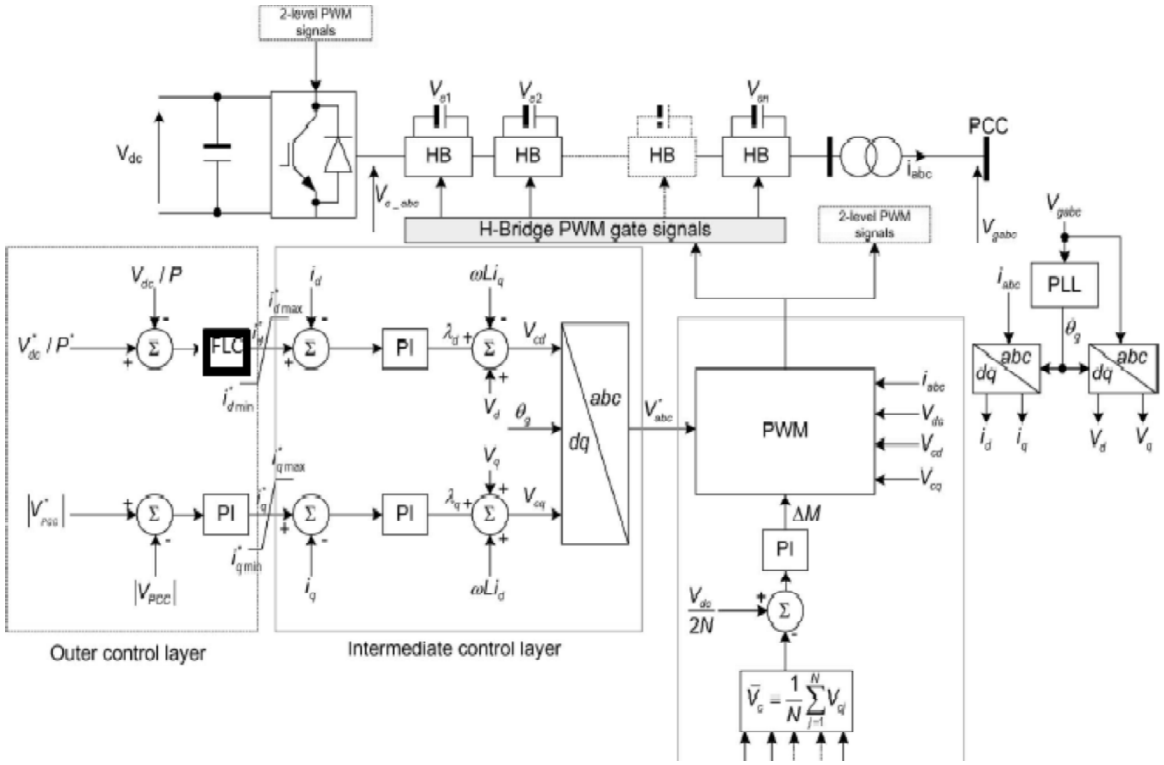
After substitution of (7) and (8) into (3) and (4), two identical and independent sets of equations, suitable for control design, are obtained as

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{dW_d}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R+K_p)}{L} & \frac{1}{L} \\ -K_i & 0 \end{bmatrix} \begin{bmatrix} i_d \\ w_d \end{bmatrix} + \begin{bmatrix} \frac{K_p}{L} \\ K_i \end{bmatrix} i_d^* \tag{11}$$

$$\begin{bmatrix} \frac{di_q}{dt} \\ \frac{dW_q}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R+K_p)}{L} & \frac{1}{L} \\ -K_i & 0 \end{bmatrix} \begin{bmatrix} i_q \\ w_q \end{bmatrix} + \begin{bmatrix} \frac{K_p}{L} \\ K_i \end{bmatrix} i_q^* \tag{12}$$



(a)



(b)

Figure 2: (a) Representation of VSC station and (b) schematic diagram summarizing the control layer of the hybrid multilevel converter with ac side cascaded H-bridge cells

After Laplace manipulations of the state-space equations in (11) and (12), one transfer function is obtained for i_d and i_q, which is used for the current controller design

$$\frac{i_{d(s)}}{i^*_{d(s)}} = \frac{i_q(s)}{i^*_{q(s)}} = \frac{\frac{K_p}{L}s + \frac{K_i}{L}}{s^2 + \frac{(R+K_p)}{L}s + \frac{K_i}{L}}$$

Equations relating the reference voltages to the modulator v^*_{cd} and v^*_{cq}, current controller output λ_d, and λ_q feed forward terms can be obtained from expressions for and as follows:

$$v^*_{cd} = \lambda_d + V_d - \omega L i_q \tag{13}$$

$$v^*_{cq} = \lambda_q + V_q - \omega L i_d \tag{14}$$

Based on (5), (6), (13), and (14), the structure of the current controller shown in Fig. 2(b) (intermediate layer) is obtained. *DC Voltage Controller:* Based on Fig. 2, the differential equation describing the converter dc-side dynamics is

$$C\frac{dv_{dc}}{dt} = I_{dc} - I_i \tag{15}$$

Assuming a lossless VSC, dc power at the converter dc link must equal the ac power at converter terminal. $I_i = (V_{cd}i_d + V_{cq}i_q)/V_{dc}$. Therefore, (15) can be written as

$$C\frac{dv_{dc}}{dt} = I_{dc} - \frac{(V_{cd}i_d + V_{cq}i_q}{V_{dc}} \tag{16}$$

Equation (16) can be linearized using a Taylor series with the higher order terms neglected. Therefore, the linearized form of (16) is

$$\frac{d\Delta V_{dc}}{C} = \frac{\Delta I_{dc}}{C} - \frac{V_{cd}}{CV_{dc}}\Delta i_d - \frac{V_{cq}}{CV_{dc}}\Delta i_q - \frac{i_d}{CV_{dc}}\Delta V_{cd} - \frac{i_q}{CV_{dc}}\Delta V_{cq} + \frac{(V_{cd}i_d + V_{cq}i_q)}{CV^2_{dc}}\Delta V_{dc} \tag{17}$$

Let

$P_{ac} = V_{cd}i_d + V_{cq}i_q$

And

$$\Delta u_{dc} = \Delta J_{dc} - \left(V_{cd}/V_{dc}\right)\Delta i_d - \left(V_{cq}/V_{dc}\right)\Delta i_q - \left(i_d/V_{dc}\right)\Delta V_{cd} - \left(i_q/V_{dc}\right)\Delta V_{cq}$$

and the variable Δu_{dc} can be obtained from the DC voltage controller based on the PI control as follows:

$$\Delta u_{dc} = k_{pdc}(\Delta V^*_{dc} - \Delta V_{dc}) + k_{idc}\int\left(\Delta V^*_{dc} - \Delta V_{dc}\right)dt \tag{18}$$

Equation (17) can be reduced to

$$\frac{d\Delta V_{dc}}{dt} - \frac{\Delta u_{dc}}{C} + \frac{P_{uc}}{CV^2 dc}\Delta V_{dc} \tag{19}$$

Where V_{dc}^{*} represents reference dc link voltage.

Let the new control variable introduced for the integral part of the dc voltage controller be z_{dc}, therefore:

$$\frac{d\Delta V_{dc}}{dt} = -\frac{1}{C}\left(K_{pdc} - \frac{P_{ac}}{V_{dc}^2}\right)\Delta V_{dc} + \frac{1}{C} + \Delta Z_{dc} + \frac{\Delta V_{dc}^2}{C} \tag{20}$$

$$\frac{d\Delta Z_{dc}}{dt} = K_{idc}(\Delta V_{dc}^{*} - \Delta V_{dc})\,. \tag{21}$$

The state equations in (20) and (21) in matrix form are:

$$\frac{d}{dt}\begin{bmatrix}\Delta V_{dc}\\ \Delta Z_{dc}\end{bmatrix} = \begin{bmatrix} -\left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV^2 dc}\right)\frac{1}{c} \\ 0 \\ -K_{\bar{i}dc}\end{bmatrix}\begin{bmatrix}\Delta V_{dc}\\ \Delta Z_{dc}\end{bmatrix} + \begin{bmatrix}\frac{K_{p\,dc}}{C}\\ K_{idc}\end{bmatrix}\Delta V_{dG}^{*} \tag{22}$$

Equation (22) in the s-domain is $\begin{bmatrix}\Delta V_{dc}(S)\\ \Delta Z_{dc}(S)\end{bmatrix}$

$$\frac{1}{T}\begin{bmatrix} S & \frac{1}{C} \\ -K_{idc} & S + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV^2 dc}\right)\end{bmatrix}\begin{bmatrix}\frac{K_{pdc}}{C}\\ K_{idc}\end{bmatrix}\Delta V_{dc}^{*} \tag{23}$$

Where

$$T = S^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV^2 dc}\right)s + \frac{K_{idc}}{C}$$

$$\begin{bmatrix}\Delta V_{dc}(S)\\ \Delta Z_{dc}(S)\end{bmatrix} = \begin{bmatrix} \dfrac{\frac{K_{pdc}}{C}S + \frac{K_{dc}}{C}}{S^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV^2 dc}\right)s + \frac{K_{idc}}{C}} \\ \dfrac{k_{\bar{i}dc}\left(s - \frac{P_{ac}}{CV^2{}_{dc}}\right)}{s^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV^2 dc}\right)s + \frac{K_{idc}}{C}}\end{bmatrix}\Delta V_{dc}^{*} \tag{24}$$

From (24), the transfer function for the dc voltage controller is

$$\frac{V_{dc}(s)}{V_{dc}^{*}(s)} = \frac{\frac{k_{pdc}}{C}S + \frac{k_{idc}}{C}}{S^2 + \left(\frac{K_{pdc}}{C} - \frac{P_{ac}}{CV^2 dc}\right)s + \frac{K_{idc}}{C}} \tag{25}$$

Normally, the voltage angle at the converter terminal relative to the PCC is sufficiently small, resulting in $V_{cq} \approx 0$ and $\Delta V_{cq} \approx 0$. Therefore, the reference current for the current controller can be obtained from the outer dc voltage controller as follows:

$$\Delta i_d^{*} = -\frac{1}{V_{cd}}\left(\Delta u_{dc} + i_d \Delta \tilde{V}_{cd} - \Delta I_{dc}\right) \tag{26}$$

Where $\overline{v}_{cd}$ and $\overline{v}_{cq}$ are normalized by V_{dc}^{*}.

Active Power *Controller:* The active power controller sets the reference active current component assuming a constant voltage at the PCC as follows:

$$i_d^{*} = K_{pp}(P^{*} - V_d^{*} i_d) + K_{ip}\int\left(P^{*} - V_d^{*} i_d\right)dt \tag{27}$$

Assume the voltage vector at the PCC is aligned with the -axis and its magnitude is regulated at V_d^{*} as $V_q^{*} = 0$, and *P** represents active power reference. After replacing the integral part with a new control variable, the following sets of equations result:

$$i_d^{*} = K_{pp}(P^{*} - V_d^{*} i_d) + Z_p \tag{28}$$

$$\frac{dz_p}{dt} = K_{ip}(P^{*} - V_d^{*} i_d) \tag{29}$$

After substituting (28) into (11), the following state space representation for the power controller is obtained:

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{dz_d}{dt} \\ \frac{dz_d}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(R + K_p + K_p K_{pp} v_d^{*}}{L} & \frac{1}{L} & \frac{Kp}{L} \\ -\left(K_i + K_i K_{pp} V_d^{*}\right) & 0 & K_i \end{bmatrix} \begin{bmatrix} i_d \\ Z_d \\ Z_p \end{bmatrix} + \begin{bmatrix} \frac{K_P K_{PP}}{L} \\ K_i K_{pp} \\ K_{ip} \end{bmatrix} P^{*}$$

where we have (30), shown at the bottom of the page.

AC Voltage Controller: The reference reactive power current component is set by the ac voltage controller as

$$i_q^{*} = K_{pv}\left(\left|V_{ac}^{*}\right| - \left|V_{ac}\right|\right) + K_{iv}\int\left(\left|V_{ac}^{*}\right| - \left|V_{ac}\right|\right)dt$$

Where $\left|V_{ac}^{*}\right|$ represents reference voltage magnitude at PCC. However, the gains for the ac voltage controllers are obtained using a trial 0 and-error search method that automatically runs the overall system simulation several

times in an attempt to find the gains that produce the best time domain performance. The gains for all of the controllers and test network parameters used in this paper are listed in Tables I–III.

$$\frac{P(s)}{p^*(s)} = V^* d^* \frac{i_d(s)}{p^*(s)} = V^* d^*$$

$$\frac{\left(KpKpp + Kp + K\bar{i}p\right)}{L} S + \frac{K_L}{L} S^3 + \frac{(R + Kp + KpKppV * d)}{L} S^2 + \frac{\left(K_{i4} k_s k_{pp} V^* d^* k_p k_{ip} V^* d\right)}{L} s + \frac{K_s K_{ip} V_d^*}{L} \quad (30)$$

4.1. Fuzzy Logic Controller

The Fuzzy logic control consists of set of linguistic variables. The mathematical modelling is not required in FLC. FLC consists of

1. Fuzzification: Membership function values are assigned to linguistic variables. In this the scaling factor is between 1 and -1.
2. Inference Method: There are several composition methods such as Max-Min and Max-Dot have been proposed and Min method is used.
3. Defuzzificaion: A plant requires non fuzzy values to control, so defuzzification is used. The output of FLC controls the switch in the inverter. To control these parameters they are sensed and compared with the reference values. To obtain this the membership functions of fuzzy controller are shown in fig (10).

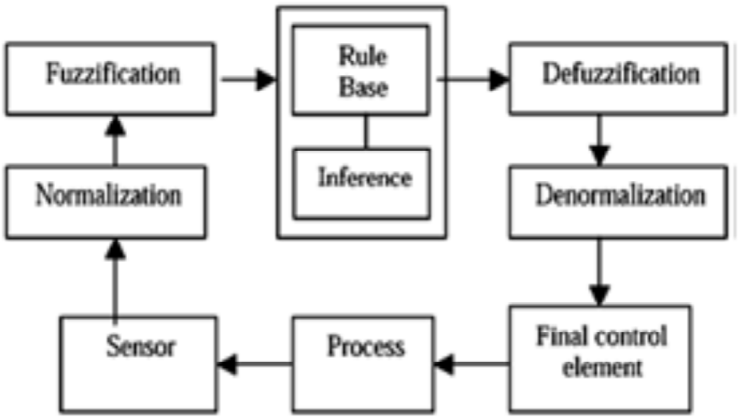


Figure 2.c: Fuzzy logic Controller

Fuzzy Control Rule:

e / de	NL	NM	NS	ZE	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	ZE
NM	NL	NM	NM	NM	NS	Z	PS
NS	NL	NM	NS	NS	ZE	PS	PM
ZE	NL	NM	NS	ZE	PS	PM	PL
PS	NM	NS	ZE	PS	PS	PM	PL
PM	NS	ZE	PS	PM	PM	PM	PL
PL	ZE	PS	PM	PL	PL	PL	PL
PL	ZE	PS	PM	PL	PL	PL	PL

In fuzzy Logic Toolbox software, fuzzy logic should be interpreted as FL, that is, fuzzy logic in its wide sense. The basic ideas underlying FL are explained very clearly and insightfully in Foundations of Fuzzy Logic. What might be added is that the basic concept underlying FL is that of a linguistic variable, that is, a variable whose values are words rather than numbers.

Another basic concept in FL, which plays a central role in most of its applications, is that of a fuzzy if-then rule or, simply, fuzzy rule. Although rule-based systems have a long history of use in Artificial Intelligence (AI), what is missing in such systems is a mechanism for dealing with fuzzy consequents and fuzzy antecedents. In fuzzy logic, this mechanism is provided by the calculus of fuzzy rules. The calculus of fuzzy rules serves as a basis for what might be called the Fuzzy Dependency and Command Language (FDCL).A trend that is growing in visibility relates to the use of fuzzy logic in combination with neuron computing and genetic algorithms.

The guiding principle of soft computing is: Exploit the tolerance for imprecision, uncertainty, and partial truth to achieve tractability, robustness, and low solution cost. In the future, soft computing could play an increasingly important role in the conception and design of systems whose MIQ (Machine IQ) is much higher than that of systems designed by conventional methods.The fuzzy logic toolbox is highly impressive in all respects. It makes fuzzy logic an effective tool for the conception and design of intelligent systems. The fuzzy logic toolbox is easy to master and convenient to use. And last, but not least important, it provides a reader friendly and up-to-date introduction to methodology of fuzzy logic and its wide ranging applications.

Table 1
Converter Stations Parameters

Converters 1 and 2	
Power ratings	687 MVA
Maximum active power capability	600 MW
Maximum reactive power capability	335 MV Ar
Two-level dc link voltage	600k V
H-bridge de link voltage	42.86k V
Two-level dc link capacitance	150μ F
H-bridge cell capacitance	3mF
H-bridge switching frequency	1kHz
Converter 1 controllers	
Current controller: K_p	35
Current controller: K_i	3000
Power controller: K_{pp}	0.0015
Power controller: K_{ip}	20
AC voltage controller: K_{pv}	30
AC voltage controller: K_{iv}	500
Converter 2 controllers	
Current controller: K_p	38
Current controller: K_i	2000
DC voltage controller: K_{pdc}	0.015
DC voltage controller: K_{idc}	0.0573
AC voltage controller: K_{pv}	0.00015
AC voltage controller: K_{iv}	400

Table 2
Converter Transformer Parameters

Transformers 1 and 2	
Power rating	687MA
Voltage ratio	330kV/400k V
Per unit impedance	(0.0008 + j0.32)

Table 3
Transmission Systems Parameters

Lines parameters (based on humped π model)	
ac line length	60 km
ac line series impedance	(0.0127 + j0.2933)Ω/km
ac line shunt capacitance	12.74nF/km
dc transmission distance	75 km
dc line series resistance	13.9mΩ/km
dc line series inductance	0.159mH/km
dc line shunt capacitance	0.231μF/km

Gains for all of the controllers and test network parameters used in this paper are listed in Tables I–III

5. SIMULATION RESULTS

The viability of the VSC-HVDC system that uses a hybrid multilevel VSC with ac-side cascaded H-bridge cells is investigated here, with emphasis on its dynamic performance during network alterations. In the steady state, the test network in Fig. 3(a) is used to assess its power control and voltage support capabilities. To further illustrate the advantages of multilevel converter during ac and dc network disturbances, the same test network is subjected to a three-phase ac-side fault and a pole-to-pole dc-side fault at locations depicted in Fig. 3(a), both for a 140-ms duration. Converter stations 1 and 2 in Fig. 3(a) are represented by detailed hybrid VSC models with seven cells per phase, with the controllers in Fig. 2(b)incorporated. Seven cells per arm are used in this paper in order to achieve acceptable simulation times without compromising result accuracy, as each system component is represented in detailed. Also, the hybrid converter with seven H-bridge cells per phase generates 29 voltage levels per phase, which is the same as the two-switch modular multilevel converter with 28cells per arm, for the same dc link voltage such that devices in both converters experience the same voltage stresses. The converters are configured to regulate active power exchange and dc link voltage, and ac voltage magnitudes at and respectively. The test system in Fig. 3(a) is simulated in the MATLAB Simulink environment.

5.1. Four-Quadrant Operation And Voltage Support

To demonstrate four0quadrant operation and voltage support capability of the presented VSC-HVDC system, converter station1 is commanded to increase its output power export from grid to from 0 to 0.5 pu (343.5 MW) at 2.5 pu/s. At time 1 s it is commanded to reverse the active power flow in order to import 343.5 MW from grid, at 2.5 pu/s. At a load of is introduced to, illustrating the voltage support capability of converter station 2during network alteration.

Fig. 3(b) and (c) show converters 1 and 2 active and reactive power exchange with and respectively. The converters are able to adjust their reactive power exchange with and in order to support the voltage during the entire operating period. Fig. 3(c) and (d) show that converter2 adjusts its reactive power exchange with when the load is introduced at 2 s to support the voltage magnitude. Fig. 3(e) and (f) show that converter 2 injects and

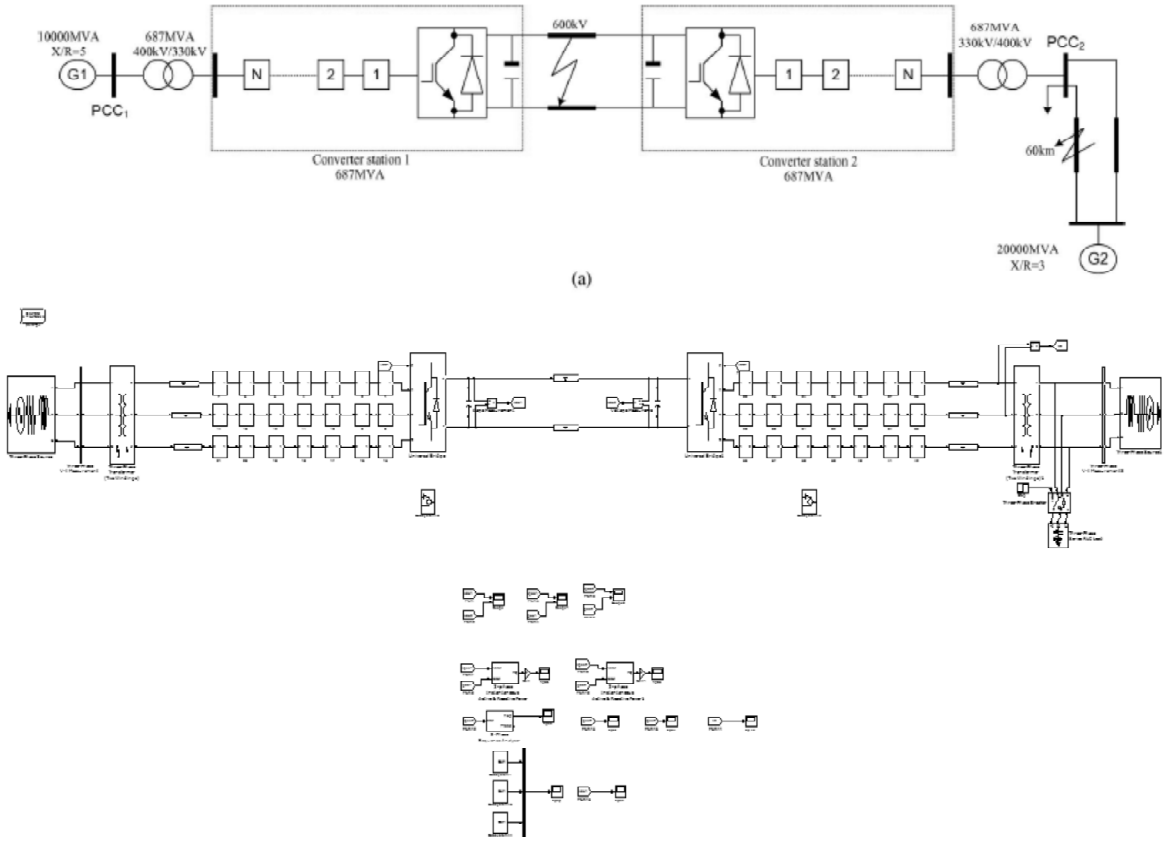
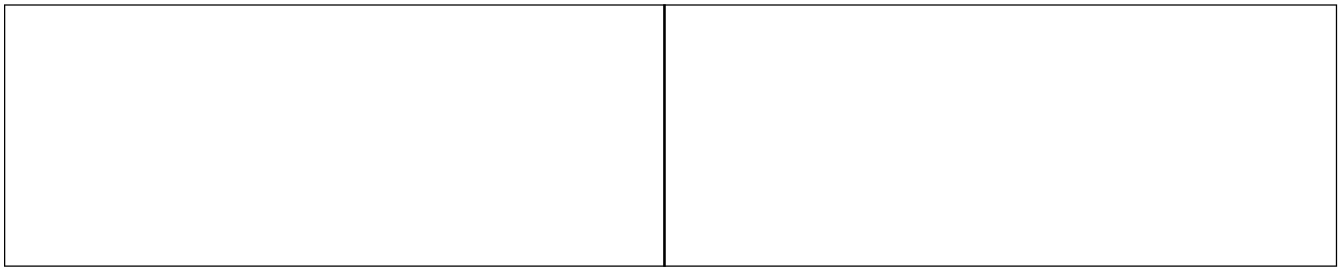


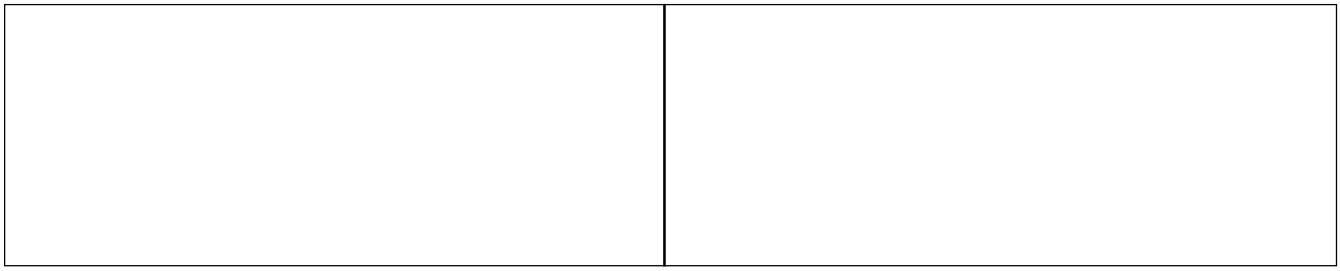
Figure 3: Simulation diagram of test network and of waveforms demonstrating the steady-state operation of HVDC system based on hybrid voltage source multilevel converter with ac sidecascaded H-bridge cells. (a) Test network used to illustrate the viability of the hybrid multilevel voltage source converter HVDC systems; (b) active and reactivepower converter station 1 exchanges with pcc1; (c) active and reactive power converter station 2 exchanges with pcc2 ; (d) voltage magnitude at pcc2;(e) voltage waveforms at pcc2; (f) current waveforms converter station 1 exchanges withpcc1 ; (g) voltage across 21 cell capacitors of the three phases ofconverter 1; (h) voltage across the dc link of converter station 2.

(a) **(b)**

(c) **(d)**



(e) (f)

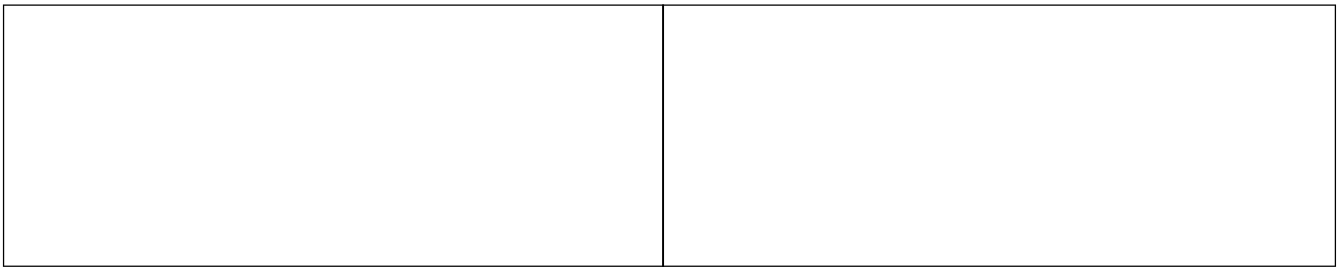


(g) (h)

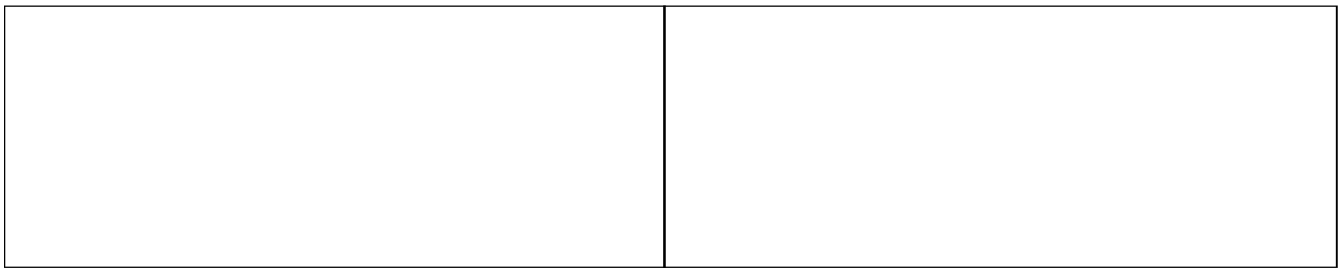
presents high-quality current and voltage waveforms into with no ac filters installed). Fig. 3(g) demonstrates that the voltage stresses across the H-bridge cell capacitors of converter 1 are controlled to the desired set point during the entire period. Fig. 3(h) displays the total dc link voltage across converter 2, which regulates the dc link voltage. Based on these results, the proposed VSC-HVDC system is able to meet basic steady-state requirements, such as provision of voltage support and four quadrant operation without compromising the voltage and current stresses on the converters switches.

5.2. AC Network Faults

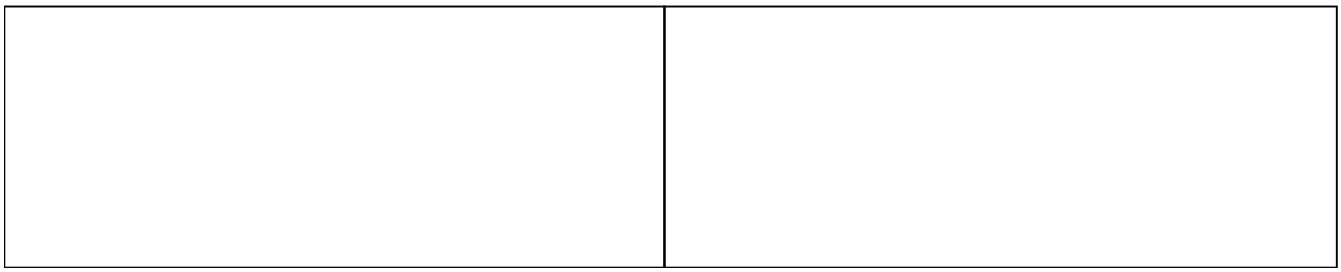
To demonstrate the ac fault ride-through capability of the presented HVDC system, the test network is subjected to a 140 ms three-phase fault to ground at the location shown in Fig. 3(a).During the fault period the power command to converter 1 is reduced in proportion to the reduction in the ac voltage magnitude (this is achieved by sensing voltage). This is to minimize the two-level converter dc link voltage rise because of the trapped energy in the dc side, since power cannot be transferred as the voltage at collapses. Fig. 4 displays the results when the test network exports 0.5 pu (343.5 MW) from grid to and is subjected to the three-phase fault at.Fig. 4(a) shows the active and reactive powers converter 1 exchanges with. Note that converter 1 matches its active power export to in order to minimize the rise of converter2 dc link voltage as its ability to inject active power into grid reduces with the voltage collapse at, as shown in Fig. 4(d) and stated above. Fig. 4(b) shows the active and reactive powers that converter 2 injects into PCC2. The system is able to recover as soon as the fault is cleared, and converter2 adjusts its reactive power exchange with grid2 G2 in order support voltage at PCC2.The transients shown of active and reactive powers at PCC2 are related to the reaction of the ac voltage controller that regulates the ac voltage at PCC2.



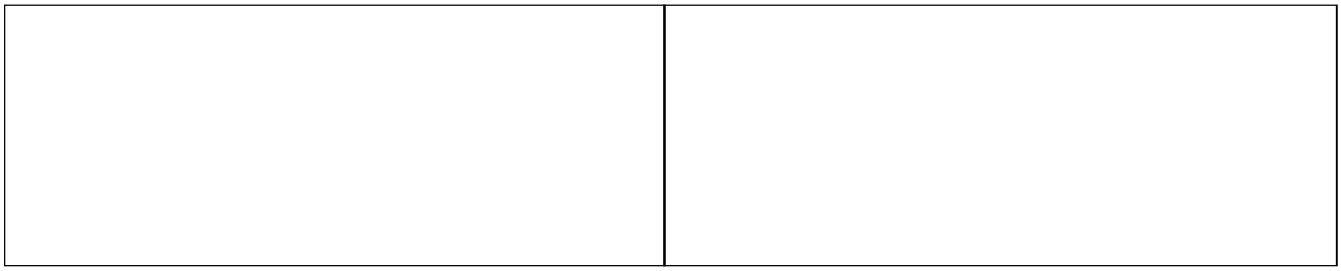
4(a) (b)



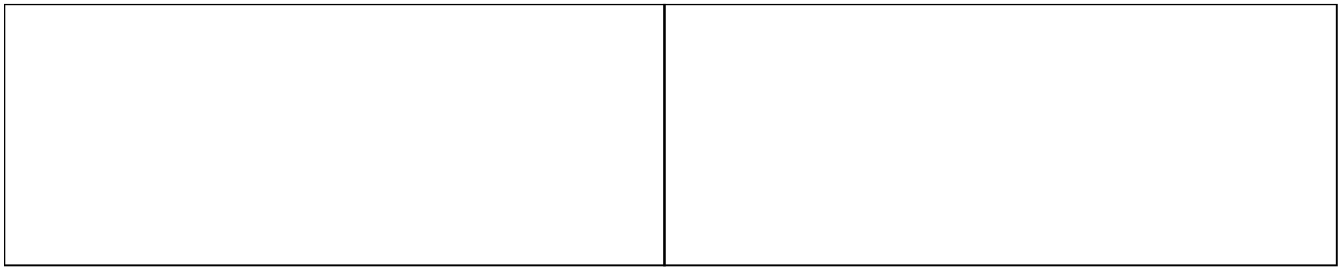
(c) **(d)**



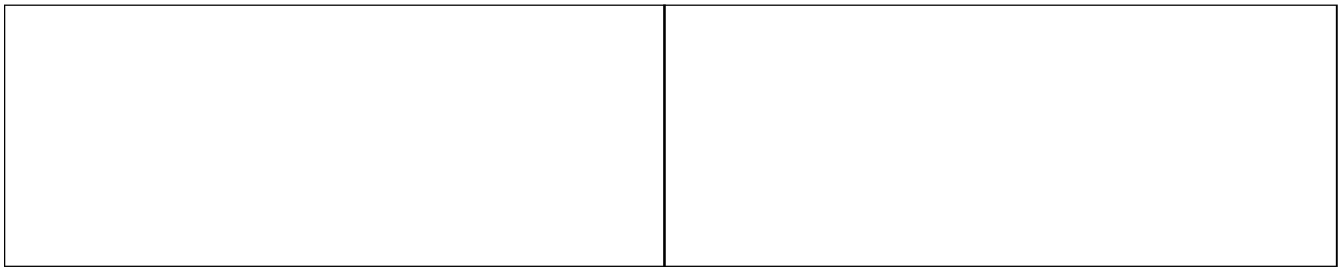
(e) **(f)**



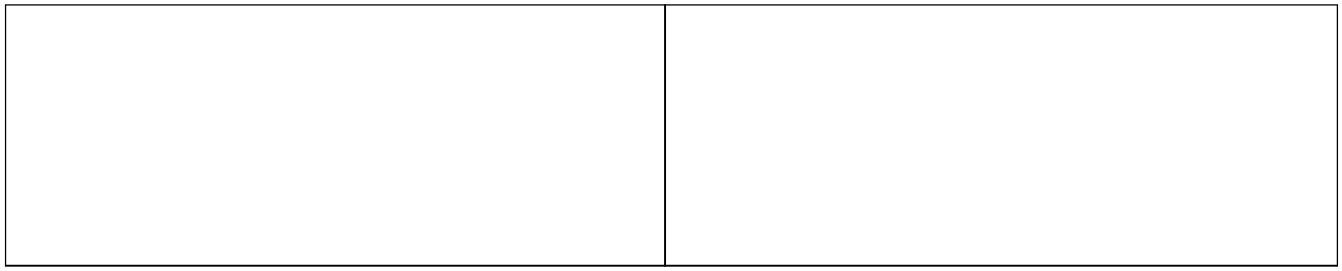
(g) **(h)**



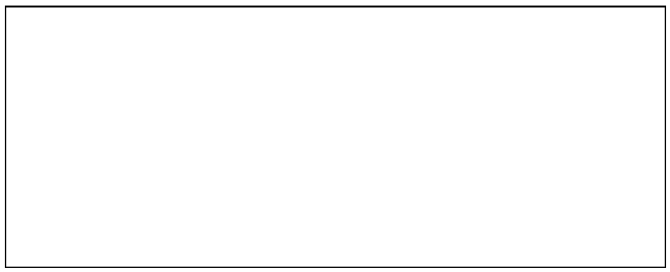
(i) **(j)**



(k) **(l)**



(m) (n)

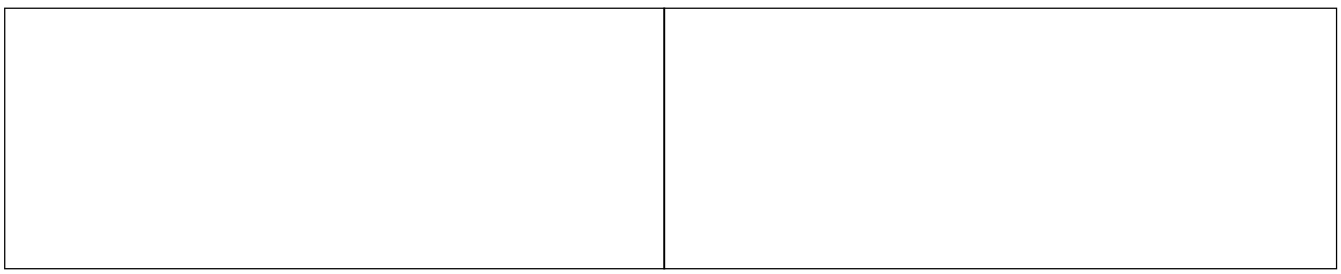


(o)

Fig.4. Waveforms demonstrating ac fault ride-through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells. (a) Active and reactive power converter 1 exchanges with PCC1 (b) Active and reactive power converter 2 injects intoPCC2. (c)Voltage magnitude at PCC1 (d) Voltage magnitude at PCC2. (e) Current waveforms converter 2 injects into PCC2. (f) Converter 2 dc link voltage. (g) Voltage across 21 H-bridge cells of the converter 2.(h) line-to-line voltage waveform at the terminal of converter1.(i) Active and reactive power at PCC1. (j) Active and reactive power at PCC2. Results in (i)–(o) demonstrate the case when the converter stations operate close to their maximum active powercapabilities (power command at converter 1 is set to 0.75 pu, which is 515 MW) and system is subjected to a three-phase fault with a 300-ms duration.

5.3. DC Network Faults

The inherent current-limiting capability of the hybrid multilevel VSC with ac-side cascaded H-bridge cells that permits the VSC-HVDC system to ride-through dc-side faults will be demonstrated here. The test network is subjected to a 140ms solid pole-to-pole dc-side fault at the location indicated in Fig. 3(a). During the dc-side fault period, active power exchange between the two grids and is reduced to zero. This facilitates uninterruptable system recovery from the temporary dc fault with minimal inrush current, since the power paths between the converter's ac and dc sides are blocked (by inhibiting all converter gate signals) to eliminate a grid contribution to the dc fault. Charge from both ac sides; this causes a large current flow from both ac sides to the dc side to charge the dc link capacitors and cable distributed capacitors as shown in Fig. 5(e) and 5(f). The results in Fig. 5(e) and 5(f) also demonstrate the benefits of dc fault reverse blocking capability inherent in this hybrid system, as the converter switches experience high current stresses only during dc link voltage build-up. Fig. 5(g) shows that converter 2 dc link voltage recovers to the pre-fault state after the fault is cleared.



(a) (b)

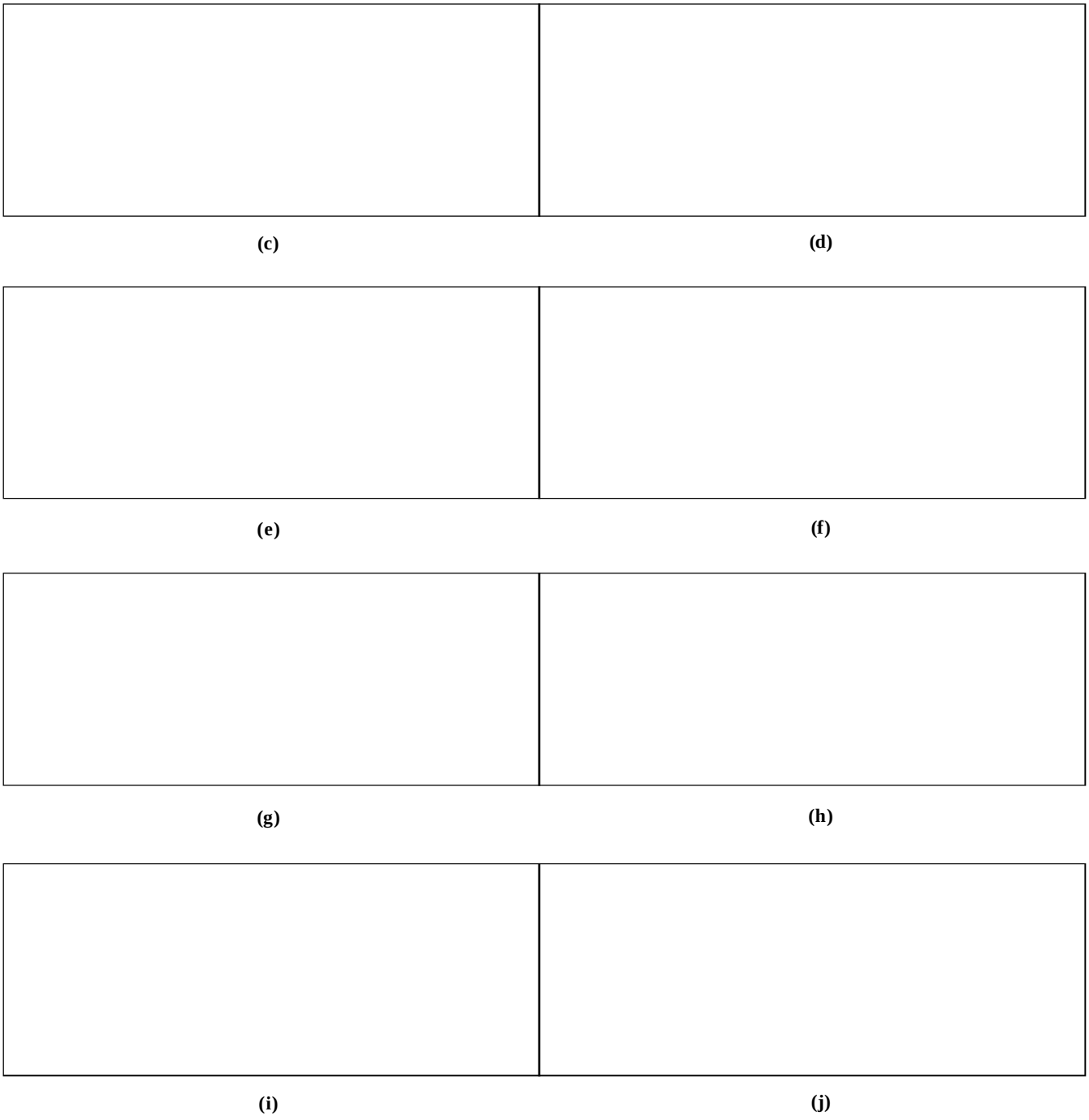


Fig.5. Waveforms demonstrating dc fault ride through capability of HVDC transmission systems based on hybrid voltage multilevel converter with ac side cascaded H-bridge cells. (a) Active and reactive power converter 1 exchanges with PCC1. (b) Active and reactive power converter 2 exchanges with PCC2.(c) Voltage magnitude at PCC1. (d) Voltage magnitude at PCC2.(e) Current waveforms converter 1 exchange with grid G1 at PCC1. (f) Current waveforms converter 2 exchange with grid G2 at PCC2. (g) Converter 2 dc link voltage. (h) Zoomed version of dc link current demonstrating the benefits of dc fault reverse blocking capability. (i) Voltage across the H-bridge cell capacitors of converter 1. (j) Voltage across the H-bridge cell capacitors of converter 2.

6. CONCLUSION

This project presented a new generation VSC-HVDC transmission system based on a hybrid multilevel converter with ac-side cascaded H-bridge cells.The main advantages of the proposed HVDC system are:

- Potential small footprint and lower semiconductor losses compared to present HVDC systems.
- Low filtering requirement on the ac sides and presents high-quality voltage to the converter transformer.
- does not compromise the advantages of VSC-HVDC systems such as four-quadrant Operation; voltage support capability; and black-start capability, which is vital for connection of weak ac networks with no generation and wind farms.
- Modular design and converter fault management (inclusion of redundant cells in each phase may allow the system to operate normally during failure of a few H-bridge cells; whence a cell bypass mechanism is required).

  By using fuzzy controller the voltage sag can be mitigated and it is a high efficiency regulator compares to other controllers.
- Resilient to ac side faults (symmetrical and asymmetrical)

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