I J C T A, 9(13) 2016, pp. 6221-6227

Ultra-Low Power Asynchronous Pipeline Domino Logic Design Based on Quad and Single Rail Domino Gates

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ABSTRACT

The present aims to design method of Ultra low power asynchronous pipeline domino logic focus on achieving the circuit efficiency and it is used for integrated circuits. This logic is to construct a single and quad rail gate to perform synchronizing logic gate with latch and also to analyze the power consumption, delay and threshold voltage. This feature offers reduced overhead delays, occupies less silicon area and very low power consumption. Single-rail logic alone can't be used because it would break the data path as only non-inverting logic can be used. Quad rail gates are limit to building a fixed critical data path. The method discussed in this paper save power consumption by reduce the overhead delays of logic circuits. This approach a localencoding handshaking protocol, with synchronize at each stages between next pipeline stages compare to previous synchronous and asynchronous pipelined design techniques. The evaluation results shows that the proposed pipeline method of quad rail based asynchronouspipelined domino logic, which focuses on reduced delay and less power consumption, better circuit efficiency than a dual rail based asynchronous domino logic.

Keywords: Asynchronous pipeline domino logic, Single rail, Dual rail, Quad rail.

1. INTRODUCTION

Asynchronous pipeline design is considered as a promising solution for dealing with the issues local handshake instead of externally supplied global clock. Handshake circuits generate local clock pulses and use delay matching to indicate valid signal. It leads to the most efficient circuits due to the extensive use of timing assumptions. The four-phase dual-rail protocol design is implemented in a detailed way that the handshake signal is combined with the dual-rail encoding of data.

This project presents a design method of quad rail based asynchronous domino logic pipeline which focuses on improving the circuit efficiency and make in asynchronous domino logic pipeline design more practical for a wide range of applications. This design method combines the advantages of the four-phase quad-rail protocol and the four-phase bundled-data protocolto improve the efficiency of area and power in asynchronous domino logic pipeline.

The latch less design provide less critical delays, small silicon area and lower power consumption. Asynchronous domino logic pipeline has a problem that dual-rail domino logic has to be used to compose the domino data path. Only single-rail domino logic cannot be used as it would break the domino data path, The domino data path has a dual-rail encoding above thelevel of head that consumes a lot of silicon area and high power consumption. The asynchronous pipelines automatically provide flow control. Handshaking protocols inherently offer underflow and overflow protection, even speed environments. Synchronous flow control is typically supported using explicit credit-based techniques involving extra registers or complex

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decoupled latch control. A signal, used for back pressure, must also be synchronized to the clock at every stage.It cause low circuit efficiency and put limit to the application area of four-phase dual-rail protocol design.

2. DOMINO GATES

2.1. Single Rail Domino Gate

The main motive of dynamic logic styles is to use only in n-transistors logic trees, to achieve their high performance and less area. The main problem of directly connecting the two dynamic node is that the pre-charged at high output node will cause theresult in conducting of n-transistors in the logic trees. Single rail domino logic solve this issue with a modified inverter design,It follows an n-transistors are in off condition and there is no flow out. The single rail domino logic style like domino logic pipeline design realize only non-inverted modified design. The inverter outputs are early arrived, that has enough time to switch off all n-transistors in the circuit.

2.1.1. Single Rail Data paths

Therefore several solutions are proposed for gate level pipeline design of wide range single and dual rail data path can be implemented. The proposed approach is used to separating the each pipeline. The Quad rail completion detector are replaced with modified single rail completion detectors and encoding signals. However, there is no data path break in single rail bundled asynchronous data paths, each data stream has its own unique “request” and “acknowledgement” signal. The Joining of multiple data paths requires the explicit mergingof the multiple request and acknowledgement signals at the each stage inputs. This Joiner is to achieving a high speed operation.

However, the event that there are multiple path request signals are required for the pipeline.An efficient way of combining multiple request signals is to add a small number of additional pipeline stages, which recombine the control signal for the modified encoded completion generatorcan produce earlier than the control valid signal that pre-charges and evaluates the each pipeline stage. Asa result, more overhead delay of transmitting the valid control signal to the eachgates in parallel pipeline stages.

2.2. Quad Rail Domino Gate

However, asynchronous domino logic pipeline has a common problem that quad-rail domino logic has to be used to create the domino data path. Single-rail domino logic cannot be used because it would break the domino data path hence only non-inverting logic can be implemented. As a result, the domino data path has a dual-rail encoding overhead that it consumes more silicon area and power consumption. Such overhead almost cancels out the area and power benefits provided by the latch less feature.

Another problem is overhead of handshake control logic. Conventional designs of asynchronous domino logic pipeline is based on four-phase quad-rail protocol rely on domino data path to transfer the data and encoded handshake signal and it is used to detectthe completion detectors and collect the handshake signal throughout the entire data paths.

In proposed design the data paths are composed mixture of Quad-rail and single-rail domino gates. To achieve less area and less power consumption.The critical data paths, composed of Quad-rail logic, transfers a valid data signal and an encoded handshake protocol. Noncritical data paths are composed of quad rail and single rail logic to transfer valid data signal.

2.2.1. QuadRail Data paths

In this proposed system present a Quad rail method for quad rail domino circuit that provides lesser power consumption and reduced delay. The Mixed Swing Quad Rail is a multiple power supply method in each

gate has less multiple power supply voltage.A bundled power-rail method called Mixed Swing Quad rail has been proposed to construct a stable static CMOS in digital logic gates using multiple voltages.A wide range of Quad rail dominodata path may be separated into several data paths.

As in each modified completion detector only examine the valid bits that belongs to its own data path. The output of aneach stage modified completion detectors aretypically less, the less distribution of the valid control signals. In FIFOs have separate data paths do not interact with otherdata paths with logic processing may involve mergingand forkingof data path at certain points in the each pipeline stages, it would cause the complicate pipeline structure.

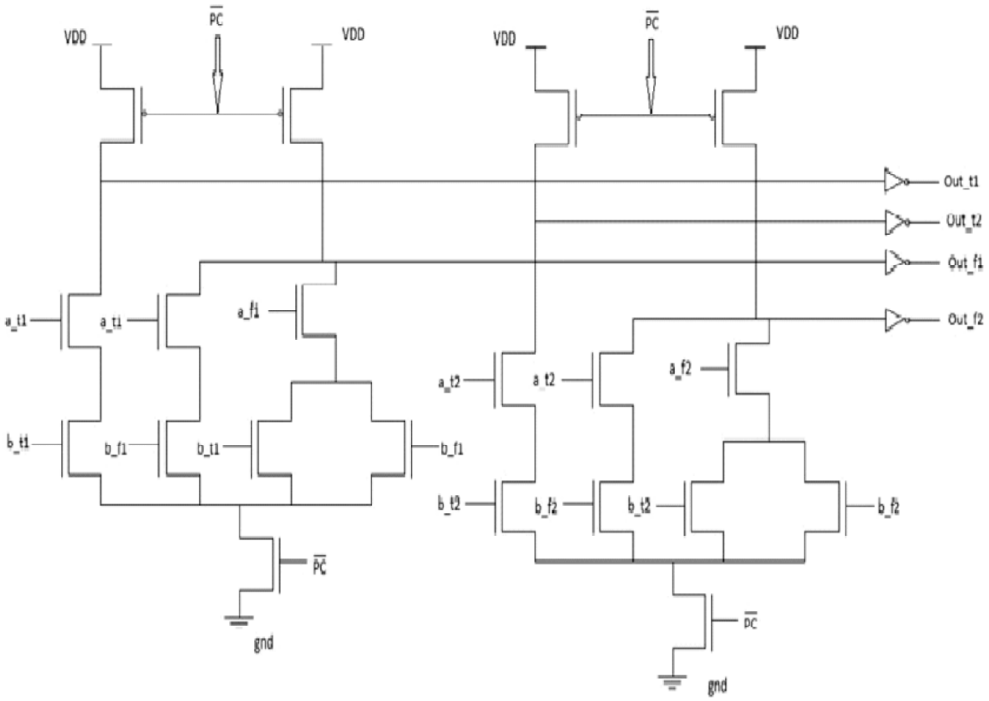

Figure 1: Quad rail domino AND gate

3. ADVANCED PIPELINES

1) Synchronize Logic Gates

SLGs are dual rail domino logicgates that have no gate delay dependence problem.Synchronize logic AND gate. Compared with the modified design, the logical expression is changed to out_ f = (a_t · b_ f + a_ f · b_t + b_ f). In every data path have transistors at the sequential position, and there is no another path required only one path turns ON the input data pattern. As a result, the gate delay may independent of different input data patterns. An SLGL has an enable signal*(*en_*t,* en_ *f)*,which controls the state of transistor in opaque and transparent state of the SLGL. SLGLs cannot start evaluation untilthe presence of the enable signal.Same as all traditional quad rail domino logiccan be re-designed to become an SLG or an SLGL.The critical data path in Quad rail asynchronous pipeline can be easily constructed using SLGs and SLGLs.

2) Delay Assumptions

Proposed design is a very robust pipeline itrequires no delay assumptions or calculations. However, the robustness of circuits comes at the better of its performance. The encoded handshake circuits slow down the handshake speed and consume high power. For high speed handshake is achieved by re-designing of encoder circuit using control circuits that are always correct for common conditions.

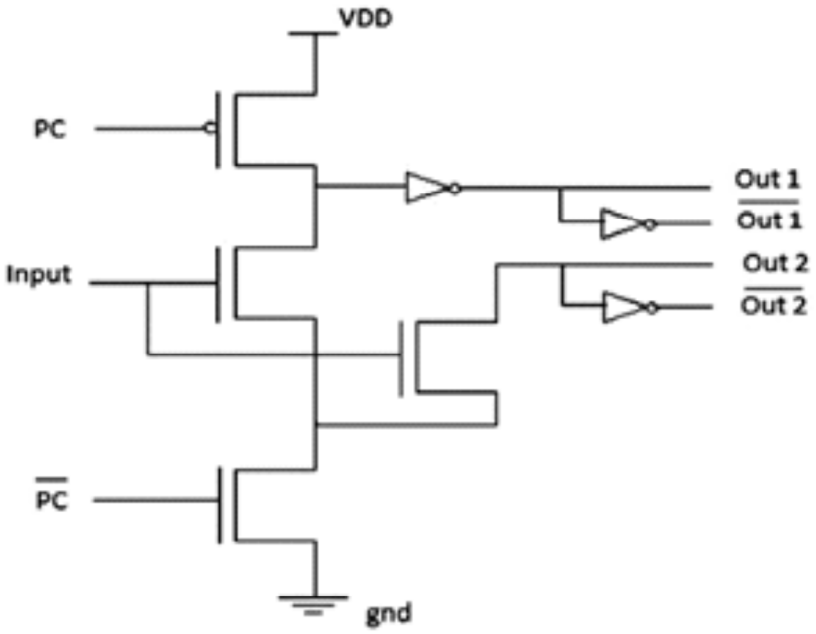

Figure 3: Single rail to Quad rail Encoding Converter

4. PIPELINE DESIGN BASED ON QUAD RAIL DOMINO LOGIC

In each pipeline stage requires a static NOR gate used as1-bit completion detector to generate an encoding handshaking signal for the entire data paths by detecting the critical path. Driving buffers deliver each total done signal to the pre-charge/evaluation control port of the each pipeline stage. Since the modified completion detector only detects the critical path, the non-critical data paths do not have to transfer encoded handshake signal anymore. Therefore, single rail domino gates alone used in the non-critical data path to save logic overhead.

Encoding converter is used to bridge the connection between single-rail domino gate and quadrail domino gate.

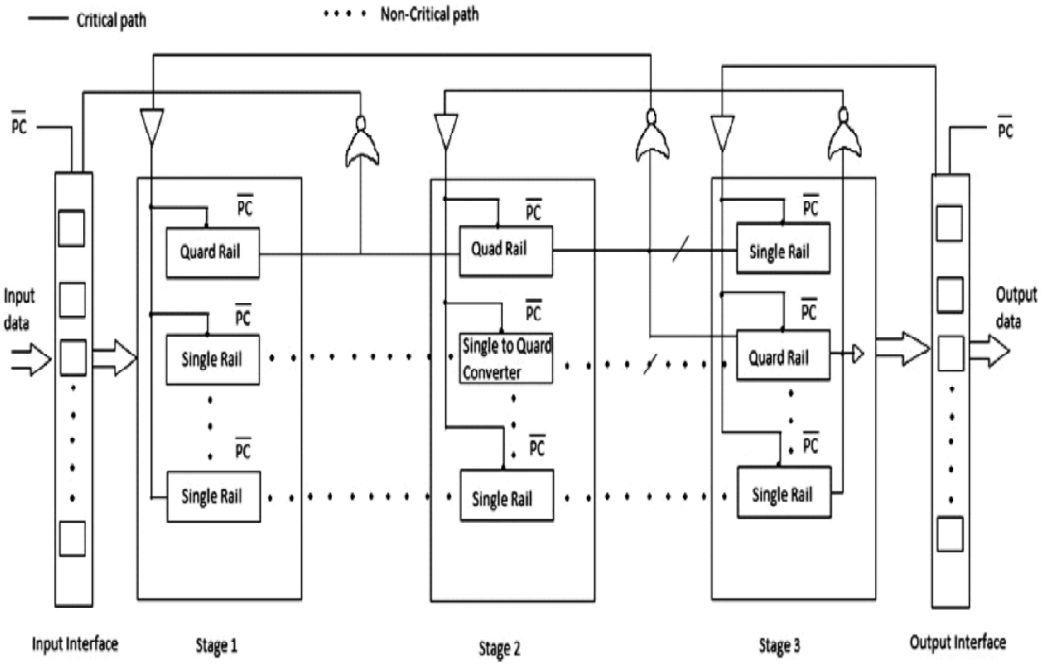

Figure 4: Structure of Proposed Pipeline Design Based on Quad Rail Domino logic

After link each pipeline stage's by SLG together, the SLG in the following pipeline stage be the previous gate to start evaluation since italways waits for the acknowledgement to the critical signal transition from previous SLG. As a result, thelinked SLG data path provides a stable data path. Linking each pipeline stage'sSLG is partially done in the process of selecting a valid signal Lin gate in each pipeline stage. The solid and dotted lines, representing the critical and non-critical data paths. In addition, the results also show that Sync-CG saves a large clock power compared with Synchronous pipeline design. However, because of the clock-gating design, Synchronous clock- gating consumes a little more power than Synchronous when the circuits operate at high speed.

The higher throughput of Asynchronous and Synchronous clock-gating related to the other pipeline performance. The higher throughput can be improved by using quad rail domino logic design, the power consumption decreases rapidly. Therefore, Synchronous and Synchronous clock-gating are re-designed by considering the high tradeoff between throughput and power. Although Synchronous and Synchronous clock-gating have the highthroughput performance with proposed design. The energy consumption of VLSI circuits relates to the toggle rate in domino data paths. In proposed, the adoption of quad-rail domino gates in the noncritical data paths saves not only silicon area by reducing transistor count but also energy consumption.

5. RESULTS AND ANALYSIS

The following figure indicates the delay analysis, threshold voltage analysis and different pipelined architecture.

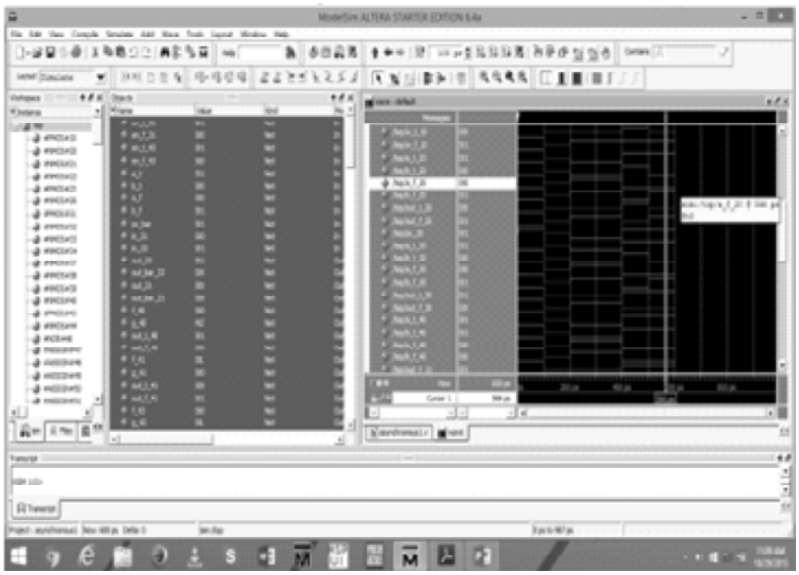

Table 1
Pipelined Architectures

Proposed Asynchronous Pipeline Design		*Bundled data asynchronous pipeline*	*Synchronous pipeline*
Logic Gate	*Domino gate*	*Domino gate*	*Static Gates*
Delay	6.86ns	8.72ns	9.75ns
Total memory	175 kb	235kb	280kb
Transistor Count	6345	8654	9120
Threshold voltage	2.6v	3.8v	4.5v

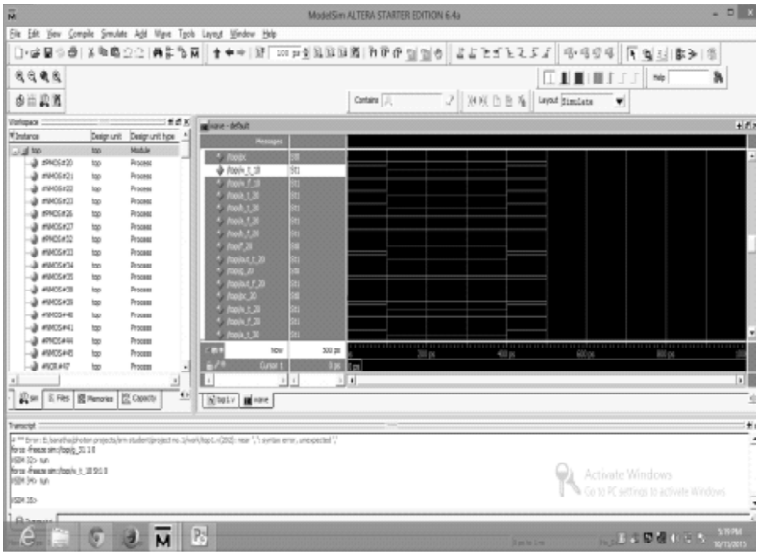

Figure 5: Asynchronous Pipeline Design Based on Constructed Data path

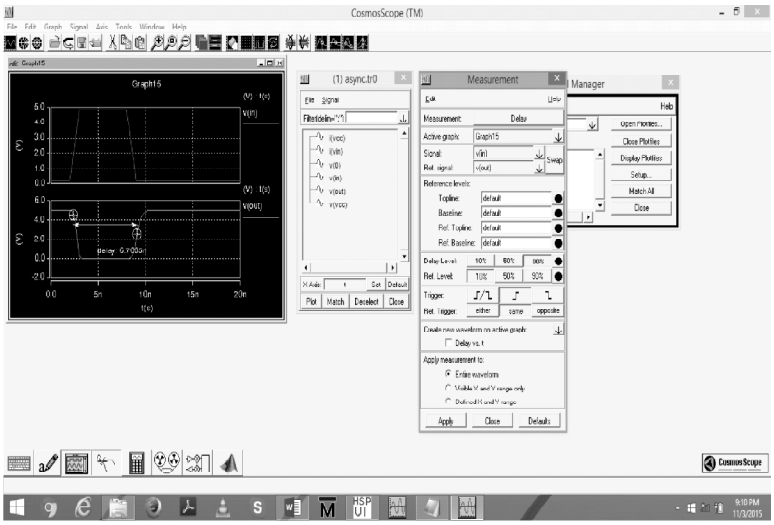

Figure 6: Delay Analysis

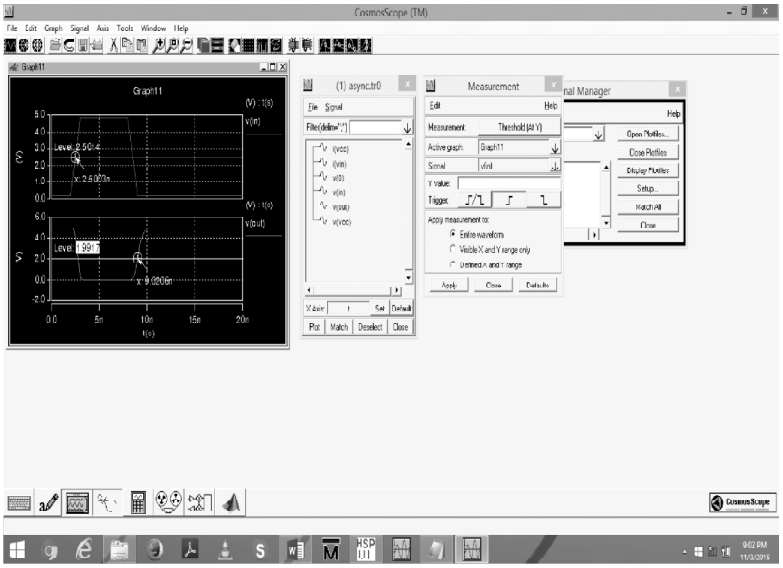

Figure 7: Threshold Voltage Analysis

6. CONCLUSION

This paper proposed ultra-low power asynchronous pipeline design is designed based on special quad rail and single rail domino logic gates. The critical data path transfers only valid data signal along with encoded handshake signal. Noncritical data paths,uses only single-rail domino data path it can transfer valid data signal (logic 0 or logic 1). Proposed asynchronous pipeline design is an interesting pipeline style that can entirely avoid explicit storage elements between the each stage by implicit latch function of domino logic gates. The latch free design features provides the benefits of reduced critical path delays and occupies less silicon area, and consumes very less power.

In order to implement modules, control logic has been separated from the data path, while provision must be made for initialization and testing. If data bundling is used, the data path will look much the same as that in a synchronous implementation. The main differences are likely to be the routing ofa data valid signal and the use of latches controlled by local signals, rather than registers controlled by a global clock signal. If Quad-rail coding is used, the logic blocks on the data path may resemble domino logic.

The Synthesis results shows in the table 1 the proposed design has better performance than bundled data asynchronous domino logic pipeline, even it compared with synchronous pipeline and synchronous clock-gate pipeline design.This proposed method of ultra-low power asynchronous domino logic pipeline focuses on improving the efficiency and reduced delay, reduced silicon area and used for a wide range of application in VLSI domain.

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