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A Novel Level Shifted Carrier PWM Technique for Neutral Point Stabilization of Five Level DCMLI

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Abstract: An existing problem with diode clamped multi-level inverter is having voltage oscillations at the neutral point. These oscillations cause uneven voltage sharing among the switching devices and increase the distortions in the output voltage. Inherent neutral point control is not possible i.e. they require extra components. However, these solutions are found not be practicable for many applications. A Novel Level Shifted Carrier based PWM technique has proposed for five level diode clamped multi-level inverter. In this the carrier shift will be done by measuring the Neutral-point voltage and current. The proposed convertor system will solve the voltage unbalance drawback of the conventional multilevel voltage-source converters, while not exploiting any extra voltage balance circuits or separate voltage sources. This technique has been verified by using MATLAB SIMULINK.

1. INTRODUCTION

The idea of multilevel converters has been introduced in 1975 [1]. Power electronic converters, particularly dc/ac PWM inverters are extending their vary of use in trade as a result of the supply reduced energy consumption, higher system potency, improved quality of product, smart maintenance, and so on. The most benefits of the multilevel inverters are Low THD, less EMI interference, higher bus utilization and low voltage stress [2]. The multi-level inverter is to synthesize a close to sinusoidal voltage from many levels of dc voltages. As range of levels will increase, the synthesized output waveform has a lot of steps, which provides a staircase wave that approaches a desired waveform. Also, as steps are added to wave, the harmonic distortion of the output wave decreases, because the range of voltage levels will increase. But multilevel converters do have some disadvantages [3]. Though the lower voltage rated switches is utilized in a multilevel converters, every switch needs a connected gate drive circuit. This might cause the general system to be more expensive and sophisticated. However the benefits of the multilevel converter have dominated its disadvantages.

As per literature there are three popular multilevel convertor structures reported, they're cascaded H-bridges convertor with separate dc sources, diode clamped, and flying capacitors [2]-[3]. However the diode clamped converter is usually used due to less dynamic voltage sharing problems, wonderful static equalization and low THD and *dv*/*dt* losses. However the drawback of the Diode clamped multilevel inverter is neutral point voltage instabilization i.e. a low-frequency voltage oscillation at the neutral point [1]. This is due to the difference in capacitor values because of manufacturing tolerances, Inconsistency in switching device characteristics, unbalanced three-phase operation [1]. Because of these oscillations in the neutral point, It causes an uneven voltage levels and hence increases output distortions, It also results in premature failure of switching devices. However, it's long been recognized that once a variety of levels larger than three is employed, capacitor voltage equalization is just accomplishable if the modulation index

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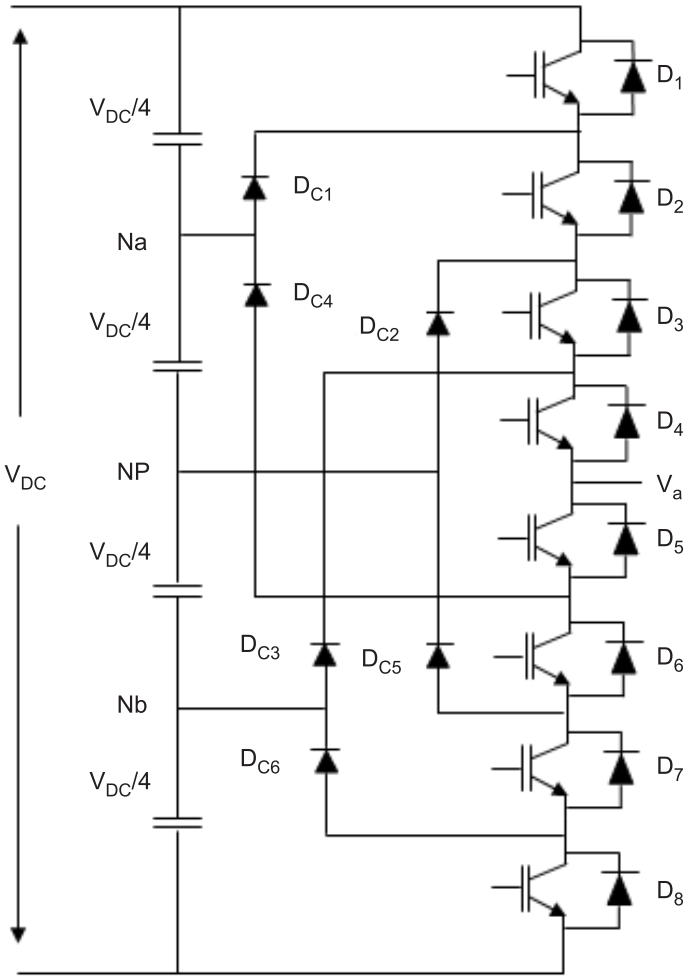


Figure 1: Five level structure of DCMLI

is restricted to max value of loads at 0.8 pf. For electrical converter applications, if the modulation indexes are beyond this limit, the middle capacitors tend to discharge and eventually the device converges to a 3 level [4]. This paper deals with the stabilization of the neutral voltage under varied loading conditions.

2. EXISTING TECHNIQUE FOR NEUTRAL POINT STABILIZATION

Generally in the existing techniques the neutral point is rather stabilized by the carrier based pwm technique or the space vector pwm technique or both which is rather termed as the hybrid. For the neutral point stabilization using the carrier based pwm technique, the DC bias is added to the reference wave [5]-[6]. So in this case the dc bias added causes the shift of the reference wave thus on generate a median neutral current of the specified polarity to balance the capacitor voltages v1 and v2. As the output waveform reflects the reference wave, the DC bias or the DC shift causes the distortion in the output waveform which rather increases the THD of the output. Then in the space vector pwm technique, the neutral point voltage is stabilized by using the redundant states of the small vectors, as the small vectors majorly affect the neutral point voltage [7]-[8]. Using their redundant states is absolutely the best way to control the neutral voltage with less distortion, but the complexity of the logic for the generation of the waveforms and for the neutral voltage stabilization is the major drawback.

In the hybrid technique, the near vector and the non near vector strategies are used [9]-[10]. The nearest vector deals with the nearest three vectors where the neutral point is stabilized using the vectors in the

sector near the reference vector which is rather similar to carrier based pwm technique. In the non-nearest vector, the neutral point is stabilized using the vectors which are rather not near to the reference vector. These two techniques are the controlled by a threshold value. But the main drawback of this technique is that the logic is very complex to determine as the both Nearest Vectors and Non Nearest Vectors strategies are the types of the space vector PWM techniques. The voltage generation is done using the carrier based pulse width modulation technique [5] which is rather simpler and the neutral point voltage stabilization is done using the space vector pwm technique [7], which is rather the best way for the voltage generation and the neutral point voltage stabilization. The procedure deals with the switching in between the sine PWM technique and the space vector PWM technique [9]. The voltage equalization management theory for the multilevel "back-to-back" rectifier/inverter system is given. The strategy depends on coordination between rectifier and inverter switching angles to attain capacitance charge balance and at a similar time minimize the switch harmonics of each rectifier and electrical converter. The strategy differs from that given in [4] this a voltage-source management is implemented on each rectifier and inverter circuits.

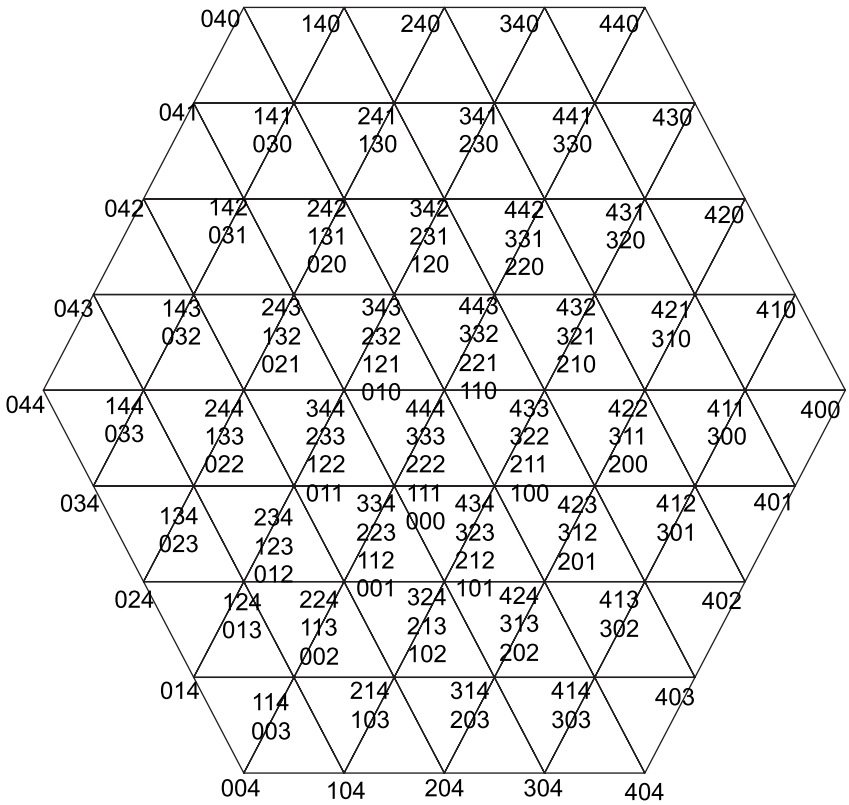


Figure 2: Space vector diagram of 5-level inverter

3. PROPOSED TECHNIQUE FOR NEUTRAL POINT STABILIZATION

The existing techniques apply well for 3-level inverter, but fails for higher levels. The paper proposes a novel level shifted carrier PWM scheme for 5-level Diode clamped multilevel inverter. In the proposed technique neutral-point stabilization for five level diode clamped multilevel inverter by done by appropriately level shifting the carrier signal [9] shown in Figure 3(b). By shifting the width of the pulses change which results in delay in turn on and turn off the switches. This result in discharging the overcharged capacitor and charging of under charged capacitor will stabilize [11]. In the five level diode clamped multilevel

inverter there are four capacitors and hence three capacitor junctions i.e. N_a, NP (Neutral point), N_b as shown in Figure 1. Unlike the existing carrier based PWM techniques were reference is level shifted, As there is only single reference wave i.e. only one degree of freedom to control the various capacitor junction. This can mitigate the neutral point voltage oscillation. But the other two junctions are not at fixed levels as expected. This results in distorted output voltage. But in the proposed scheme as level shifting of carrier is done and there are 4 carriers, There are more degrees of freedom which leads to better stabilization of all the capacitor junctions. The main theme here involves the controlling of these three capacitor junction voltages Figure 2. For stabilizing the capacitor junctions voltage the current leaving the respective junction (In) and the difference of the corresponding capacitor voltages ($V_{cn} - V_{cn+1}$) connected to that junction are measured. Using these values the dc offset i.e. error to be added to the carrier signals of respective phase is decided by following the truth table shown below in Table.1.That error is given to all the carriers of respective phases i.e., when $n = 1$ for phase A, $n = 2$ for phase B, $n = 3$ for phase C.

Table 1
Truth table to increment or decrement the value of *e* for neutral-point voltage balancing

$Sign(V_{cn} - V_{cn+1})$	$Sign(I_n)$	*Error(e)*
0	–	0
1	1	–1
1	–1	1
–1	1	1
–1	–1	–1

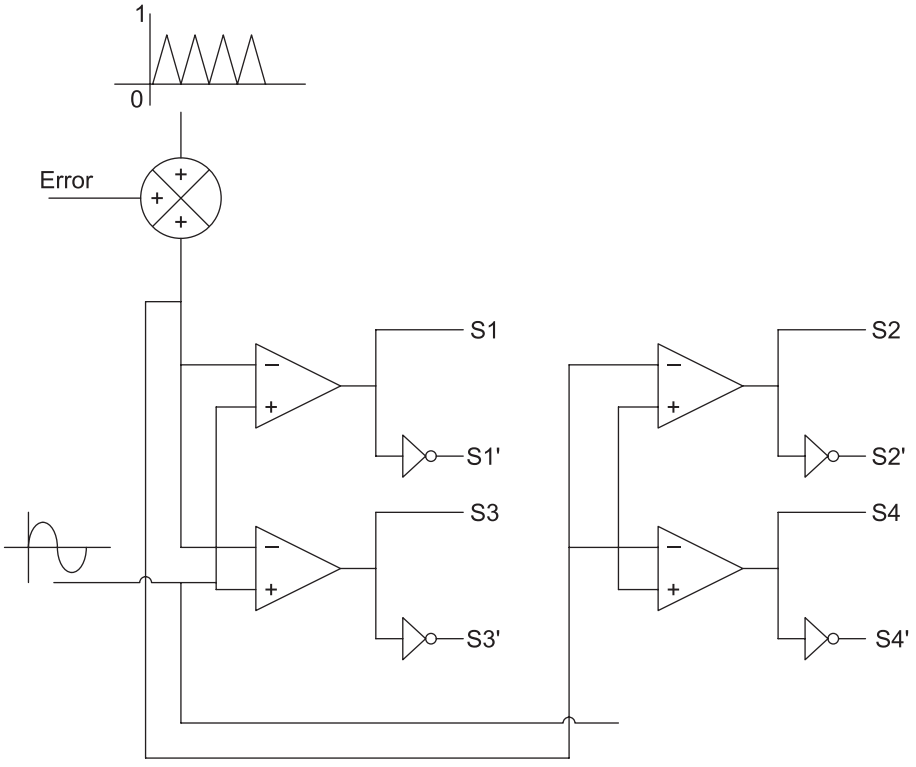
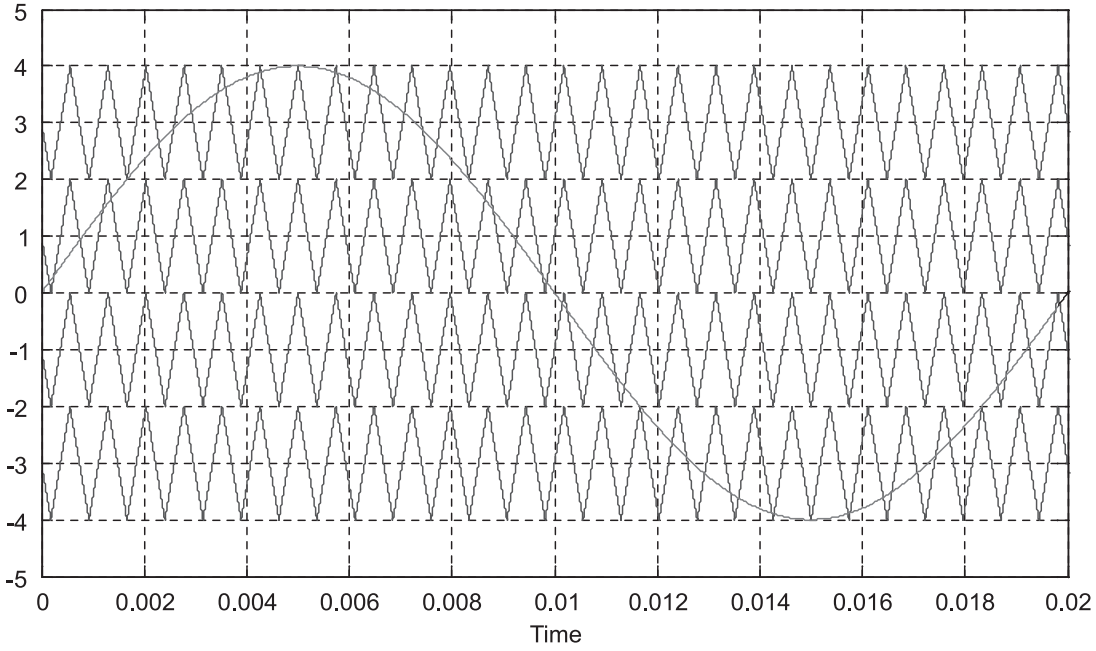


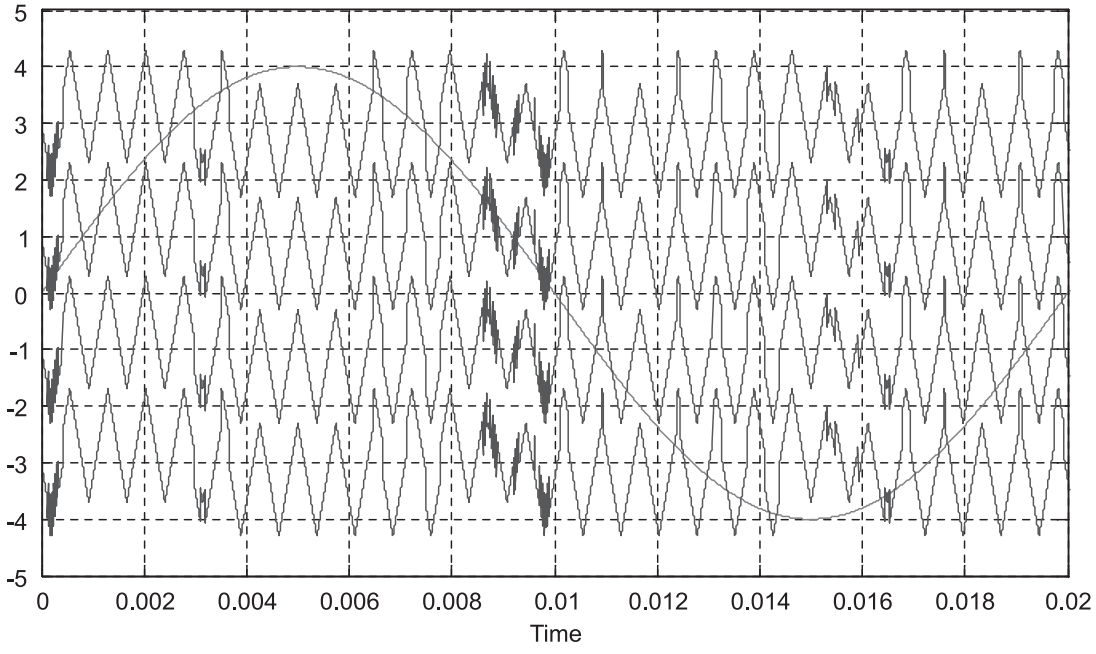
Figure 2: Schematic for level shifting carrier PWM for Neutral point stabilization

4. SIMULATION RESULTS

To appraise the performance of the proposed level shifted carrier PWM technique over the conventional PWM technique. The techniques applied to three phase five level DCMLI are simulated in the Matlab/ Simulink. By choosing the parameters as $V_s = 500$ V and R-L load is taken as 100 Ω and 10 mH. From the Figure 4, 5 observed reduction in the neutral point voltage and THD for the proposed and conventional sine pwm technique at unity power factor and Table 2 shows the Comparison of THD and Neutral Point Voltages for conventional and proposed techniques for different power factors.

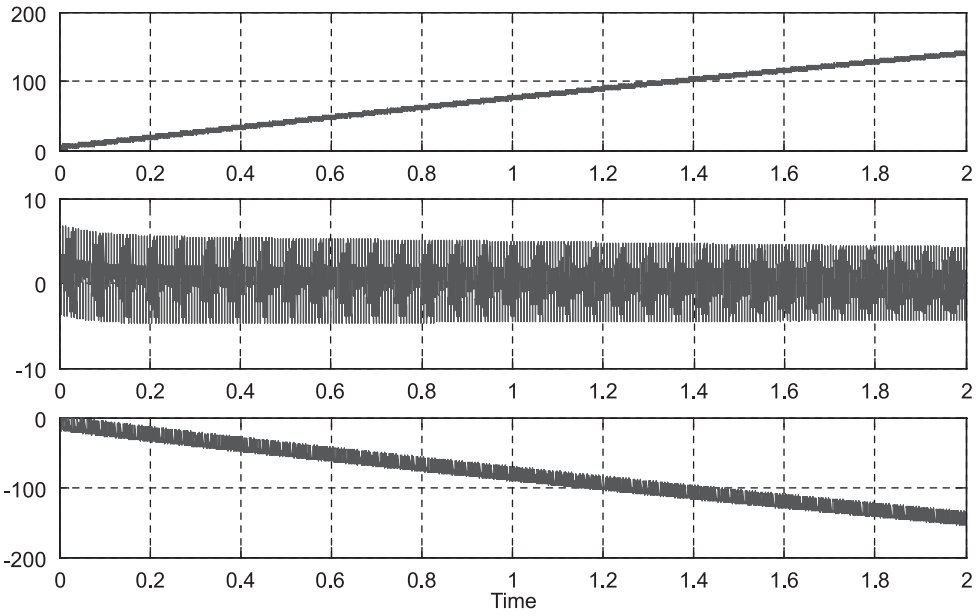


(a)

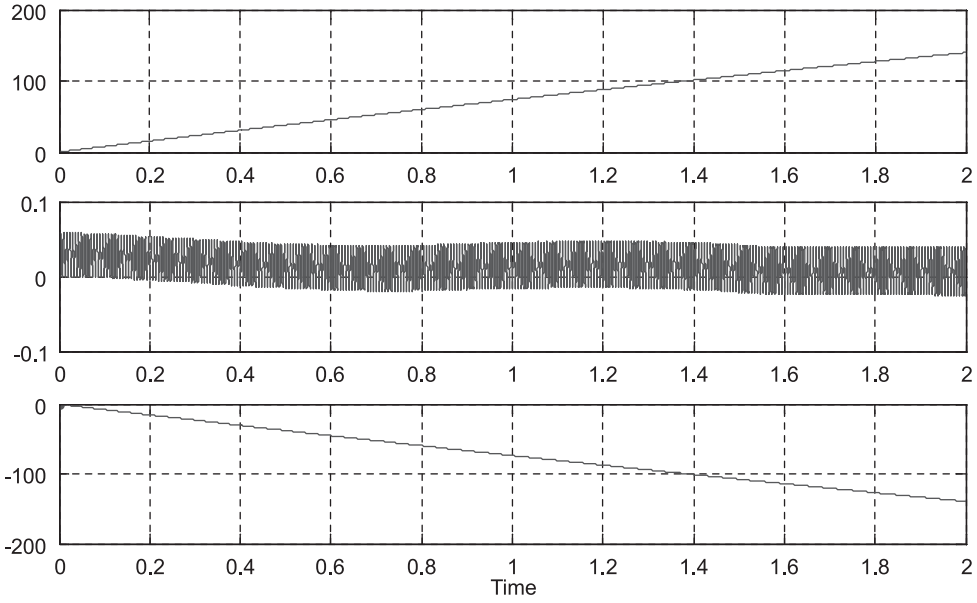


(b)

Figure 3: Modulation technique for (a) Conventional Sine pwm and (b) Proposed Sine pwm



(a)



(b)

Figure 4: Neutral-point voltage for (a) Conventional Sine pwm and (b) Proposed Sine pwm

Table 2
Comparing the THD and NP Voltage of open loop and closed loop for different power factors

Power Factor	*Conventional technique*		*Proposed Technique*	
	Neutral-point Voltage (Volts)	*THD%*	*Neutral-point Voltage (Volts)*	*THD%*
Unity	+5 to –5	15.94	+0.04 to –0.02	15.60
0.8	+40 to –40	21.32	+0.8 to –0.5	16.38
0.6	+50 to –50	19.13	+0.8 to –0.8	15.86
0.4	+40 to –40	17.20	+0.6 to –0.6	15.56
0.2	+25 to –25	15.88	+0.4 to –0.4	15.43

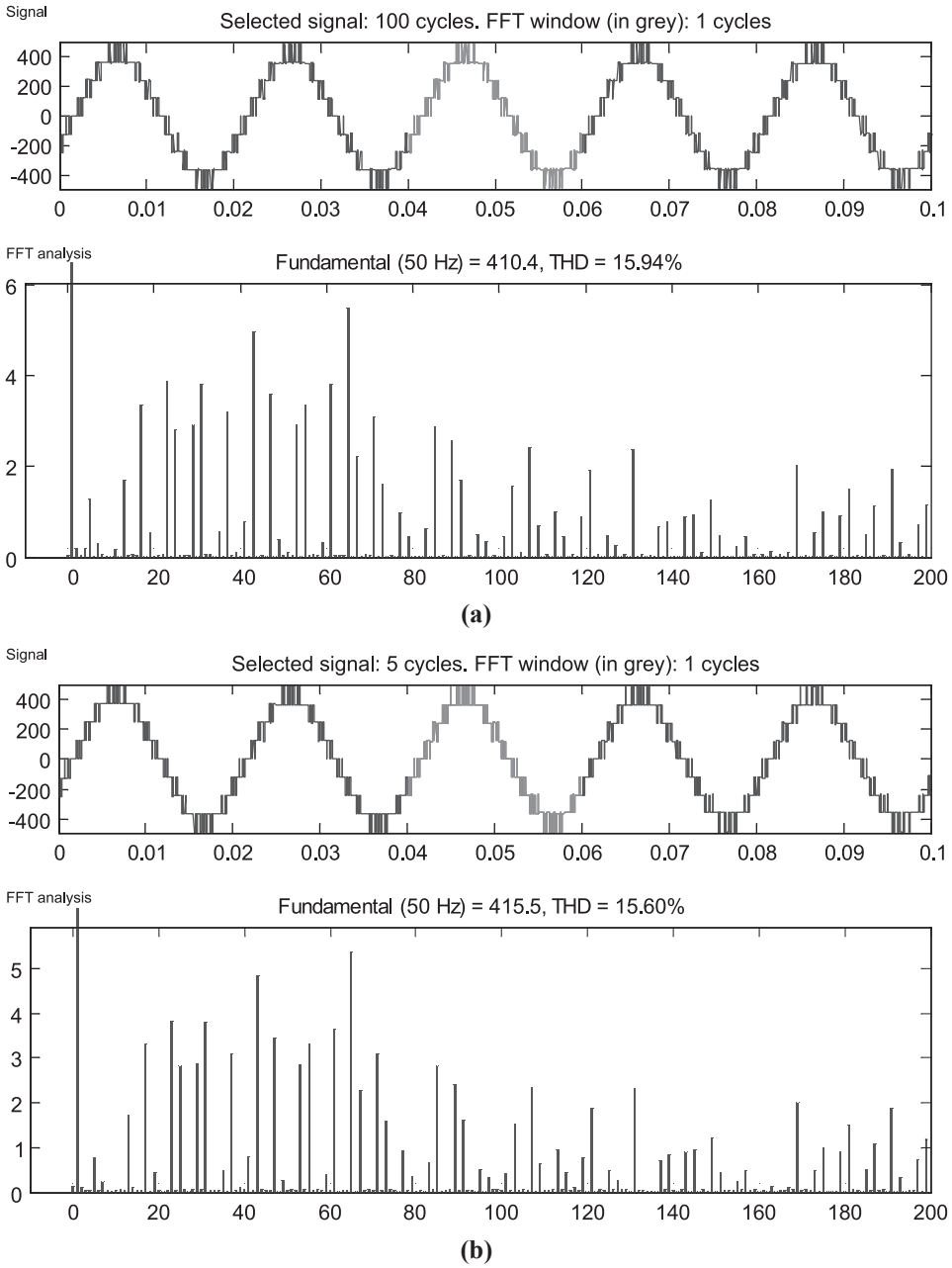


Figure 5: THD for (a) Conventional Sine pwm and (b) Proposed Sine pwm

5. CONCLUSION

A Novel level shifting carrier-based neutral point voltage balancing for a five-level Diode clamped multilevel inverter in combination with a closed-loop controller has been proposed in this paper. The proposed level shifting carrier PWM provides improved inverter performance in terms of reduced Total Harmonic Distortion (THD), harmonic profile, neutral point voltage and balanced dc link with near zero average Neutral point voltage.

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