I J C T A, 10(20), 2017, pp. 67-81 ISSN: 0974-5572

Energy-efficient Devices Using a Design of Reconfigurable Robust Integrated Power Converters

R. Dhanagopal*, V. Krishnamurthy and A. Rajaram*****

ABSTRACT

Nowadays, the application evolving interest is increased day to day in self-continued low-power. An integrated power supply solution with a configurable is accessible with an adaptive dual loop gain-pulse control and step-up/ down switched-capacitor power stage. It makes use of a stage reconfigurable design of power to execute variable gain ratios that provide efficient voltage conversion within range of power and voltage of wide input/ output. It also services an interleaving regulation scheme to significantly reduce the input inrush currents and the output voltage ripples with fast transient response. Design strategy, system optimization, and circuit implementation are considered. The converter was designed with a standard process of 0.35-,μmdigital CMOS n-well. According to the initial source, oscillate of voltage from 1.5 to 3.3 V, the transformation of elements step-up/down voltage with a load current (90 mA) is achieved converter. The system efficiency utmost is 80%. The converter responds to a 70-mA load-current step change within 4.6 μs, while it robustly operates under a 1.8-V input supply variation. The design can be easily inclusive and reconfigured for a variety of application scenarios and function.

Keywords: DC–DC power conversion; energy management; reconfigurable architecture; switched-capacitor (SC);

1. INTRODUCTION

Switching power supplies have been widely employed in consumer products. Switching power converters are generally controlled by pulse width modulation (PWM) with high switching frequency; therefore, it has the characteristics of high efficiency and light weight. However, due to the constant switching frequency, few dominated harmonic clusters will show on the spectrum. The electromagnetic interference (EMI) will cause the dominant harmonic clusters to supplementary electronic devices through radioactive or conductive. EMI is a very important issue in power supplies, due to the high-voltage/high-current switching. Therefore, power supplies have to meet the electromagnetic compatibility (EMC) standards, such as Federal Communications Commission, and before selling in different countries[1]–[3].

Instead of adding an EMI filter [4], [5] on the input side of power supplies, several random-switching techniques have been developed to reduce the EMI. Random-switching techniques have been widely used in motor controls [6]–[9]; however, in recent years, similar methods have been implemented on power converters [10]–[14] to reduce the power of dominant harmonic clusters, thereby reducing the cost of EMI filter.

One of the special features of random-switching PWM is to spread the dominant harmonic clusters to reduce the power of dominant harmonic clusters. Several random switching PWM techniques have been proposed [15]–[18]. They can be classified into four categories, including random carrier frequency modulation fixed duty (RCFMFD), random carrier frequency modulation variable duty (RCFMVD), random PWM (RPWM), and random-pulse-position modulation(RPPM).

* Research Scholar, Anna University, Chennai, India

** Former Professor, Department of Electronics and Communication Engineering, Anna University, Chennai, India

*** Professor, Department of Electronics and Communication Engineering, EGS Pillay Engineering College, Nagapattinam, India

For digitally controlled power conversion with feedback control, the sampling frequency affects the bandwidth and related controller design specifications, thereby changing the parameters of the controller. One of the most important factors to the development of random-switching PWM techniques for closed-loop digitally controlled system is retaining constant sampling frequency. Some of the previous random-switching PWM techniques [15], [16] require randomly changing the sampling frequency. Also, it became difficult for closed-loop applications.

Some methods [17], [18] provide constant sampling frequency while not keeping constant average inductor current, which results in the increase of output voltage ripple. This paper presents a new random-switching PWM switching technique with constant sampling frequency and constant average inductor current. It can be easily applied to closed loop digitally controlled power converter while not increasing the output voltage ripple.

The setup of field programmable gate array(FPGA) based digitally controlled buck converter system experimental has been arranged. The converter circumstances include input voltage = 5 V, frequency switching= 200 kHz and output voltage = 1.5 V. The proposed pattern random switching is implemented by software. Experimental results initiate the random switching efficiency of pattern. The rest of the manuscript is arranged in section wise. In this section the intro and survey of application in pattern switching. In section II the converter of discrete DVS is explained. The proposed work is discussed in section III. The system implementation and simulation results are carried out in section IV and V. Finally conclusion is available in section VI.

2. DISCRETE DVS CONVERTER

This section objective is to present a great control law performance for the converter of discrete DVS. This controller is essential to satisfy the needs originated earlier for the transient periods, i.e., through the voltage output is scaled from a less level voltage to great voltage level (increasing period of transient) and from the voltage level of high to a less level of voltage (dropping period of transient). This controller is aimed to deliver constant performance by using methodology of control. In the stable states, the extreme constant voltage and the smallest stable voltage obtained where based on various factors it is problematic for estimation. It catches the errors model of PMOS, current differences, voltage supply, and the resistive damages through the switched on of the PMOS transistors.

Statement: are lesser with detail to and no variations of the properties stability system. Some models are achieved in such a manner that the performance of the system of closed-loop with the controller's variations is shown. The PMOS transistors total number is in the system and the schematic of adder for converter are shown in Fig.1. Also, at least switch on of one active transistor is must and supply voltage is V.

The reference signal is a stage between the high and less level of the voltage V. The resistances system are R and the capacitance is nF while, the voltage threshold is V, and frequency of the system is MHz The frequency sampling has the similar value that the frequency of the clock. As a final point, the reference signal slope is V/s.Wave equation for the device is given by,

$$\frac{\partial^2 u}{\partial t^2} = v^2 \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \right) \tag{1}$$

Where, u is pressure and v is velocity. The growth of the better controller performance for the converter of DVS is stimulated by the "intuitive control" which is processed in [7], under the procedure in this law, only one switches of transistor is consider at every time sampling as per the error voltage sign. So, there is limitation in controller that not more than one transistor can be on or off switched at each time sampling.

Likewise, it is applied using 4 bits in fixed-point. So, this controller offers a general execution and the results as an oscillatory performance with significant peaks current. The other control alternative is proposed without the limitation. In that swapping of on or off of one transistor is possible until the number of transistor is limited by 1.

Remark: The design of control law is in such a way that the preferred voltage output relates to one of the bounds saturation or, meanwhile they relate to the level of voltage lower or higher, correspondingly. It will be planned using the nonlinear continuous-time directly. It is lead to an expression of continuous-time controller and will be almost discredited.

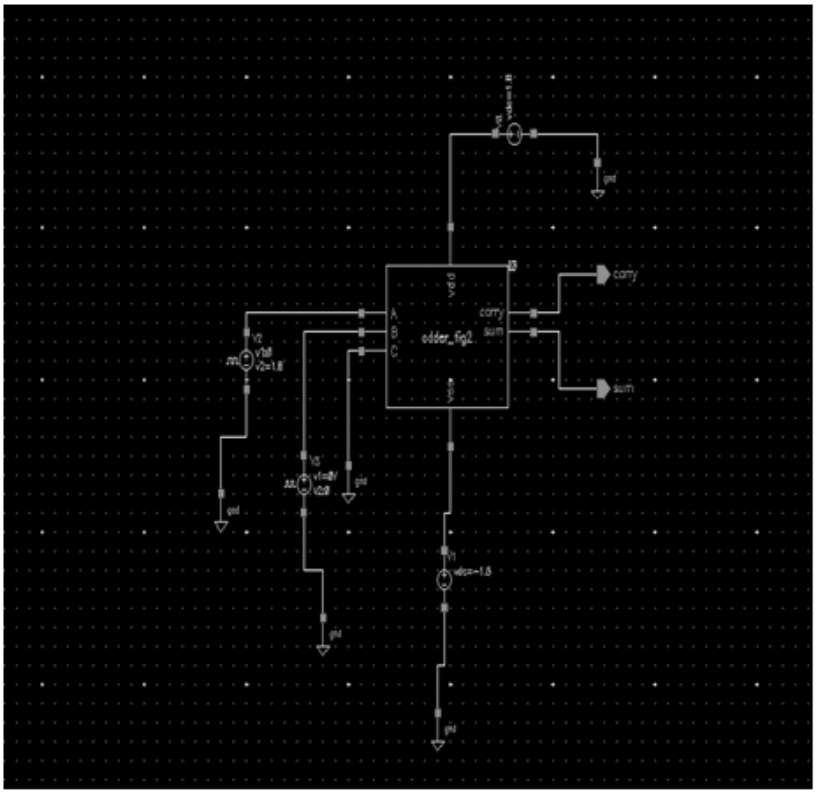

Figure 1: Schematic of the adder for the converter

Similarly, it is actual frequent in the automatic control field [13], [14]. The application of this controller of discrete-time is shown in the block diagrams. The algorithm elaborates as:

$$\frac{\partial v_i(\vec{x},\mathrm{t}))}{\partial t} - b(\vec{x})\frac{\partial \sigma_{ij}(\vec{x},\mathrm{t})}{\partial x_j} = b(\vec{x})\left[f_i(\vec{x},t) + \frac{\partial m_{ij}^a(\vec{x},\mathrm{t})}{\partial x_j} \right]$$

$$\frac{\partial \sigma ij(\vec{x},\mathrm{t})}{\partial t} - \lambda(\vec{x})\frac{\partial v_k(\vec{x},\mathrm{t})}{\partial x_k}\delta_{ij}$$

$$-\mu(\vec{x})\left[\frac{\partial v_i(\vec{x},\mathrm{t})}{\partial x_j} + \frac{\partial v_j(\vec{x},\mathrm{t})}{\partial x_i} \right] = \frac{\partial m_{ij}^s(\vec{x},\mathrm{t})}{\partial t} \quad (2)$$

3. PROPOSED WORK

In this section, proposed an adaptive law in order to manage with the case of parameter load is unidentified or/and slowly changes. Signify as the expected value for the parameter of load. This will be processed

instead of the certain simulations controller real value in the converter of DVS is achieved by using the reported information. In order to achieveadded accurate tests, a supple mentary specific model for the load is measured in such a manner that is contingent, i.e., it is varying the time.

The closed-loop results are done by retaining the ideal reference of voltage and the mechanism variation. It is executed the system can attain a comparable results to the recognized load case. Although, the adaptive control starts a delay in the response of system, the less peak current and speed transient periods are attained. This is accomplished by using 4 bits in fixed-point. Acquire the real value of approaches, in meanness of the circumstance that is varying time. The algorithm involvedas:

$$\frac{\partial \theta}{\partial t} = -\frac{u}{ah_x}\frac{\partial \theta}{\partial \lambda} - \frac{v}{a}\frac{\partial \theta}{\partial \varphi} - \dot{\sigma}\frac{\partial \theta}{\partial \sigma} + F_\theta \tag{3}$$

3.1. System Specifications Andproposed Topologies

In FCEV applications of high-power, the main disadvantages of consuming converters of conventional boost are complex in components magnetic of the design and great ripple current input, which influence perhaps lead to reduction of FC stack lifetime. Decreasing the current rating and applied voltage to passive and components of power electronic (keeping the similar scheme valued power) is a planned solution. This creates construction of the magnetic moduleeasier, giving additional flexibility for the power electronic selection of components involved in the converters. Itis withthe outcomes of floating and input interleaving, which allow not onlydecrease in stress of current so voltage, unlike predictable topologies interleaved.

Benefit of FIBC N-phase are: growing the efficiency of complete converter; raising frequency of the ripple input and output without switching the frequency increasing;decreasing input of ripple current; improving the reliability of the system by paralleling stages andnot by multiple devices paralleling; reducing ratings of voltage and current of power electronic devices; decreasing the weight and size of the passive modules. The conditionsof system are presented the ratings of current and voltage of FIBCs islesser than that ofthe enclosing boost converters.

For the similar power FC rated, the simpleduty cycle of boost is greater than the topology proposed. The greater cycle makes lesser the efficiency of the converter. The approach involved:

$$I \approx \langle f_H \rangle N = \frac{1}{N}\sum_{i=1}^{N} f_H(\vec{x_i}) \tag{4}$$

Where, $\vec{x}_i$ is the input vector, N is the number of sample points, and $\langle fH \rangle N$ is the sampled mean value of the quantity. Fig. 2 shows the multiplexer module schematic diagram.

3.2. Generation Of Phase Circulating Current

The zero-sequence voltage can be injected into the reference phase voltage directly. However, the generation of phase circulating current is more difficult. In order to avoid the phase circulating currents flowing into the dc link, the sum of three phase circulating currents should be zero. Both the upper and the lower bridge reference voltages must subtract the same voltage upcx to cancel out the voltage across bridge inductor l so that the phase circulating currents will not affect the output currents. It shows the equivalent circuit after injecting zero-sequence voltage and phase circulating currents, in which each bridge is equivalent to several controlled voltage sources.

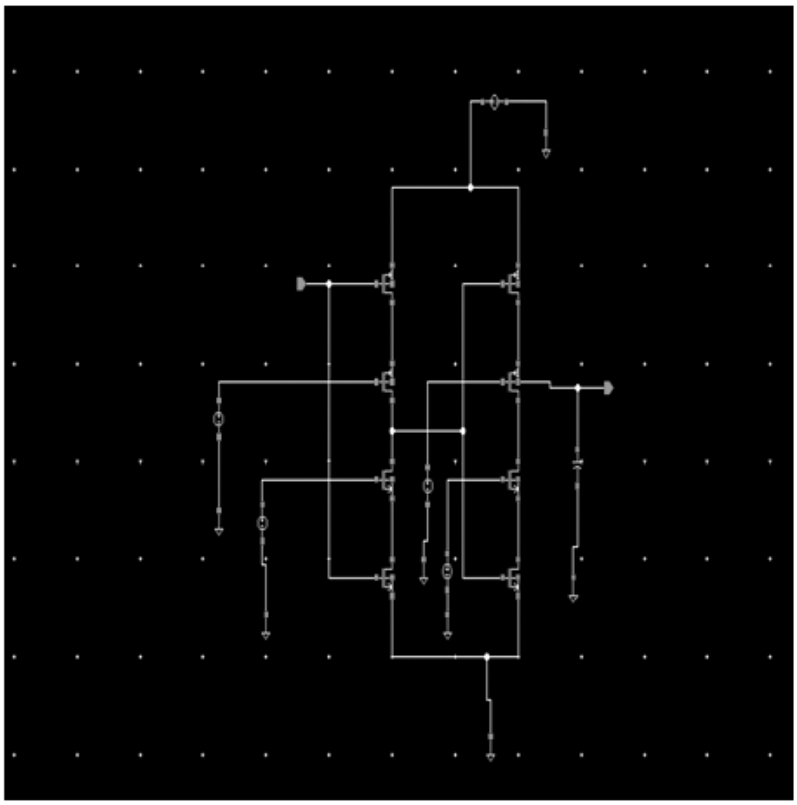

Figure 2: Schematic of the multiplexer module

According to super position theorem, can be regarded as the superposition and where shows the equivalent circuitof only injecting zero-sequence voltage. The limitation of this voltage-fluctuation-suppression method is that it cannot be applied to high modulation indices.

When the modulation indexes very high and close to one, Uz will be close to zero, and then, the phase circulating current will be increased quickly. However, it is very suitable to drive an IM with voltage/ frequency control in which the modulation index is proportional to the frequency. When the frequency is lower than a certain value, the modulation index is also lower than a corresponding value. So the voltage-fluctuation-suppression method canbe used under a certain frequency and modulation index. When the modulation index and frequency are higher, the capacitor voltage fluctuation is not so acute, and only the voltage balancing method is used.

3.3. Operating Principles and Terminology

The M2C consists of series connected half-bridges with capacitors. These half-bridges are referred to as sub modules and the converter is controlled in such a way that the voltages across the sub module capacitors are kept close to their nominal values. In this way, the sub modules capacitors perform as sources of voltage that can be any of include or bypassed in the chain of series connected sub modules. In each phase, the sub modules are divided into two arms withN series connected sub modules per arm. Each arm also has an arm inductor with the inductance and resistance R. The arm is connecting the ac to the dc positive terminal and referred as the upper arm. Likewise, the arm that is connected between the ac terminal and the lower arm is referred by the negative terminal of dc. The voltage at theac terminal can then be controlled by varying the number of inserted sub-modules in each arm.

3.3.1. Modulation and Control

Numerous control strategies have been proposed since theM2C was introduced in [1]. These control strategies may be based on phase-shifted carriers as presented in [18], or depends on the sorting approach which

presented in [1], such as the controllers in [17] and [13]. It is also possible to use programmed modulation or model predictive control as presented. Any control scheme for the modulation and control not only consider the another option and direct voltages, but also certain internal state variables like the separate sub-modules capacitor voltages. Many control methods also consider the circulating current flowing of each phase leg of the dc-terminals.

For the analysis in this manuscript, assume that the current circulating is managed. So, harmonic components are not in the circulating current implying that idc is equal to the direct component idccorresponding to the power exchange between the converter and the dc link. Also, assume the voltage balancing of the capacitor within the arms. In reality, however, there may be small changes among the separate capacitor voltages in each arm due to the limited switching frequency. Therefore, the limits of voltage should be select for the less variation from the average value can be tolerated.

3.4. General Considerations on Energy Storage

By controlling the converter in such a way that the value of kdc is greater or less than unity, the time average of the stored energy in the sub-modules is affected. It is evaluated even if the average time of the available voltage has been reduced the converter can still operate without entering the region of over modulation.

Peak Voltage and Energy Storage Capability the voltage in each sub-module will vary with time as the capacitors are charged and discharged due to the arm currents. The maximum voltage is depends on the sub-modules rated voltage and it must not go beyond the limit. In order to take this into consideration, the factor kmax is introduced. This factor defines the upper limit of the capacitor voltages and is defined such that the instantaneous value of the capacitor voltages is never greater than kmax times Vd over N. Accordingly $vcap \leq kmaxVdN$.

In this analysis, it is assumed that the capacitor voltages are well balanced within each arm. However, in most applications the separate voltage capacitor in every arm will deviate from the average value due to the limited switching frequency. The capacitor voltages spreading in each arm is based on the switching frequency, the capacitor voltage balancing strategy and even the number of sub-modules [13]. Therefore, the spread in the capacitor voltages is not included in the analysis. The voltage limit kmax is defines the minimum possible peak voltage which is achieved when the capacitor voltages balanced in every arm.

Therefore, the voltage limit kmax must be chosen such that individual variations in capacitor voltages can be allowed. The limit kmax is directly related to the maximum amount of energy that can be stored in each are that is, if the capacitance C of the sub-module capacitors is equal to or greater than Cmin the inequality (13) is satisfied. The excess energy ΔE_{max} must be stored in the arms converter based on the converter specifications. This means that ΔE_{max} can be calculated from the requested power transfer capability, dc-link voltage, and a side voltage. Thus, ΔE_{max} does not depend on the size of the sub-module capacitors or number of sub-modules. It is observed that the minimum requirements of the energy storage capability only depend on ΔE_{max}, the constant kmax, and kdc. The size and cost of the sub-module capacitors are proportional to the rated the capability of the energy storage. So all converters, regardless of the number of sub-modules per arm and have similar restrictions for the overall size and cost of the sub-module capacitors.

3.5. Adaptive Power Transistor Sizing Scheme

To further improve the overall efficiency, an adaptive power transistor sizing (APTS) scheme is proposed to optimize the power stage of the converter on the circuit level. Conventionally, with a fixed load and a fixed output voltage, the size of each power transistor is determined by minimizing the sum of conduction and switching losses [16], [17]. Fig. 3 shows the control of power delivery of the system.

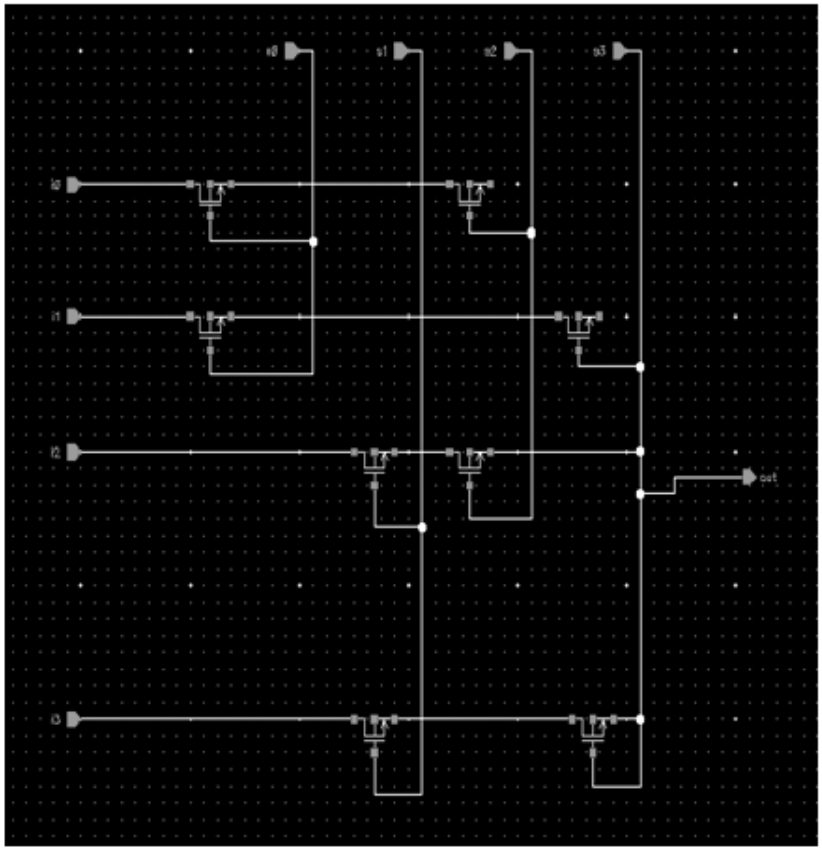

Figure 3: Multiplexer for the power delivery control

Several techniques have been presented in [5], [18] to adjust power transistor size at different load. However, for the proposed reconfigurable adaptive power converter, where input/output voltage, load power and conversion ratio are largely variable, the optimization for each power transistor's size becomes very difficult with different operation conditions. The APTS scheme is thus proposed to solve this problem. Compared to the prior arts, in which the transistor are sized only based on the load current, the proposed APTS adaptively optimizes each power transistor in different operation modes, based on the instantaneous load power, which is directly detected by an on-chip power meter.

Therefore, the optimization is more accurate; especially with variable input/output voltage. Here, each power transistor is divided into a group of sub-switches. The on and off of each sub-switch is jointly determined by the operation mode, input/output voltage, instantaneous load power and inductor current level, so that power loss is minimized at each particular operation condition (start-up period, pseudo-buck mode, pseudo-boost mode and transition mode). In addition, during the line/load and DVS transients, sizes of power transistors can also be adaptively adjusted to maintain maximized power efficiency.

3.6. Control Strategies in the Proposed Converter

As the operation scheme targets to overcome the challenges on power stage, the increase of also imposes strict constraints on the controller and buffer designs. For high switching frequency, due to the limited bandwidth and large compensation capacitors, a PWM controller does not suffice here. The conventional hysteresis controller is well known for its fast transient response and unconditional stability.

However, because of the finite hysteresis window between two voltage bounds, the processing speed is limited. The delay introduced by the finite hysteresis window between and, which overwhelmingly dominates the total delay, as shown in the figure. To reduce and, very fast comparators are needed, which consumes

much higher power consumption. In addition, for the conventional hysteresis control, output voltage ripples are mainly determined by the width.

4. SYSTEM ARCHITECTURE AND IMPLEMENTATION

It consists of a highly reconfigurable power stage, aSBHC, an adaptive frequency compensator (AFC), a GM operation controller, and an adaptive substrate multiplexer (ASM). The power stage of the proposed converter is automatically reconfigured by the GM operation controller to achieve step-up/ down power conversions. Each bulky power transistor is divided into a group of several sub switches, which are connected in parallel and controlled separately. The size of each power transistor can thus be adaptively optimized at different regulation conditions and operation modes, based on the proposed APTS scheme.

In addition, a freewheeling switch is also included to modulate and assist single-bound voltage regulation. Since the freewheeling period is usually very short, and the average current in is very low, no APTS is applied to. Meanwhile, the ASM automatically selects the higher voltage between and to bias the substrates of PMOS power transistors, preventing the converter from large leakage currents and potential latch-ups.

For the controller design, is first sampled by a resistor divider and, and fed into the SBHC to determine the coarse duty ratio, An AFC is then applied to compensate, so that the switching frequency of the converter can be well regulated under all operation conditions. Finally, the GM operation controller defines the ultimate gate control signals and automatically reconfigures the converter to the optimal operation structure. The power density over A_{beam} is

$$S_R = \frac{P_{rad}}{A_{beam}} = \frac{P_T / L_t}{A_{beam}} \text{ w/m}^2 \tag{5}$$

4.1. Current Ripple Input Evaluation

The numerical expressions for input current ripple are derivative under six assumptions. The capacitor and inductor resistances are insignificant. Switches are supreme and same in passive apparatuses. The parallel function of switches (360/N)° out of stage. Itoperates in continuous conduction mode (CCM). The ratio of ripple to the current inductor is given by

$$M(D) = \Delta iFC/\Delta iL \tag{6}$$

Where, X is the gap among two values of duty cycle, subsequent in ripples of zero current. The input ratio is differing to the inductor as a duty cycle utility.

It can be perceived that cancelation of input happens at explicit cycles, which are 1/N multiple duties, such as in a FIBC two-phase is 0.5; 0.25, 0.5, and 0.75 in a FIBC four-phase; and 0.16, 0.33, 0.5, 0.66, and 0.83 in a six-phase FIBC. Also, it is clear that the input current ripple is continuously lower than the ripple current inductor. The fact is always low than the inductor which allows to rise this latter, accordingly.

Though, because of core losses reducing both the flowing of current and inductor value is to decrease its cost, volume and weight. The suitable way is to display in what manner the current ripple inputreductions with the amount of stages is to regulate this leading according to the specifications of system for anassumed value of inductor. For this assessment, the value will be selected as 50 μH. It is not the circumstance from a two-phase or one-phase to a FIBC four phase.

As dependent on the system graded power, a FIBC six-phase can have input larger than a four-phase, which is not the circumstance when associates a four-phase with a two-phase for some power rated. Therefore, from the input the view of point is reduced and can show the advantages of converter of six-phase. So,

attractive analyzed with its costs and complexity improvement. The interval is updated in pattern Q for every character and moving from the last to the first character:

$$k_{new} = c(\mathrm{x}) + \mathrm{s}(\mathrm{x}, \mathrm{k}_{\mathrm{current}} - 1)$$
$$l_{new} = c(\mathrm{x}) + \mathrm{s}(\mathrm{x}, \mathrm{k}_{\mathrm{current}}) - 1 \quad (7)$$

Where, pointers k and l are respectively the smallest and largest indices in the SA which starts with Q, the symbols in the sequence of BWT as c(x) (frequency) that are lexicographically smaller than x and s(x, i) (occurrence) is the total symbol occurrences of x in the BWT sequence from the 0^{th} position to the i^{th} position. Fig. 4 shows the power inverter schematic diagram.

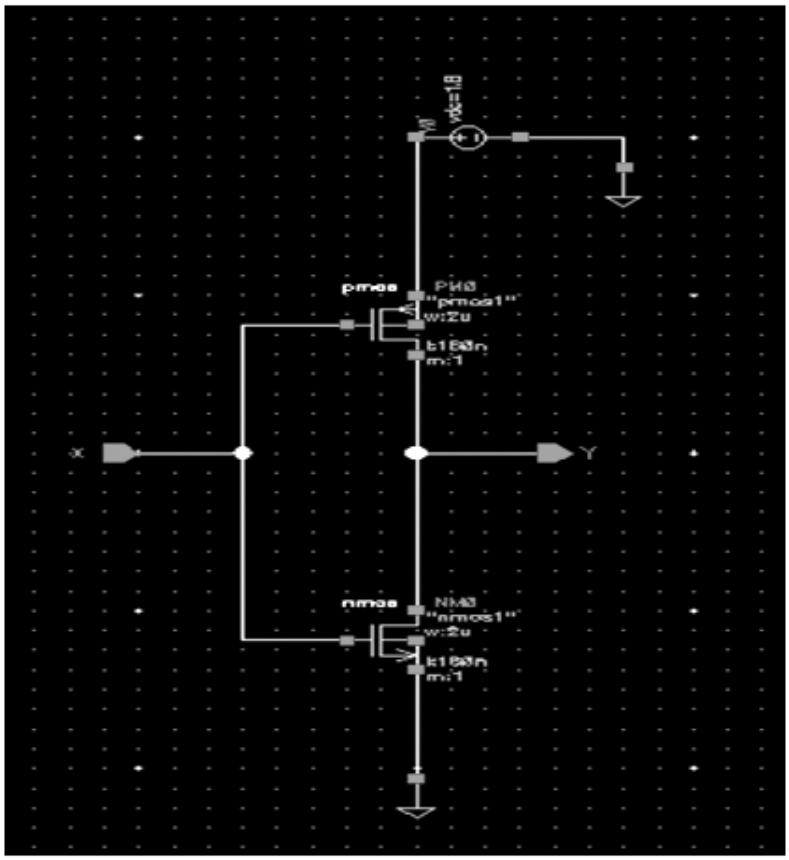

Figure 4: Schematic of the inverter for the power

$$p(X|\lambda) = \sum_{i=1}^{M} w_i g(X|\mathrm{u}_\mathrm{i}, \sum i) \quad (7)$$

4.2. Inductor Volume Evaluation

To estimate the decrease in the volume of inductor for the planned topologies is analyzed with the conventional boost. It is essential to go over the electromagnetic details used for comparable magnetic cores. In the investigation, the core material chosen is ferrite. Specifics trategies of material of magnetic I chosen and compared for larger power $\Delta B = 0.2$ T is the alteration in density of flux J, which is the variation of current density among 2 and 5 A/mm2.

In the investigation, it selected coefficient as 3.5 A/mm2.kB which is higher than 1, which proceeds into account. The variations is carried out among the section effective of the conductors and the section needed windings. It is connected to the conductor's form and occurrence of the various isolation levels.

Likewise, it is selected as (kB = 1.5) kb is a coefficient geometric, and in our case, it is occupied to be equivalent to 1. Equivalence exposed the reduction given in whole energy stored inductor and connected volume magnetic, as related by the converter of conventional boost. In the traditional boost, Inductor (I) are the energy stored respectively.

Inductor (N) is the energy deposited in the inductor of single-phase and the equivalent of the FIBC N-phase volume, separately. E(N) is the energy of inductor storage and V (N) is the decreased volume, respectively, given as:

$$E(N)100=EInductor(I)–N\times EInductor(N)\ EInductor(I)$$

It allows heating capacitor reduction of resistive losses due to the corresponding internal of series resistance (ESR). The current RMS and the temperature capacitor lesser is the lengthier of the lifetime capacitor. The boost current of RMS capacitor is as the operations of the duty cycle.

The complete storage of volume and energy is the standard from boost conventional to a FIBC two-phase and decreased by 62.6% and 49.3%, correspondingly. For a FIBC four-phase, it is decreased by 86% and 83.7% and for six-phase is by 87.2% and 87.35%, respectively. At the feed of power is given below.

$$P_{rad} = \frac{P_T}{L_t}\ \text{w} \tag{8}$$

4.3. VARIATIONS IN THE STORED ENERGY

In order to calculate the minimum energy storage requirements, the excess energy storage ΔEmax must be known. The injection of harmonic is the reason for the excess needing of energy storage is calculated both for a sinusoidal voltage reference and for this injection of third-order harmonic are used. The energy storage requirements only depend on the voltage limit defined by kmax and the excessenergy ΔEmax, but also on the constant kdc. The value of kdc can change by managing the average time of the energy stored in the converter. There are, however, certain limitations for how the value of kdc can be chosen.

The reason for this is that when the voltage vu or vl is to be inserted in the arm of lower or upper, the voltage need must be presented in the sub-module capacitors of the corresponding arm. If the sum of all capacitor voltages in the arm is lower than the requested voltage that should be inserted, then this will result in over modulation. Consequently, the value of kdc must be chosen such that the requested voltage is available in the sub-module capacitors at alltimes. As the limit for over modulation is determined by the instantaneous values of the demand and voltages available, the capacitor voltage ripple shape will have an impact on the storage energy needing.

By injecting harmonic apparatus in the circulating current, it is possible to shape the capacitor voltage ripple in such a way that kdc can be reduced even further. Injecting harmonic components in the circulating current and the converter losses is increased, which means that such methods should not be used unless necessary. As this paper investigates the minimum energy requirements during nominal steady-state operation, these category of region operating extension approach are not incorporated in the analysis.

4.4. Calculating the Required Energy Storage

The maximum voltage that can be inserted in every arm is the total capacitor voltages in the arm. This voltage is referred to as the available voltage and is denoted as v∑cap. As it is assumed that the capacitor voltages are well balanced, the relation between the available voltage and the energy that is stored in the arm can be expressed as arm = N2 Cv∑capN2. The instantaneous value of the stored energy in each arm can be expressed as the sum of its time average arm and its alternating components.

Due to the symmetry of the system it can be concluded that if is satisfied, and then is satisfied as well. It is therefore sufficient to consider only one of the arms when calculating the energy storage requirements. In order to avoid over modulation, the value of kdc should be chosen large enough such that is satisfied at all times. The operating range can be maximized by choosing kdc equal to the minimum value that satisfies. This will allow the highest possible voltage ripple in the sub-module capacitors without entering the region of over modulation or exceeding the allowed peak voltage.

The insignificant energy storage is needed and can be calculated for any given operating point and voltage ripple limit using. This is done by first calculating the value of ΔEmax for the given operating point by using for a sinusoidal voltage reference, or if the third-order harmonic injection is used. The minimum value of kdc for the considered operating point is then given. Since ev,u represents the normalized value of eu , it does not depend on the power transfer S. Thus, the only term in that depends on the power transfer is ΔEmax.

From the results, it is clear thatΔEmax is proportional to the apparent power transfer S. As a consequence, Enom and Emaxare proportional to the apparent power transfer as well. Therefore, it is possible to express the energy storage requirements in terms of total energy storage per transmit VA. Therefore, converter of three-phase with six arms the energy storage requirements can be expressed asWconv = 6SEnomWrated = 6SEmax where Wconv is the required nominal energy storage in the converter per transferred VA, and Wrated is the rated energy storage capability of the converter. It should also be made clear B.

Dependence on the Index Modulation and Power Angle the storage of energy requirements in (41) depend on the voltage limit defined by kmax, the frequency line ω1, the modulation index m and the power angle ϕ. However, as the energy variations are inversely proportional to the line frequency this means that ΔEmax and thus also the energy storage requirements are inversely comparative to the frequency line. Accordingly, the energy storage requirements for different line frequencies can effortlessly analyzed and no need of supplementary analysis. Therefore, it will, hereafter, be assumed that the line frequency is always 45 Hz.

5. RESULTS AND SIMULATION

The proposed converter was fabricated with IBM 130-nmCMOS process. The chip microphotograph is with a chip area of 1 mm (1 mm 1 mm). Because the foundry mandatorily requires each die to be covered by a layer of top metal for pattern density checks, the details of the chip are unobservable. It demonstrates the floor plan. The input is designed at 1.5 V, but can vary between 0.9 and 1.8 V. The output voltage of the converter can be regulated from0.9 to 2.2 V with a maximum load power of 400 mW. Here, measured the steady-state regulation of the proposed converter at (a) pseudo-buck mode, (b) pseudo-boost mode and (c) transition mode. A nominal value of 10 MHz, the switching frequency of the converter can reach to 20 MHz.

The inductor and output filtering capacitor is designed at 1 H and 1 F, respectively, for high switching frequency operation. The steady-state regulation of the converter is in three operation modes. With 1.5-V and 10-MHz, is regulated at1.2 V, 1.8 V, and 1.5 V, in the pseudo-buck, pseudo-boost, and transition modes, respectively.

The proposed GM operation controller can automatically reconfigure the converter topology based on and, so that the most efficient regulation can be achieved. For the down-tracking, a 16- settling time is observed, which gives a 26.7- down-tracking speed. For the up-tracking, it needs 56 for to settle, resulting in a 93.3- up-tracking speed. The relatively control scheme. Is depends on changes from 1.2 to 1.8 V, the converter switches from pseudo-buck to pseudo-boost mode. At pseudo-boost mode, information is required to assist the single-bound voltage regulation. As a consequence, certain processing delay is required. Fig. 5 shows the DC response of the system.

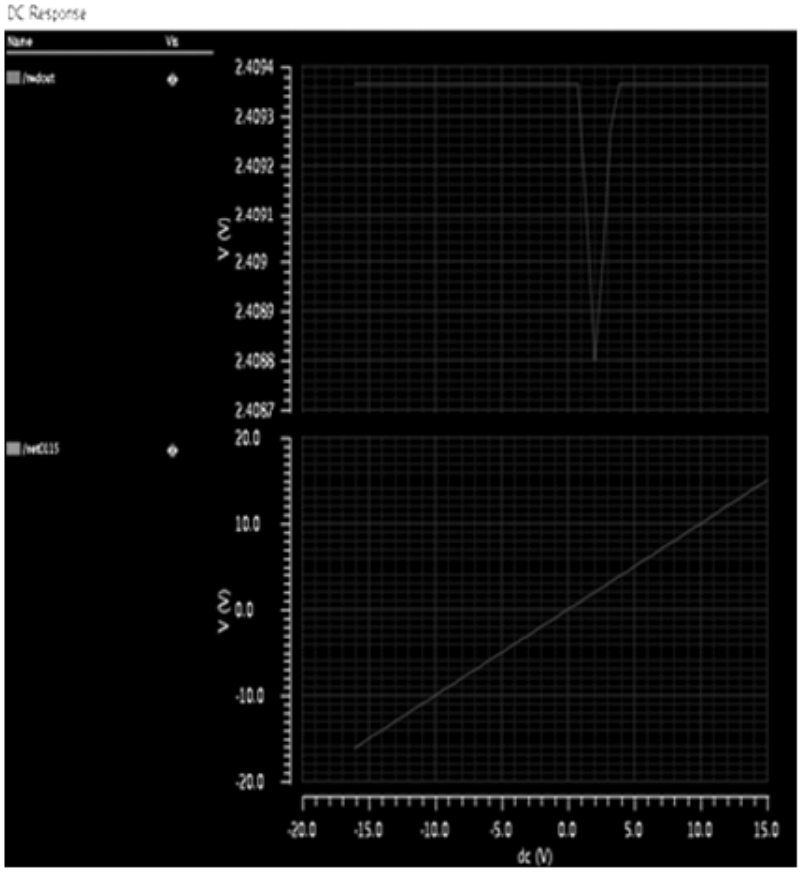

Figure 5: DC Response

On the other hand, when changes from 1.8 to 1.2 V, the converter is reconfigured from pseudo-boost to pseudo-buck mode. At pseudo-buck mode, only is sufficient for closed-loop regulation. Therefore, a faster down-tracking speed is observed. With regulated at 0.9 and 1.2 V in the pseudo-buck mode and1.8 and 2.1 V in the pseudo-boost mode, respectively.

As increases from 0.9 to 1.8 V with 100-mV step changes, the line regulation of the converter is maintained below 0.8%, and a lowest value of 0.17% is measured at 1.1-V and 0.9-V. With the proposed adaptive frequency compensator, is regulated between 9.74 and 10.27 MHz, and the deviations from the 10-MHz target frequency are within 3%.area, with a maximum static power dissipation of 227 W.

The input voltage range of the proposed circuit is designed from 0.9to 2.5 V. The ASM circuit is fixed at 1.8 V, while is swept periodically from 0.9 to 2.5V as a triangular waveform. The ASM can adaptively switch the output to the higher voltage level between two inputs, with a switching delay of 350 ns. Now varies as a square waveform from 0.9 to 2.5 V, while is still fixed at 1.8 V. As a result, a switching speed of 800 mV/180 ns4.44 mV/ns is observed, which is fast enough to survive most of the variable-output power supplies.

In addition, the tracking error, which represents the deviation between the output of ASM and the ideal value, is below 5 mVin steady state, allowing accurate substrate biasing for PMOS power transistors. The efficiencies measured of the converter at pseudo-buck, pseudo-boost and transition operation modes. With a 10-MHz switching frequency and 1.5-V input supply, a maximum efficiency of 92.1% is measured at 1.2-Voutput voltage and 250-mW load power.

Due to the employment of the proposed GM and APTS schemes, the efficiencies in pseudo-buck and pseudo-boost modes see obvious improvements, compared to conventional non-inverting buck-boost converter with the same load condition. Even during the transition mode, the APTS scheme continues to

contribute a noticeable efficiency enhancement. Overall, the efficiency of the converter stays above 80% over the interested 400-mWpower range. Below table shows the variations compared to the existing method.

5.1. Analysis using an Analog Design Environment

In this paper, some assumption have been initiate and permit a model to obtain that is almost sufficient and is not supplementary make challenging than important for the DVS converter. A structure of control with a dimension moderate and difficulty should be enhanced. So, a robustness study is achieved with an additional actual model of DVS. Also, it was estimated every transistors are demonstrated as aperfect resistance once they are on switched. Now, it is complicated that the transistor models are collected by a conflict and a capacitance, in order to model the properties of dissipative and the switching periods of the transistors PMOS.

Furthermore, the transistors require many features of electrical. Likewise, it is processed that the sensor that processes the modeled core voltage as a filter of low-pass. The waveforms of steady-state emphasize the excessive advantage of the four-phase FIBC from the point vision of current ripple. As input of converter, 22-A inductors current ripple to 3 A. By using a second-order filter of low-pass, nearly zero is occur in the FC current ripple.

The signal of steady-state driving switch is with 70% of duty cycle and 90° out of stage from every other are shown in Fig. 6. Fig. 7 shows analytical and experimental of four-phase FIBC proficiency curves,

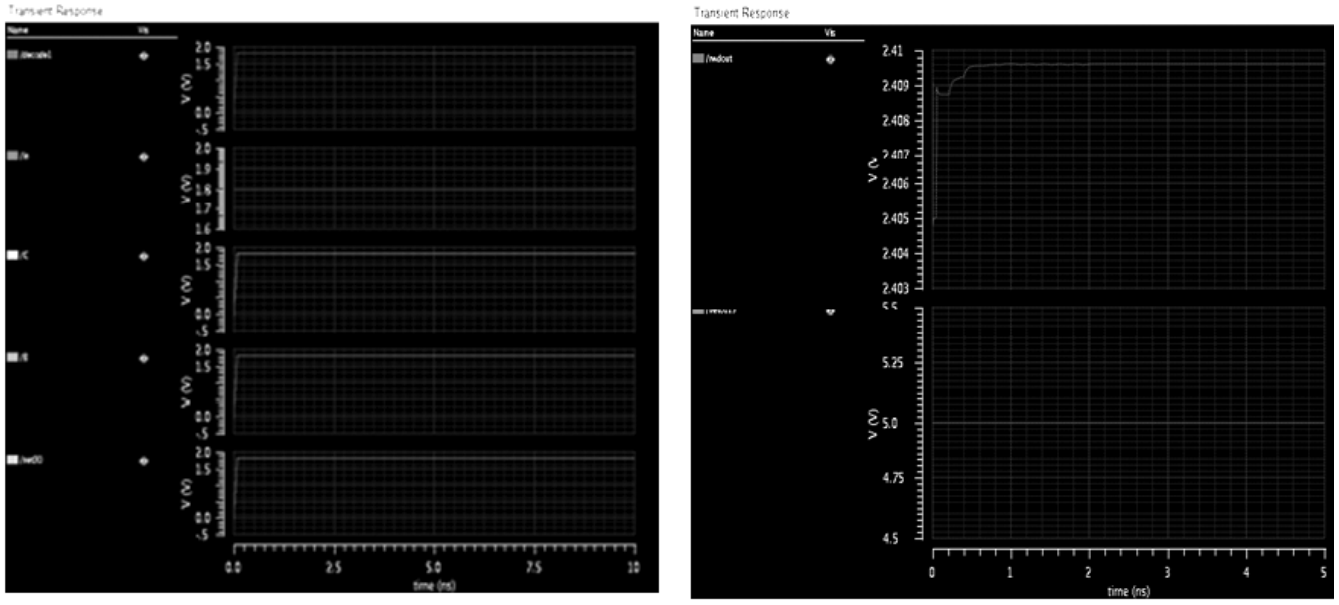

Figure 6: Transient Response of steady-state switches driving signals and phase outcome FIBC efficiency

Table 1
Comparison of existing and proposed approach

	[1]	[18]	Design	MSCV	RCED	PROPOSED
Supply voltage	3-4.51	3.31	2.01	2.01	1.81	1.81
Output voltage	5.01	4.5-5.01	1.126	2.0	0.896	0.751
Maximum output current	25.0	30.0	19.0	8.0	15.0	8.0
Power Efficiency %	77-81.71	70.751	80-851	80-851	85-901	801
Area (mm^2)	0.231	0.251	0.201	0.161	0.121	0.121
Technology	0.50	0.13	180nm	180nm	180nm	180nm
Control unit	Digital	Analog	Digital	Analog	Analog	Analog

which designate that the converter execution has a 95% of maximum efficiency at a demand of power 2.5 kW. Also, 94.7% efficiency is at a demand of power 5 kW. This specifies that the controller proposed has outstanding dynamic outcome. Similarly the proposed controller sliding has identical better response of steady-state with insignificant error of steady-state around 17.5A.

The dynamic reply of the controller sliding-mode for a stage difference of current inductor is from 13 to 20. Four-phase FIBC converter and Test bench are executed and the currents effortlessly track the reference signal. It is done with a 0.8 ms settling time and with no ringing noticeable or exceed. Such effectiveness is exact better for less power voltage of intensive current and greatly higher than an corresponding traditional converter of dc-dc boost for the similar application.

6. CONCLUSION

An integrated power converter with a reconfigurable power stage and an adaptive gain-pulse control has been presented with the high gain and high modulation of the device configuration. The novel power stage, which employs interleaving regulation scheme with multiple-phase GR reconfiguration, this made the system to be more efficient compared to the existing methods and throughput along with the supply voltages presented made the system area complexity a reduced manner with the high significant natural sequence.

This be implemented using a Cadence Virtuoso tool in 180nm CMOS process in an Analog Design Environment. It also reduces input current and output voltage ripples and improves the system bandwidth. It allows the converter to flexibly provide either step-up or step-down voltage conversion. The design provides an effective solution to ever-increasing self-powered energy-efficient applications.

REFERENCE

[1] Hing-Kit Kwan, David C. W. Ng, and Victor W. K. So, “Design and Analysis of Dual-Mode Digital-Control NStep-Up Switched-Capacitor Power Converter With Pulse-Skipping and Numerically Controlled Oscillator-Based Frequency Modulation”, IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 21, No. 11, November 2013 ,pp : 2132-2140

[2] Ben-Sheng Chen and Yuan-Yih Hsu,” A Minimal Harmonic Controller for a STATCOM,” IEEE Transactions On Industrial Electronics, Vol. 55, No. 2, February 2008, PP:655-664.

[3] Yasser Abdel-Rady Ibrahim Mohamed and Ehab F. El-Saadany,” A Control Scheme for PWM Voltage-Source Distributed-Generation Inverters for Fast Load-Voltage Regulation and Effective Mitigation of Unbalanced Voltage Disturbances”, IEEE Transactions On Industrial Electronics, Vol. 55, No. 5, May 2008, PP 2072-2084.

[4] Salman Mohagheghi, Ganesh K. Venayagamoorthy and Ronald G. Harley,” Optimal Wide Area Controller and State Predictor for a Power System,” IEEE Transactions On Power Systems, Vol. 22, No. 2, May 2007, PP 693-705

[5] Heng-Yi Li and Hung-Chi Chen,” Dynamic Modeling and Controller Design for a Single-Stage Single-Switch Parallel Boost-Flyback–Flyback Converter,” IEEE Transactions On Power Electronics, Vol. 27, No. 2, February 2012,PP 816-827.

[6] Ramesh Giri, Vijay Choudhary, Raja Ayyanar, and Ned Mohan, “Common-Duty-Ratio Control of Input-Series Connected Modular DC–DC Converters With Active Input Voltage and Load-Current Sharing ,” IEEE Transactions On Industry Applications, Vol. 42, No. 4, July/August 2006, PP 1101-1111.

[7] Yu Liu, Alex Q. Huang, Wenchao Song Subhashish Bhattacharya and Guojun Tan, “Small-Signal Model-Based Control Strategy for Balancing Individual DC Capacitor Voltages in Cascade Multilevel Inverter-Based STATCOM,” IEEE Transactions On Industrial Electronics, Vol. 56, No. 6, June 2009,PP 2259-2269.

[8] SandeepAnand, B. G. Fernandes, and Kishore Chatterjee, “DC Voltage Controller for Asymmetric-Twin-Converter-Topology-Based High-Power,” IEEE Transactions On Industrial Electronics, Vol. 60, No. 1, January 2013, pp. 11-19.

[9] Adel Gastli, and Mohamed Magdy Ahmed,” ANN-Based Soft Starting of Voltage-Controlled-Fed IM Drive System,” IEEE Transactions On Energy Conversion, Vol. 20, No. 3, September 2005, PP 497-503.

[10] B. R. Gregoire, “A compact switched-capacitor regulated charge pump power supply,” IEEE J. Solid-State Circuits, vol. 41, no. 8, pp. 1944–1953, Aug. 2006.

[11] L. Su, D. Ma, and A. P. Brokaw, “Design and analysis of monolithic step-down switched-capacitor power converter with subthreshold DPWM control for self-powered wireless sensors,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 1, pp. 280–290, Jan. 2010.

[12] T. V. Breussegem and M. Steyaert, “A 82% efûciency 0.5% ripple 16- phase fully integrated capacitive voltage doubler,” in Proc. IEEE Symp. Very Large Scale Integr. Circuits, Jun. 2009, pp. 198–199.

[13] W. Evans, J. P. Kawamura, and J. L. Krug, “Soft-start control for DC/DC switching regulators,” U.S. Patent 6 515 880 B1, Feb. 2003.

[14] M. Yang, X. Ruan, and M. Xu, “Soft start strategy for bi-directional DC/DC converter,” inProc. IEEE Power Electron. Spec. Conf., Jun. 2007, pp. 161–164.

[15] L. Ni, D. J. Patterson, and J. L. Hudgins, “High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application,” IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1141–1151, Mar. 2012.

[16] S. Bandyopadhyay, Y. K. Ramada s, and A. P. Chandrakasan, “20 mA to 100 mA DC-DC converter with 2.8 to 4.2 V battery supply for portable applications in 45 nm CMOS,” in Proc. IEEE ISSCC Dig. Tech. Papers,Feb. 2011, pp. 386–387.

[17] V. Ivanov, “Design methodology and circuit techniques for any-load stable LDOs with instant load regulation and low noise,” inAnalog Circuit Design, A. H. M. van Roermund, H. Casier, and M. Steyaert, Eds. New York, USA: Springer Science and Business Media, 2009, pp. 339–358.

[18] J.-Y. Lee, S.-E. Song, J.-K. Kim, S. Kim, and H.-J. Yoo, “A regulated charge pump with small ripple voltage and fast start-up,” IEEE J. Solid-State Circuits, vol. 41, no. 2,Feb. 2006. pp. 425–43