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All Optical Reversible Counters

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ABSTRACT

As Reversible Logic possess low power consumption and less heat dissipation, It is drags a interest among the researchers. A number of reversible gates have been proposed by different researchers and various combinational circuits based on reversible gates have been proposed. In this Scenario, Many researchers did not concentrating on Sequential circuits because of its feedback. In this work, we propose two novel reversible gates and using that we have designed Reversible D Flipflop and Reversible T Flipflop. The proposed counters has a better improvement over earlier design in the reversible literature in terms of garbage outputs, constant inputs and number of reversible gates. The Proposed work is also implemented optically and the simulation is verified using the Optisim Software.

Key Words: Reversible T Flipflop, Reversible D Flipflop

1. INTRODUCTION

Huge amount of heat is dissipated ,when we dump more logic elements into smaller stack of volumes and clock them at greater frequencies,. When a conventional system erases a bit of information, it would dissipate ln2*kT energy, where 'k' Boltzman constant and 'T' temperature in Kelvin[1]. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennett, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2]. The current conventional system deploys a bit of information everytime they perform logical operation. These logic operations are termed as irreversible. An alternative is to use logic operations that do not erase information is reversible logic operation, basically it dissipates heat in smaller amount as the energy dissipated per irreversible operation approaches the fundamental limit of ln2*kT, use of reversible operations is likely to become more attractive. Achieving a perfect reversible logic system is very difficult. As nothing is hundred percent perfect, reversible logic gates also dissipates less heat and little bit complex.

2. REVERSIBLE LOGIC CIRCUITS

Reversible circuits are do not lose information and reversible computation in a system can beperformed only when the system comprises of reversible gates[5]. These circuits can generate unique output vector fromeach input vector, and vice versa, that is, there is a one-to-one correspondance between input and output vectors. A gate is reversible if the gate's inputs and outputs have a one-to-one correspondence, i.e. there is a distinct output assignment foreach distinct input. The conventionallogic gates such as AND, OR, and X-OR are irreversible, as they are all multiple-input single output logic gates. A NOT Gate is said to be reversible Reversible logic supports the process ofrunning the system both forward and backward direction. This means that reversible computations can generate inputs fromoutputs, may stop and go back to any point in the computing history. Thus, reversible logic circuits offer an alternative thatallows computation

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with arbitrarily small energy dissipation. A reversible logic circuit should have features of using minimum number of reversible gates, Garbage outputs and constant inputs.

In reversible logic there exists a unique one to one mapping between the input and output vectors. Garbage outputs are the unused outputs are used to maintain the reversibility of a reversible circuits [4]. Fan-out and loops are not permitted[3]**.** The multiple output Boolean function $F(x_1; x_2; :::; x_n)$ of n Boolean variables is called reversible if the number of outputs are equal to the number of inputs.In other words, reversible functions are those that perform permutations of the set of input vectors.

3. SOA BASED MZI

A photon can provide matchless high speed and can store the information in a signal of zero mass. These properties of photon have attracted the attention of researchers to implement the reversible logic gates in all optical domain. The all optical implementation of reversible logic gates could be useful to overcome the limits constraine by conventional computing, and is also considered as implementation platform for quantum computing . Semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI) optical switches used to achieve the all optical implementation of reversible logic gates [6]. The Mach-Zehnder interferometer based implementation of reversible logic gates provides significant advantages such as high speed, low power, fast switching time, and ease in the fabrication.

A MZI based all optical switch can be designed by using two Semiconductor optical amplifier (SOA-1, SOA-2) and two couplers (C-1, C-2). In MZI there are two inputs ports are called incoming signal and control signal and two output ports are called as bar port and cross port.. The block diagram of MZI based all optical switch is shown in Fig. 3.2.

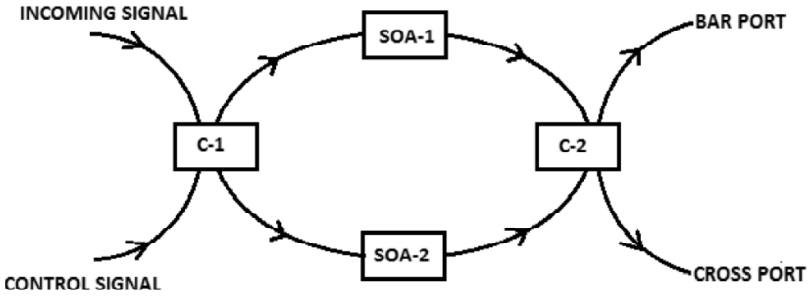


Figure 3.2: SOA Based MZ1

4. PROPOSED WORK

4.1. Reversible T Gate

The proposed T Gate is the 4*4 Reversible Gate. The inputs are A,B,C and D , the outputs are P,Q,R and S respectively. The reversible T gate is used to design Sequential Circuit. The outputs of the proposed T gate is shown in figure 4.1.

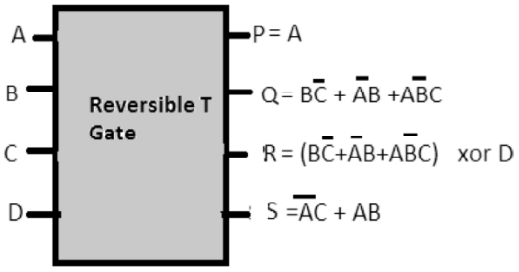


Figure 4.1: Block Diagram of proposed T Gate

Truth table of T Gate

In the conventional Gates the outputs can be repeated. We cannot track the output from the input. Thus it is called as the Irreversible in nature. The conventional NOT Gate is Reversible. The truth table that is tabulated clearly explains that the proposed Reversible T Gate is one to one mapped. The output never gets repeated. Thus it ensures the Security. This is the reason that the proposed gate is Reversible. We also can track the input from the output which is the beauty of reversible computing.

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	0	1	1	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	1

4.2: Truth Table of proposed T Gate

Modelsim Output of the T Gate

We also had verified the proposed Reversible T Gate output in the modelsim software through the Verilog code. The Output screenshot is shown in the figure.

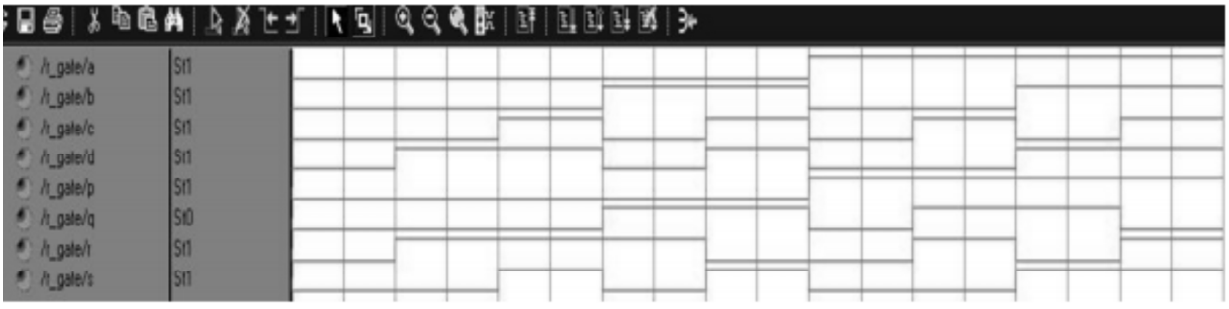


Figure 4.3: Modelsim Output of proposed T Gate

Construction of T Flipflop using T Gate

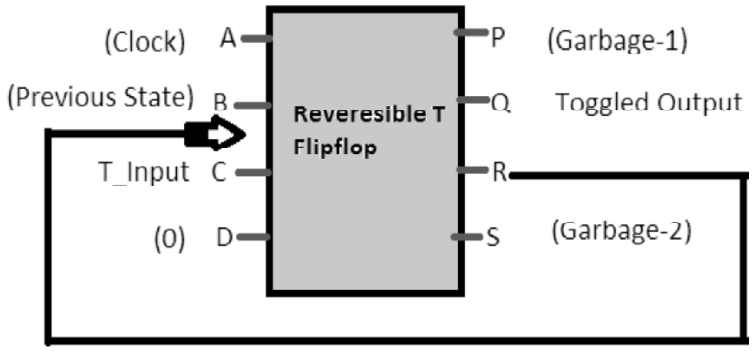
The operations of the T-flipflop are as shown in the table.The expressions can be obtained by drawing the Karnaugh map for the Output port.

The truth table of the T Flipflop is given below

T INPUT	PREVIOUS STATE	CLOCK	OUTPUT
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

4.4: Truth Table of TFlipflop

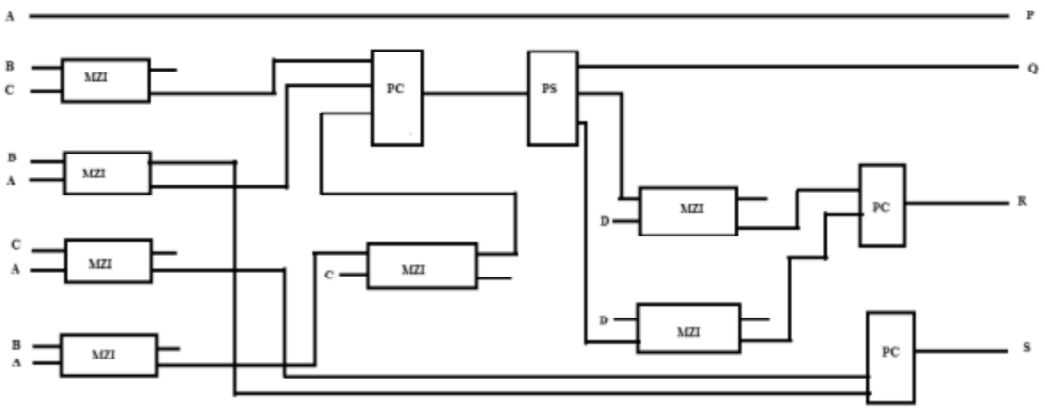
We can design the T Flipflop using the proposed T Reversible Gate and it is shown in the figure. The P output is directly taken from the Input port A. The Q output is Exclusively OR with the D input in order to get the previous state as output in R port which is set as the input in B terminal. Here P and R are considered as the garbage output.



4.4: Block Diagram of proposed T Flipflop Using T Gate

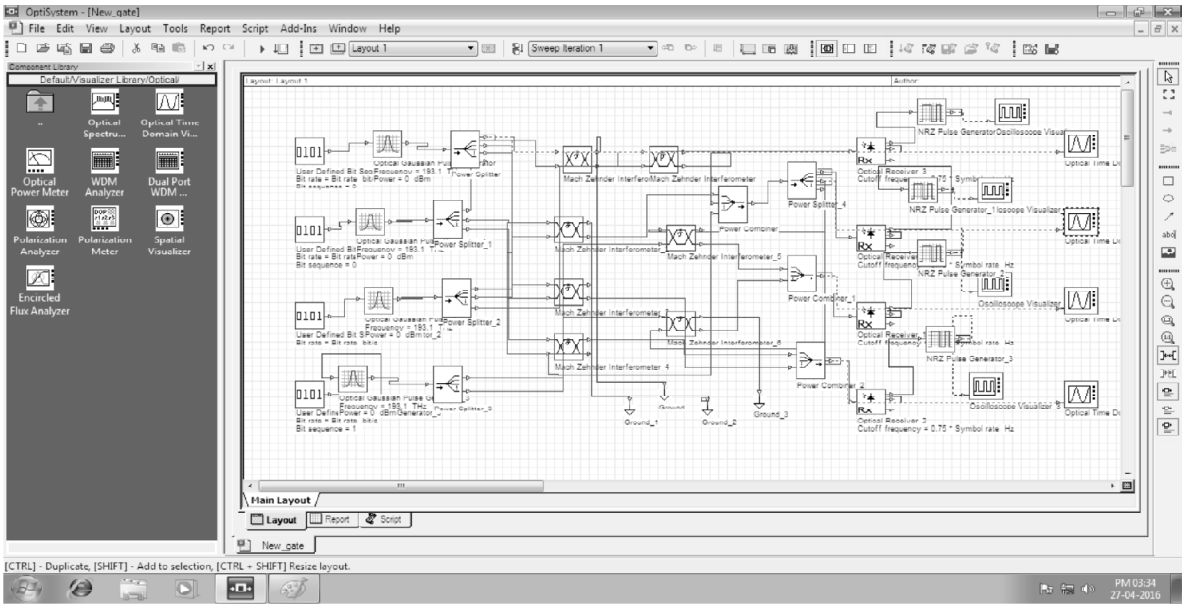
Optical Implementation of the T Gate

The proposed T Gate is optically implemented as shown in the figure 4.5. It uses the Mach Zehnder Interferometer, Beam Splitter, Beam Combiner , Non Return to Zero pulse code generator. Beam Combiner is used to combine the optical signal and the Beam Combine splitter is used split the optical signal. MZI is the ultrafast optical switch, which switches according to the optical implementation circuit.



4.5: Optical Implementation of proposed T Gate

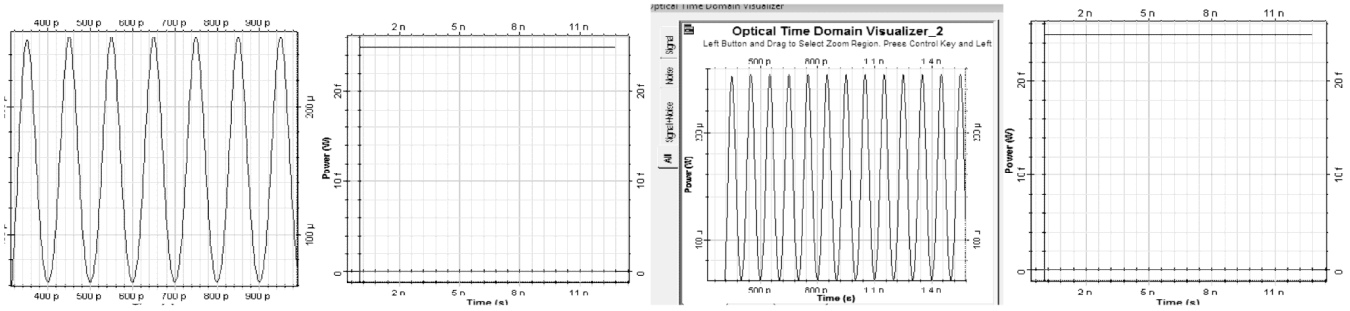
The same circuit is verified in theOptisim Software and the simulation screenshots are shown in the figure 4.7.



4.6: Simuation of T Gate using Optisim

Screenshots of the Output of the T Gate in Optisystem Software

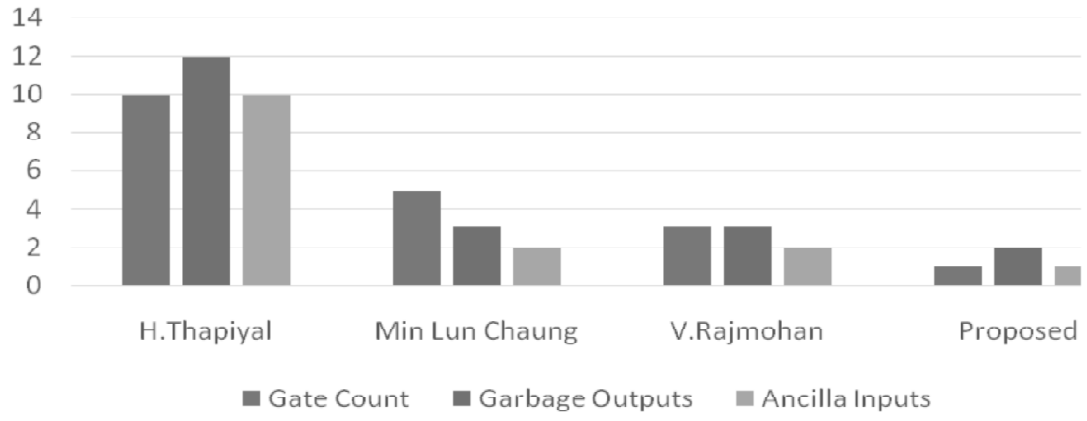
When the Input is A=1,B=0,C=0,D=1 then the output is, 1010



4.7: Optisim results of the proposed T Gate

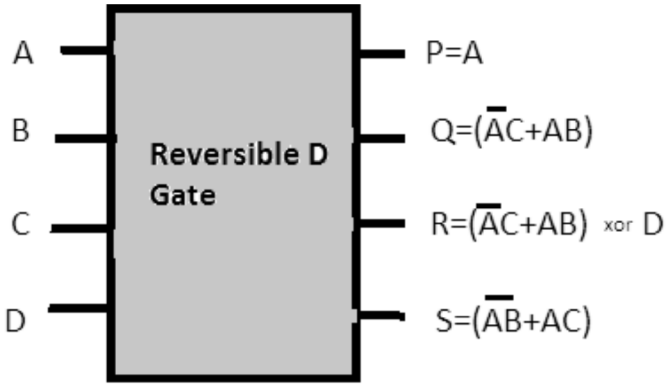
Comparison between the Existing Reversible T Flipflops

It is shown that the proposed reversible T Flipflop is better than the existing T Flipflops.[8,9,10]



5. PROPOSED D GATE

The proposed D Gate is the 4*4 Reversible Gate .The inputs are A,B,C and D , the outputs are P,Q,R and S respectively. The reversible D Gate is used to design sequential Circuit. The outputs of the D gates are shown in block diagram 5.1.



5.1: Block Diagram of proposed D Gate

Truth table of D Gate

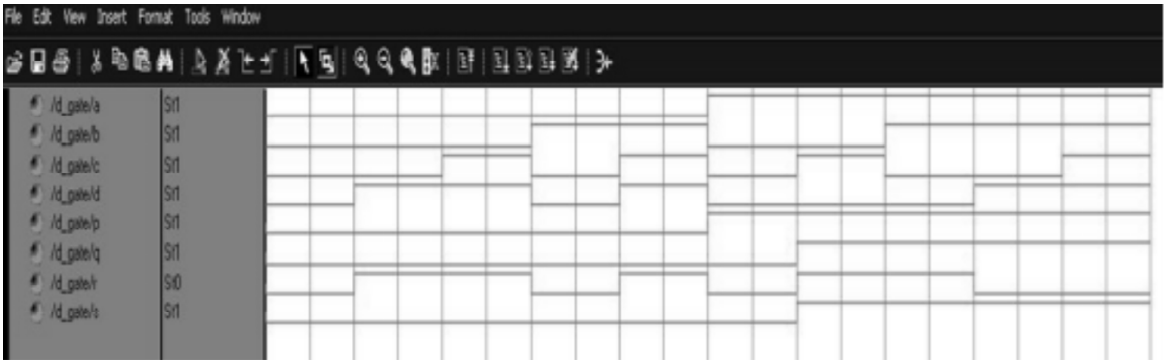
The truth table that is tabulated clearly explains that the proposed Reversible D Gate is one to one mapped. The output never gets repeated. Thus it ensures the Security.

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	1
0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0
0	1	1	0	0	1	1	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	1	0	0	1
1	0	1	1	1	0	1	1
1	1	0	0	1	1	1	0
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1

5.2: Block Diagram of proposed D Gate

Modelsim Output of the Proposed D Gate

We also had verified the proposed Reversible D Gate Output in the modelsim software through the Verilog Code.The Output Screenshot is shown in the figure 5.3



5.3: Modelsim Output of proposed D Gate

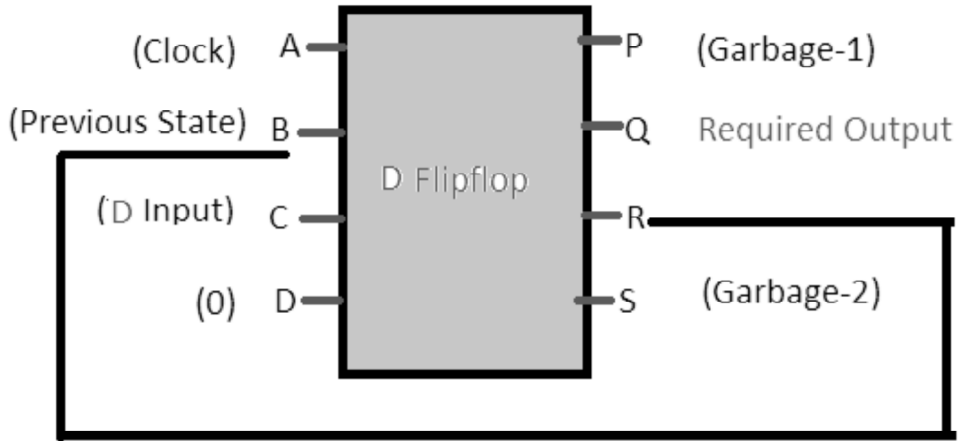
Construction of D Flipflop using D Gate

The operations of the D-flipflop are as shown in the table.The expressions can be obtained by drawing the Karnaugh map for the Output port. The truth table of the D Flipflop is given below.

Clk	D	Previous State	OP
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

5.4: Block Diagram of proposed DTruth Table of D Flipflop

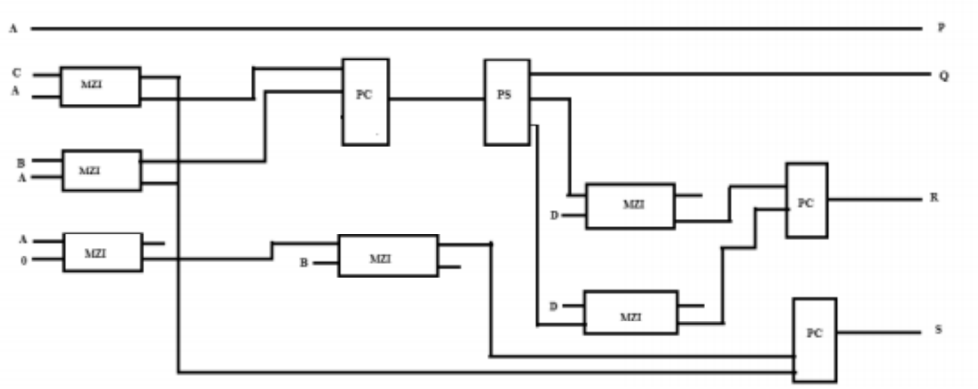
We can design the D Flipflop using the proposed D Reversible Gate and it is shown in the figure 8.3 .The P output is directly taken from the Input port A. The Q output is Exclusively OR with the D input in order to get the previous state as input. Here P and R are considered as the unwanted Output that is garbage output as shown in the figure 5.5.



5.5: Block Diagram of proposed D Flipflop using D Gate

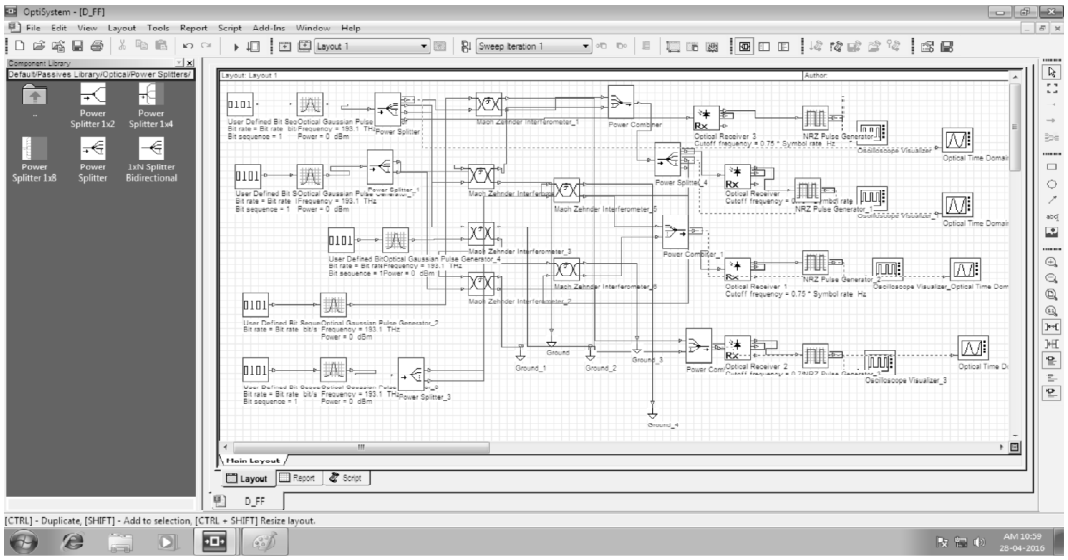
Optical Implementation of the Reversible D Gate

The proposed T Gate is optically implemented as shown in the It uses the Mach Zehnder Interferometer, Beam Splitter, Beam Combiner, Non Return to Zero pulse code generator. MZI is the ultrafast optical switch, which switches according to the optical implementation circuit given below.



5.6: Optical Implementation of the proposed D Gate

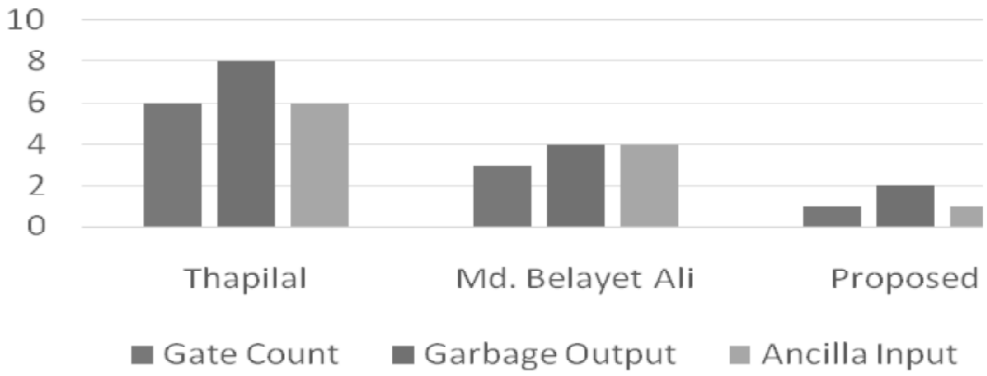
The same circuit is implemented in the Optisystem software.



5.6: Optisim Simulation of the proposed D Gate

Comparison between the Existing Reversible D Flipflops

It is shown that the proposed reversible D Flipflop is better than the existing D Flipflops. [8,11]

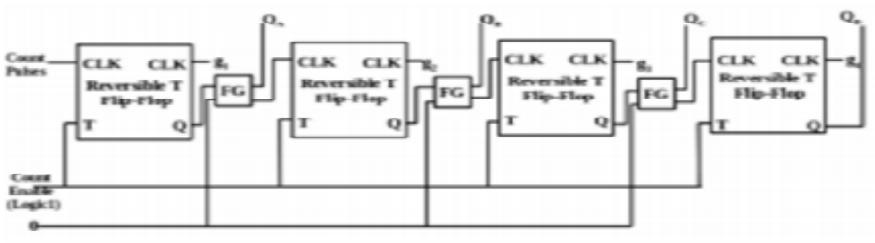


6. IMPLEMENTATION OF REVERSIBLE COUNTERS USING PROPOSED REVERSIBLE D AND T FLIPFLOP

Counters are a specific type of sequential circuits. Like registers, the state or the flip flop values themselves serves as a output.

Reversible Asynchronous Up Counters

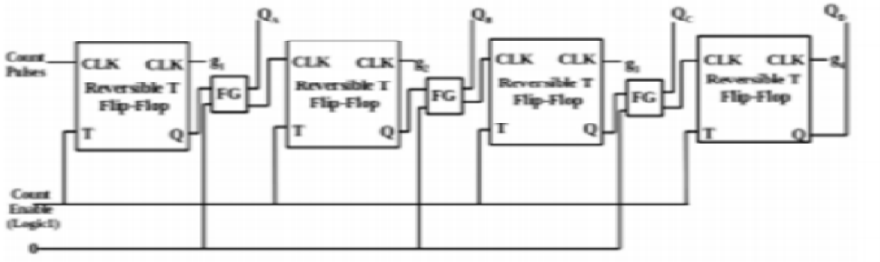
In asynchronous counters, the triggering of next flip flop is taken from the output transition from previous flip flop .The reversible design of the 4-bit asynchronous UP-Counter is shown in figure 6.1.Feynman Gate is used to take the complementary output from the flipflop in Up counter ,the control input of the Feynman gate is1.



6.1: Reversible Asynchronous Up Counter using the proposed Reversible T Flipflop

Reversible Asynchronous Down Counter

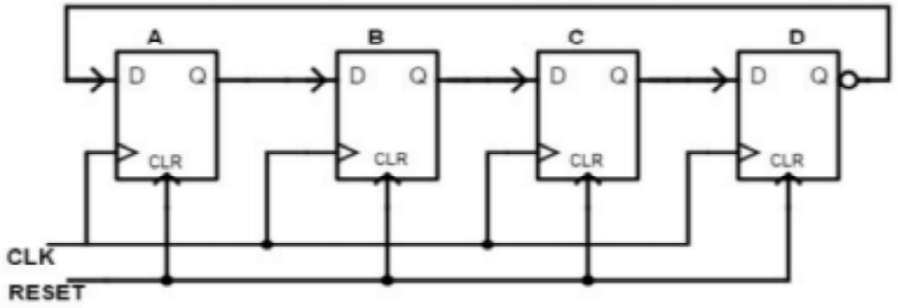
The reversible design of the above 4-bit asynchronous Down Counter is shown in the figure 6.2. Feynman Gate is used for triggering the next flip flop in down counter, the control input of the Feynman gate is 0.



6.2: Reversible Asynchronous down counter using the proposed Reversible T Flipflop

Reversible Ring Counter

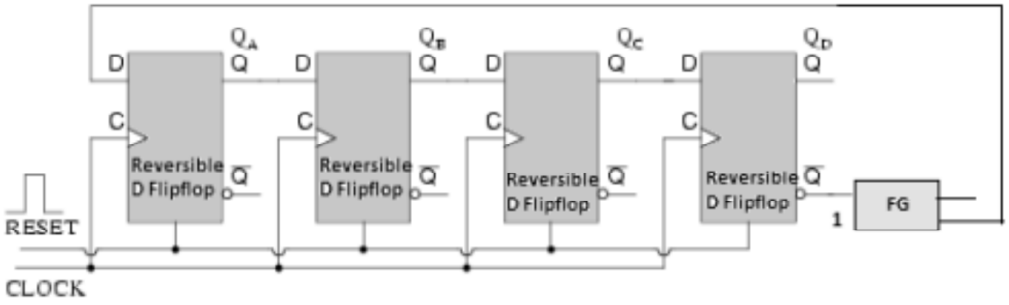
The ring counter is a cascaded connection of flip flops, in which the output of last flip flop is connected to input of first flip flop. Ring counters are implemented using shift registers. It is essentially a circulating shift register connected so that the last flip-flop shifts its value into the first flip-flop. There is usually only a single 1 circulating in the register, as long as clock pulses are applied. (Starts 1000->0100->0010->0001 repeat) [7]. The circuit diagram of the reversible ring counter is shown in the below figure



6.3: Reversible Ring Counter using the proposed Reversible D Flipflop

Reversible Johnson Counters

The switch-tail ring counter also know as the Johnson counter, overcomes some of the limitations of the ring counter. Like a ring counter a Johnson counter is a shift register fed back on itself. It requires half the stages of a comparable ring counter for a given division ratio. [7]

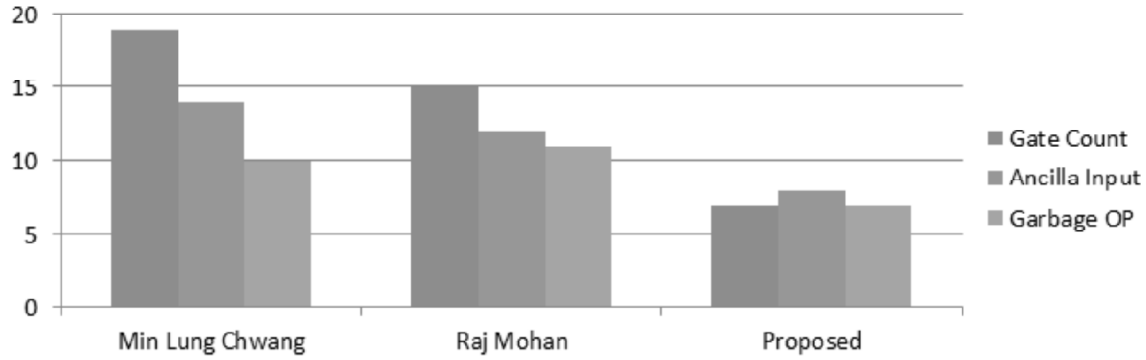


6.4: Reversible Johnson Counter using the proposed Reversible D Flipflop

If the complement output of a ring counter is fed back to the input instead of the true output, a Johnson counter results. This is the difference between a ring counter and a Johnson counter.We don't have the Q Bar Output in the proposed T & D Flipflop using T & D Gate.As we need the Q'port for fewer counters, We are adding the feynmen gate (Reversible) from which we can get the Q complement Output..

7. COMPARISON BETWEEN EXISTING COUNTERS

The comparison of the proposed design with the existing in the terms of Gate count, number of Ancilla inputs,Garbage outputs. It is proved that the designed architecture is better in the Reversible Literature [9,11] as shown below.



8. CONCLUSION

In this work, we propose a novel reversible gate which has shown the significant improvement for realizing and optimizing T and D Flipflop. We also propose the designs of reversible asynchronous Up and asynchronous down counter using reversible T flip-flop, Feynman Gate. The designs of the counters are compared with existing counter design for three parameters namely gate count, garbage output, constant inputs and found better.

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