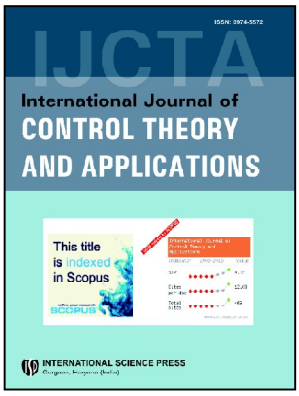

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Implementation of High Speed Volatile and Non Volatile Memory Structures for Video Application Using SoC Encounter

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Abstract: Memory Structure is the important area, where extreme care will be taken while designing system for the application area of ASIC and FPGA implementations. The internal structure of the memory depends on a dedicated application area. The traditional memory structure which are using previously will have one address and single data output for Non Volatile memory (NVM) or other designs will have independent address lines both for read and write operations, while data bus will work as dual direction port which is defined as Volatile Memory (VM). In practical system i.e., Moving Picture Expert Group (MPEG) where real time constraints are required because in these systems they follow traditional way of construction of memory design i.e., to access two different operations (write row-wise/ read column wise) parallel. All the VM and NVM structures are coded using Verilog HDL language and simulated using RTL Compiler and synthesized by using SoC Encounter for 45nm GPDK technology libraries.

Keywords: Single address VM, Dual Address NVM, Dual Port VM, RTL Compiler, SoC Encounter.

1. INTRODUCTION

In the operating system memory management subsystem [2] plays a very prominent role. Day by Day there has been more need for memory than that exists in the system. Strategies have been developed to surmount this restraint and the most successful of these is virtual memory. Virtual Memory makes the system emerge to have more memory than it actually has by allotting it between competing processes as they need it.

2. DESIGN DESCRIPTION

On Board Dual Address NVM Design

Let us consider a Video application, in which the system NVM is required to supply multiple data's parallely. The NVM is here designed to have multiple addresses at transmitter side and multiple data output at receiver side. This application which requires synchronous pipelined operation in order to achieve rapid processing speeds and clock has been used. Multiple addresses are provided fetch the multiple locations parallely. The bit length in the address bus will choose the location length or size in the NVM. Here 3 bits are provided for address,

therefore NVM has 8 locations and data width size of 64 bits. The data which is read from the NVM look up table are named as dout1 and dout2 which are corresponding to the respective addresses a1 and a2 respectively as shown in figure 1. The NVM content is only a block with the size of 8*64 bits even though multiple addresses are part of the design. The kind of necessities arises in specified applications like discrete cosine transformation and quantization processor used in Moving Picture Expert Group1, Moving Picture Expert Group2 base constant image/moving picture compression codecs.

Figure 1: Design of On Chip Dual address NVM

On Board Single Address NVM Design

The NVM as shown in figure 2, which has a one address at transmitter side and one data output at receiver side, which is used to save converse quantization parameters. In quantization process, we need to split the Discrete Cosine Transform Quantization coefficients [6] by the corresponding quantization parameters. On the other hand, division can also be implemented as multiplication by taking the inversion of quantization parameters. Therefore, store the converse of the quantization parameters in the NVM. The size of data look up table is 64 bits. While reading the NVM, only one byte is retrieved at a time. Therefore, this kind of implementation differs from the conventional way of approach which stores the data or addresses in the form of byte-wise. For an example 256*8 bits i.e., 28*10 bits, in this 8 bits are used for address. The NVM specification may be as follows:

The NVM contains the converse of the quantization parameters (i.e., 10 bits length, unsigned). It is structured as 10*256 bits, and can be read by byte-wise.

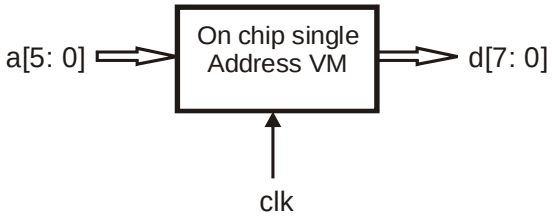

Figure 2: Design of on Chip Single Address NVM

On Board Dual Address VM Design

The prerequisite of dual VM [4] with a meticulous memory structure as represented in this fragment comes from the requirements of the design applications such as Discrete Cosine Transform Quantization, which was discussed in the VM designs. The dual port VM has two VM's which consists of image pixels data. This data will be written from a master or transmitter (computer) such as a personal computer into one of the VM through peripheral connects interface (PCI) bus. At first, one of the dual memory buffers, VM1 is filled and once it is full, the image data is once again written back to the second VM. While the VM2 is being written into, the VM1 will be read parallely to process the Discrete Cosine Transform Quantization coefficients. The most imperative design feature in this design is that the data is written at the rate of 256 bits per clock cycle. The data transfer is by the PCI interface with 256 bits data bus. To process Discrete Cosine Transform Quantization, we need to write a block of images data consisting of 256 pixels. One pixel data capacity is one byte for monochrome and three bytes for color picture. This design is for processing monochrome picture or color picture. Pin diagram for the dual VM is

shown in figure 3. The validity of the input data signals, di [255:0] is generated by 'din_valid'. As well, the validity of each of the 10bits in the 256 bit of data bus is indicated by the 'be [9:0]' pin referred to as the byte enable signal. In order to write a pixel block, we need only 5 bits address, 'wa [4:0]', corresponding to ten locations, each location being 256 bits in width. Data is at the positive edge of 'pci_clk' signal.

Signal,'rnw', is read negative (low) and write positive (high), is used to organize one of the VM in write mode while the other VM block is support in the read mode. In this manner parallel processing of both writing and reading of the double buffer is achieved. The vM1 and VM2 are automatically configured to the write mode only and vice versa. The VM is written row – wise and read column – wise. This is because of intricacy of the Discrete Cosine Transform Quantization reckoned at the rising edge of 'clk' signal. In this column – wise data read appears at the output, 'd0 [63:0]'.

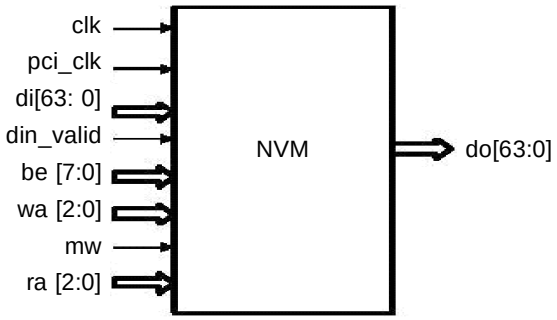

Figure 3: Design of on Chip Dual Port VM

3. BACKEND PROCESS PLACEMENT

The Placing and routing were performed by using SoC Encounter tools [5] for the 45nm technology GPDK libraries to obtain the layout structure for the device and it takes 70% of core utilization. The pads (GND, VDD) will be surrounded by the core in all the four directions (top, bottom, left, right) with subsequent width and length. The placement of dual port NVM is shown as in figure 4.

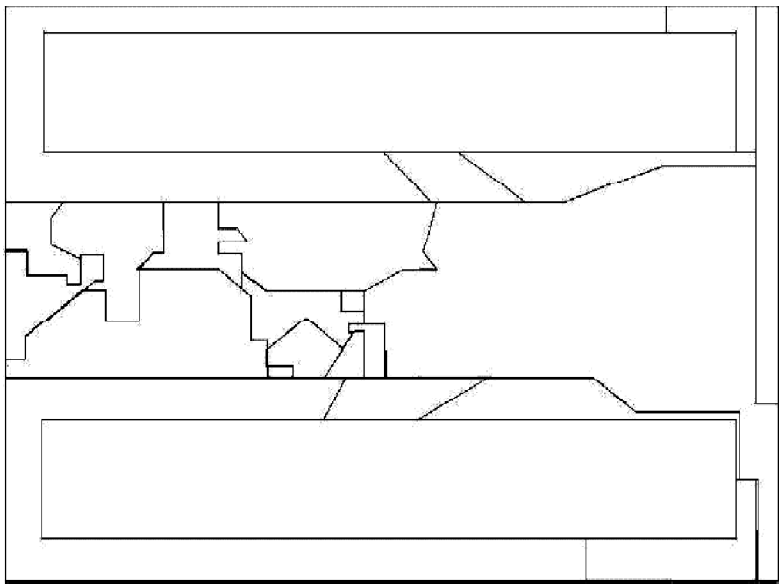

Figure 4: Placement of on Chip Dual Port NVM

4. IMPLEMENTATION RESULT

Every block is implemented by using ASIC Cadence SoC Encounter [3] tool with 45nm technology libraries. Figure 5 shows RTL Schematic of Dual address NVM, Figure 6 shows RTL Schematic of dual port VM, Table 1 gives the post clock tree synthesis report of dual port VM when it performs routing and finally figure 7 & 8 shows the IC chip fabrication layout structure of dual address NVM and dual port VM which is named as GDS II file.

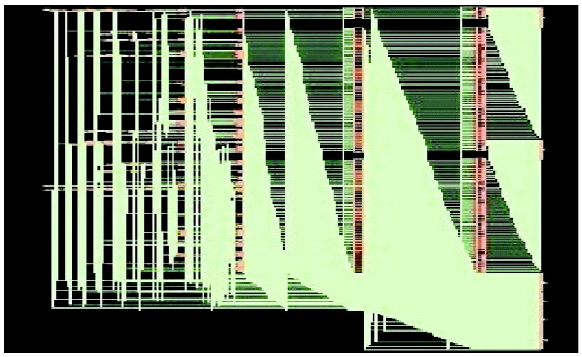

Figure 5: RTL Schematic of Dual Address NVM

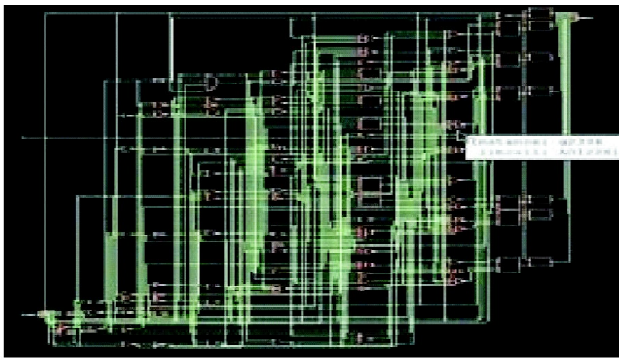

Figure 4: RTL Schematic of Dual Port VM

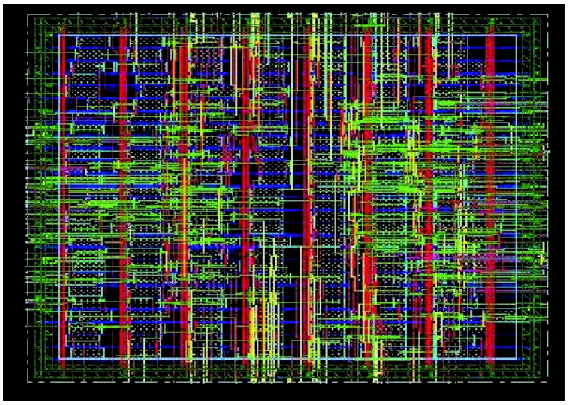

Figure 7: GDS II File of Dual Address VM

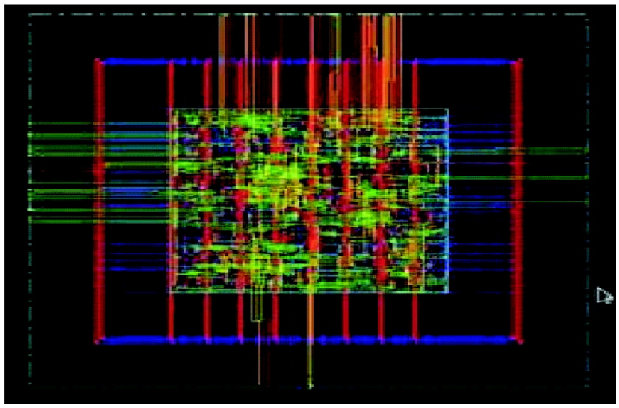

Figure 8: GDS II File of Dual Address NVM

Table 1
Post CTS Clock Tree Report Analysis of Dual Port NVM

Setup mode	*all*	*reg2reg*	*default*
WNS (ns) :	8.163	N/A	8.163
TNS (ns) :	0.000	N/A	0.000
Violating Paths :	0	N/A	0
All Paths :	16	N/A	16

5. CONCLUSION

Memory Structure plays a prominent role in the field of VLSI, Embedded Systems as well as Communications. This paper explains about several types of board level NVM's and VM's, in which few designs follow traditional approach to map the specification of MPEG applications. The Capacity of memory on board level is restricted up

to few kilobytes which are presently available in ASIC's. In some applications where huge amount of memory is required in such cases flash memories or cache memories are used which are compared to board level, the off chip memory decreases by two in terms of speed. Sometimes the board level memory area increases, so to reduce its area occupied on the chip all the blocks were implemented on SoC Encounter which is having very less area occupancy compared to the conventional memory structure.

6. ACKNOWLEDGEMENT

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