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Design and Implementation of Low Power Combinational Circuits using Reversible Logic

M. Janaki Rani[1], S. Anandhi[2] and Manivannan[3]

ABSTRACT

Recent technology advancement in VLSI designs offer shrinking device dimensions and lead to exponential increase in circuit complexities. But this device scaling is limited by the power dissipation, which needs better power optimizations methods. The conventional digital circuits generate more heat due to the effect of logic gates which are irreversible in nature. Reversible logic is used to reduce the power dissipation that occurs in digital circuits by preventing the loss of information. Reversible Logic finds applications in Low Power CMOS designs, Quantum Computing, digital signal processing, communication, computer graphics, cryptography and Nanotechnology. The design of combinational logic circuits like adder, comparator, decoder, encoder, multiplexer and demultiplexer using reversible logic gates Feynman gate, Fredkin gate, Toffoli gate, Peres gate, HNG gate etc are discussed in this paper. The above circuits are simulated using Xilinx ISE Simulator 12.1.

Keywords: Low power, reversible logic, Feyman, Fredkin, Peres, combinational circuit

1. INTRODUCTION

The conventional combinational logic circuits designed using basic logic gates have energy loss due to the information bit lost during the operation. The total no of outputs generated is less than the total number of inputs applied in digital system and this is the major cause of the lowering of entropy and information loss of the overall digital system. The amount of energy loss for one bit of information loss in an irreversible gate was given by R. Landauer in 1961 [1]. Later in 1973 C. H. Bennett has shown that this energy loss can be minimized or even removed if the circuit is made up from the reversible logic gates [2]. Reversible circuit designing is gaining wide scope in the area of Quantum computing, Low power

CMOS design, Nanotechnology, Optical computing, Signal processing, Advanced computing etc due to its ability to design low loss or approximately loss less digital circuits.

A reversible logic gate is an n-input, n-output (denoted n*n) logic device with one-to-one correspondence between the input and output. The important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed and loops are not permitted. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs. The unutilized outputs from a reversible gate/circuit are called garbage outputs. Also they must use minimum number of constant inputs [3, 4]. Reversible logic circuits should have minimum quantum cost and must use a minimum logic depth or gate levels. Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate and gate level refers to the number of levels which are required to realize the given logic function.

[1,2] Faculty, ECE Dept., Dr. M.G.R Educational & Research Institute, Chennai, *Emails: janakiranimathi@gmail.com, anandhibalaji04@gmail.com*

[3] Faculty, EEE Dept., Dr M.G.R. Educational & Research Institute, Chennai, *Email: manivannank79@yahoo.com*

This paper is organized as follows: Section 1 gives the introduction for reversible logic circuits. Section 2 gives some of the important reversible logic gates along with their logic functions. In Section 3 the design of combinational circuits full adder, full subtractor,, one bit comparator, 2:4 decoder, der, 4:2 encoder, 4:1 multiplexer and 1:4 demultiplexer using reversible logic gates is discussed. Section 4 gives the simulation results of all the designs. Section 5 gives the comparison of all the designs and Section 6 gives the conclusion.

2. REVERSIBLE LOGIC GATES

In this section the reversible logic gates like Feynman gate [5], Peres gate [6], Toffoli gate [3] Fredkin gate [4], HNG gate, M gate, L gate and BJN gate are discussed.

2.1. Feynman / CNOT Gate

Feynman gate is a 2*2 gate and its circuit is shown in Fig. 1. It is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs are A, B and outputs are P = A, Q = A⊕□□B and its quantum cost is one.

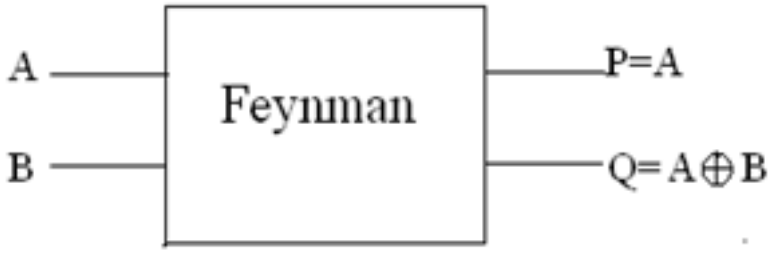

Figure 1: Feynman gate–2*2 gate

2.2. Peres Gate

Fig. 2 shows a Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs P = A,

Q = A⊕B, R = AB⊕C and its quantum cost is four.

Figure 2: Peres gate–3*3 gate

2.3. Toffoli Gate

Fig. 3 shows a Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P = A,

Q = B, R = AB⊕C and its quantum cost is five.

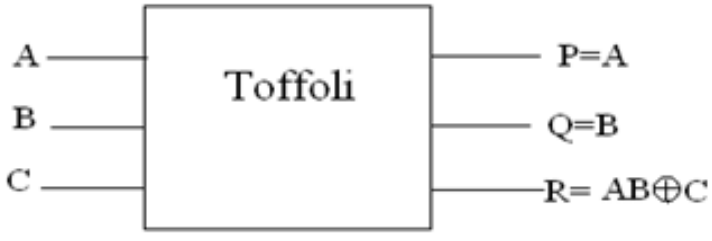

Figure 3: Toffoli gate–3*3 gate

2.4. Fredkin Gate

Fig. 4 shows a Fredkin gate which is a 3*3 gate with inputs (A, B, C) and outputs P = A,

Q = A□′B + AC, R = AB + A′C and its quantum cost is five.

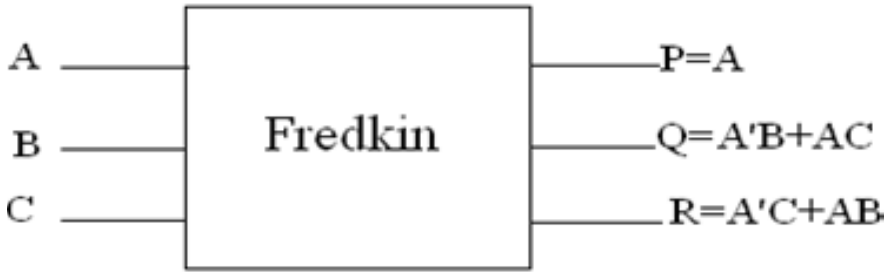

Figure 4: Fredkin gate–3*3 gate

2.5. HNG Gate

Fig. 5 shows a HNG gate which is a 4 × 4 gate with inputs (A, B, C, D) and outputs P = A,

Q = B, R = A⊕B⊕C, S = (A⊕B)C⊕AB⊕D and its quantum cost is six[7].It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

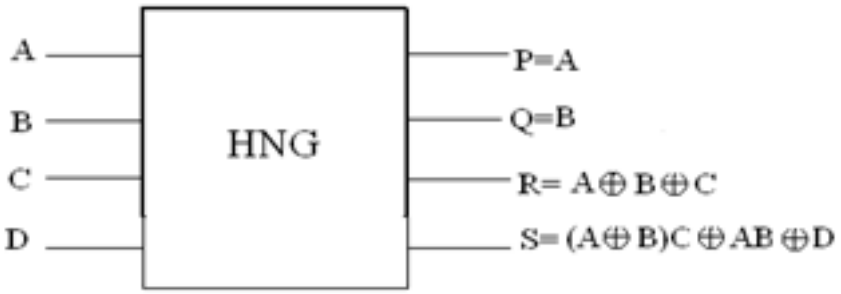

Figure 5: HNG gate–4*4 gate

2.6. M Gate

Fig. 6 shows a M gate [8]which is a 3*3 gate with inputs (A, B, C) and outputs P = A,

Q = (A⊕B)', R = AB'⊕C.

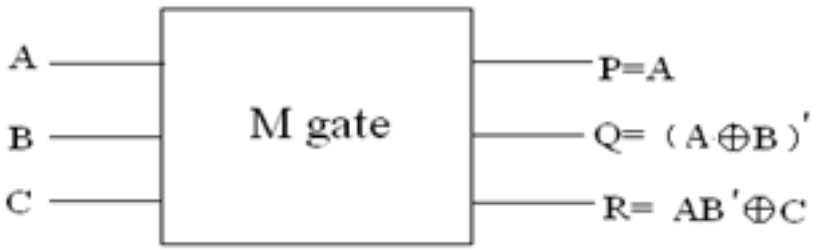

Figure 6: M gate–3*3 gate

2.7. L Gate

Fig 7 shows a L gate [8]which is a 3*3 gate with inputs (A, B, C) and outputs P = A,

Q = B, R= (A+B)'•"C.

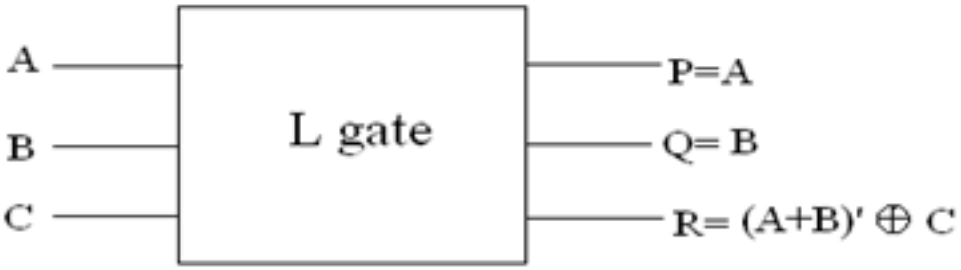

Figure 7: L gate–3*3 gate

2.8. BJN Gate

Fig. 8 shows a BJN Gate which is a 3*3 gate with inputs (A, B, C) and outputs P = A, Q = B, R = (A+B) ⊕C. It has quantum cost five.

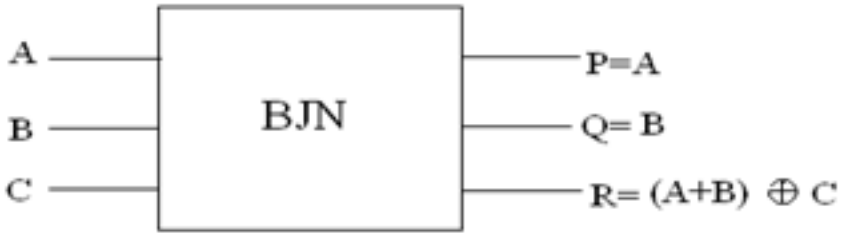

Figure 8: BJN gate–3*3 gate

3. REVERSIBLE LOGIC CIRCUITS

3.1. Reversible Full adder

Full adder is the fundamental building block in many computational units. The full adder circuit's output is given by the following equations:

$$Sum = A \oplus B \oplus Cin$$
$$Cout = (A \oplus B)Cin \oplus AB$$

The reversible logic implementation of full-adder circuit is shown in Fig. 9. This reversible full adder circuit is realized using two 3*3 Peres gates [9] and it is efficient in terms of gate count, garbage outputs and constant input than the existing counter parts.

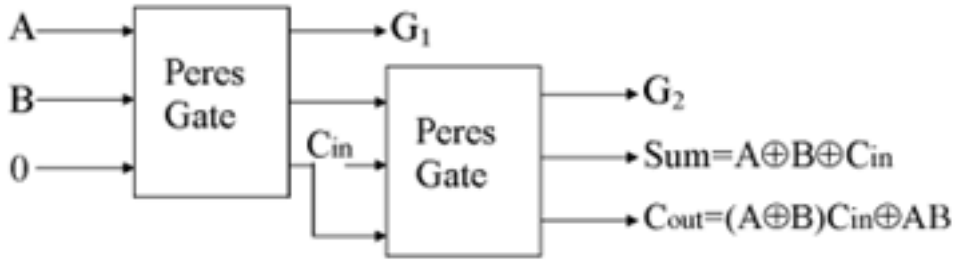

Figure 9: Reversible full adder

3.2. Reversible Four bit adder

The block diagram of four bit ripple carry adder using HNG gates is shown in Fig 10.

3.3. Reversible one bit comparator

The conventional one-bit digital comparator [10], consists of two NOT gates, two AND gates and one NOR gate is shown in Fig.11. The truth table of one bit comparator is given in Table 1.

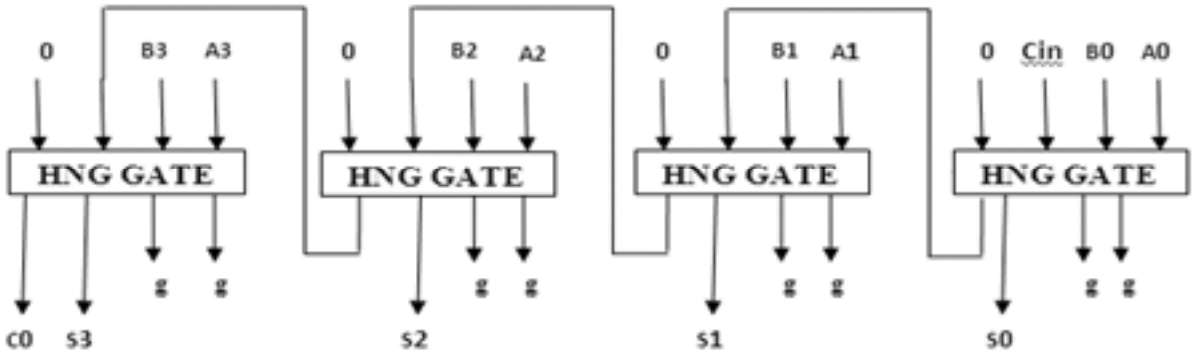

Figure 10: Reversible four bit ripple carry adder

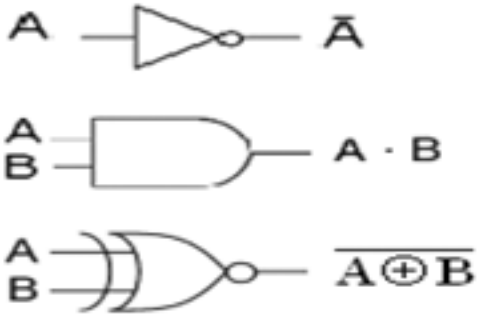

Figure 11: Irreversible gates for one bit comparator

Table 1
Truth Table of One Bit Comparator

Inputs		Outputs		
A	B	FA>B	FA<B	FA=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

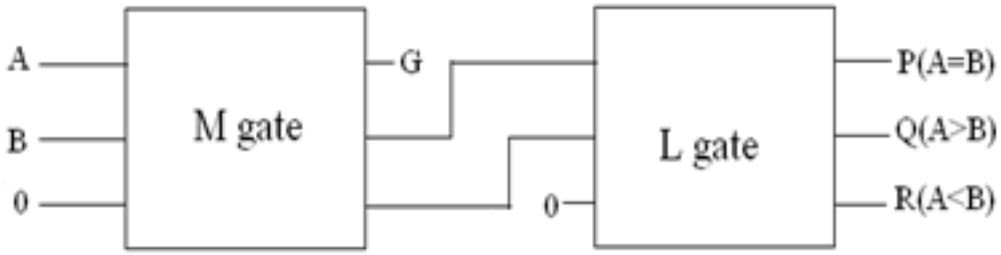

Fig 12: Reversible one bit comparator

A reversible one bit comparator is designed using Mgate and L gate[8] as shown in Fig.12. It uses two constant inputs as logic'0' and has one garbage output.

3.4. 2:4 Reversible Decoder

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. It is a multiple-input, multiple-output logic circuit that converts coded inputs into

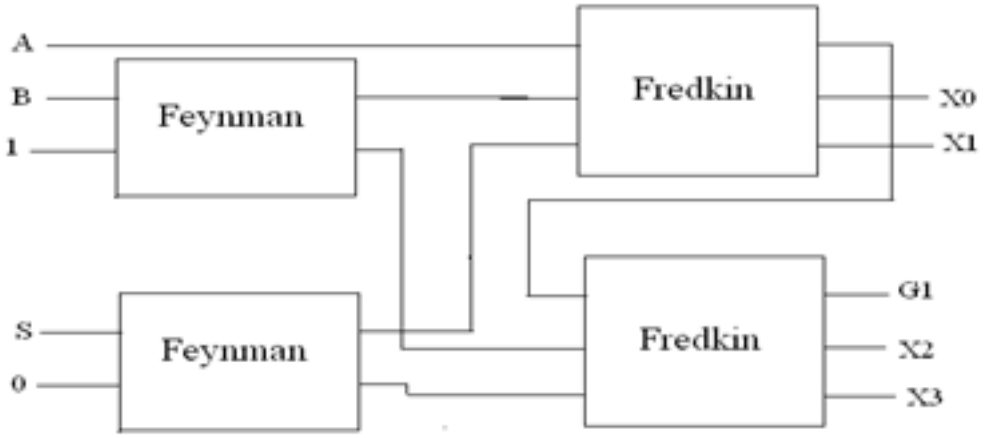

Figure 13: Reversible 2:4 decoder

Table 2
Truth Table of 2:4 Ecoder with Enable Input

Enable Input	Inputs				Outputs	
S	A	B	X0	X1	X2	X3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

coded outputs, where the input and output codes are different. Enable inputs are required for the decoder to function, otherwise its outputs assume a single “disabled” output code word. Decoders are used in data multiplexing, seven segment display and memory address decoding. The truth table of decoder is given in Table II.The design of 2:4 decoder using Feynman gate and Fredkingate[11] is shown in Fig. 13 and it has one garbage output G1.The inpts are A, B and it has the enable input as S and the outputs are X0, X1, X2, X3.

3.5. A reversible 4:2 encoder

An encoder has 2^n input lines and n output lines. The output lines generate a binary code corresponding to the input value. The truth table of encoder is given in Table III. The design of 4:2 encoder using using two Fredkin gates[12] is shown in Fig. 14. It has four inputs I0, I1, I2 I4 and two outputs Y1&Y2. It has four garbage outputs G1, G2, G3 and G4.

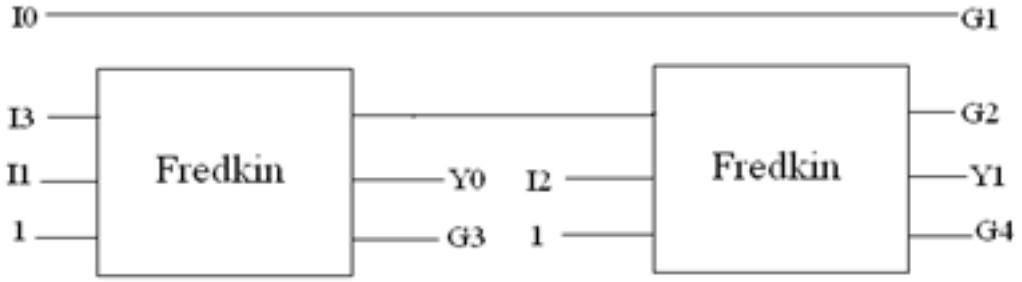

Figure 14: Reversible 4:2 encoder

Table 3
Truth Table Of 4:2 Encoder

Inputs				Outputs	
I3	I2	I1	I0	Y1	Y0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	X	x

3.6. A reversible 4:1 multiplexer

A multiplexer or MUX is a combinational logic circuit that has several inputs and only one output. MUX directs one of the inputs to its output line by using select lines. A multiplexer has 2^n data inputs, n selection inputs and a single output. Selection input determines the input that should be connected to the output. The truth table of 4:1 multiplexer is given in Table IV.

Fig. 15 shows the block diagram of a 4:1 multiplexer using three modified Fredkin (MFRG) gates[13]. It has two select inputs S0, S1 and four data inputs I0, I1, I2, I3. The output is Y and this circuit has five garbage outputs G1, G2, G3, G4, G5.

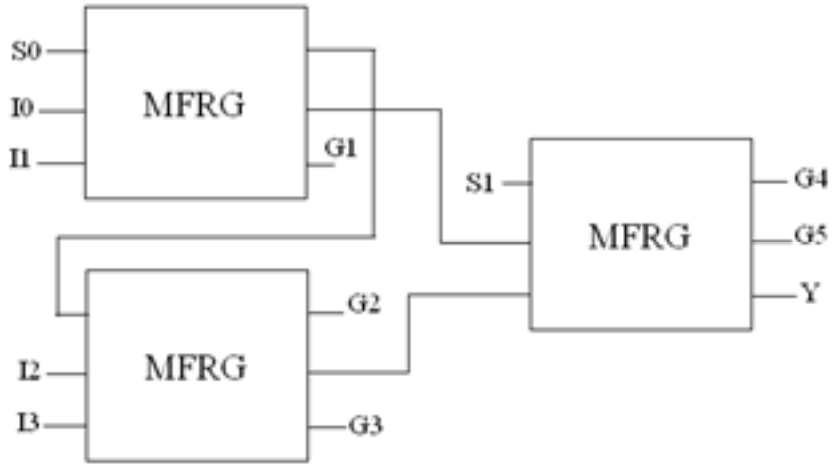

Figure 15: Reversible 4:1 multiplexer

Table 4
Truth Table of 4:1 Multiplexer

Select Inputs		Inputs				Output
S1	S0	I3	I2	I1	I0	Y
0	0	X	X	X	0	0
0	0	X	X	X	1	1
0	1	X	X	0	X	0
0	1	X	X	1	X	1
1	0	X	0	X	X	0
1	0	X	1	X	X	1
1	1	0	X	X	X	0
1	1	1	x	x	x	1

3.7. A reversible 1:4 demultiplexer

It is a digital logic circuit which performs inverse operation of the multiplexer. It has one input line Din and transmits it to one of 2^n possible output lines. The selection of the specific output is controlled by the bit combination of n select inputs.

The truth table of 1:4 demultiplexer is given in Table V. Fig. 16 shows the block diagram of a 1:4 demultiplexer using Toffoli gates and Peres gates[14]. It has two select inputs S0, S1, one data input Din, enable input E and four outputs Yo, Y1, Y2, Y3. This circuit has nine garbage outputs.

4. SIMULATION RESULTS

All the circuits are implemented using VHSIC hardware description language (VHDL).The simulation is done on Xilinx ISE 12.1 on Spartan 3 using target device: XC3S50-PQ208. The simulation waveform of

Table 5
Table V Truth Table Of 1:4 Demultiplexer

Enable input	Select Inputs		Outputs			
E	S1	S0	Y0	Y1	Y2	Y3
1	0	0	Din	0	0	0
1	1	0	0	Din	0	0
1	0	1	0	0	0	Din
1	1	1	0	0	0	Din
0	X	X	0	0	0	0

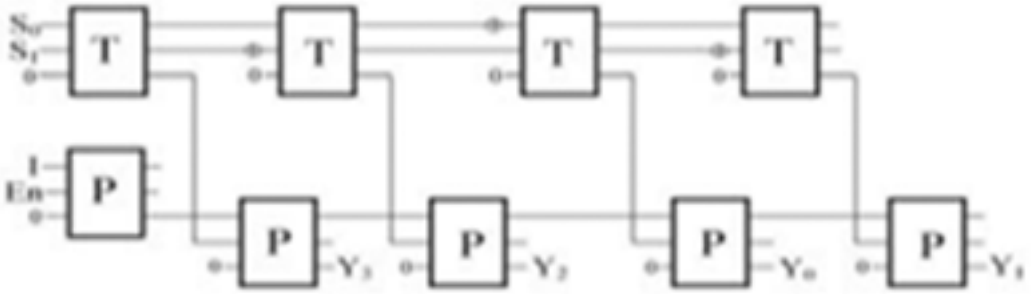

Fig. 16. Reversible 1:4 demultiplexer

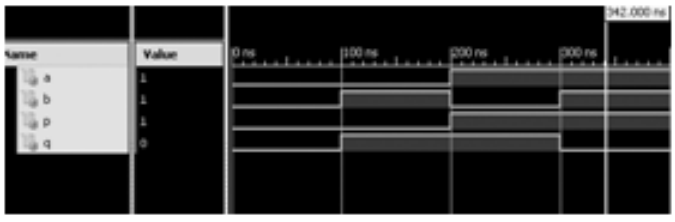

Figure 17 (a): Output waveform of Feyman Gate

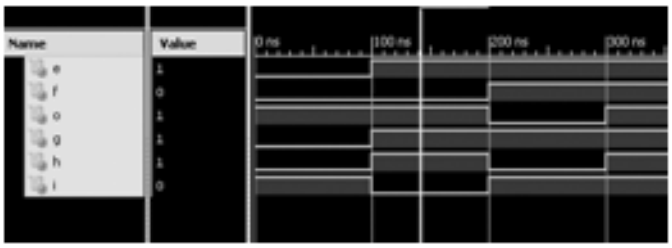

Figure 17 (b): Output waveform of Fredkin Gate

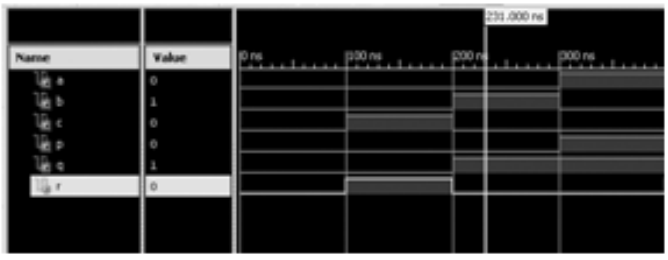

Figure 17 (c): Output waveform of Peres Gate

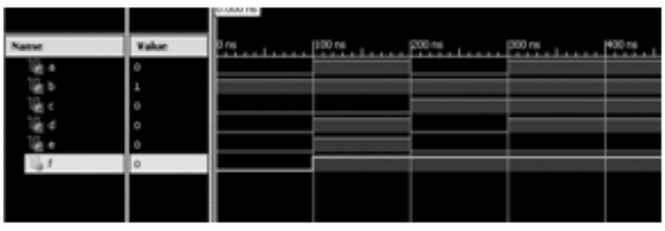

Figure 17 (d): Output waveform of MFRG Gate

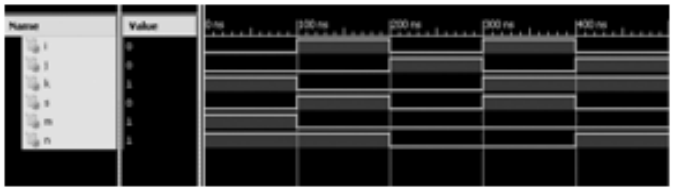

Figure 17 (e): Output waveform of M Gate

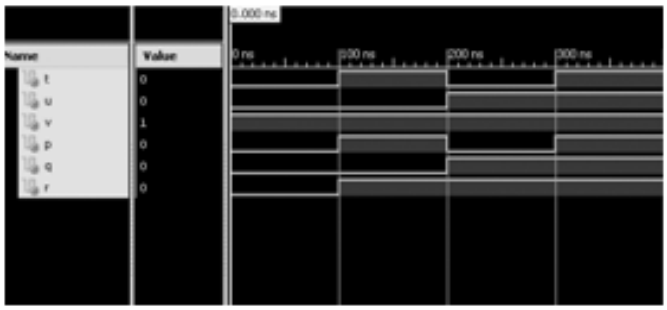

Figure 17 (f): Output waveform of L Gate

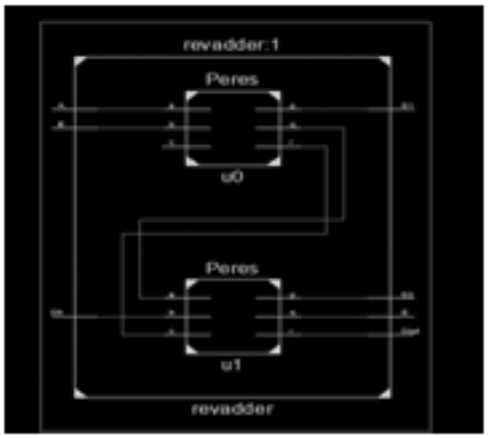

Figure 18 (a): RTL view of reversible adder

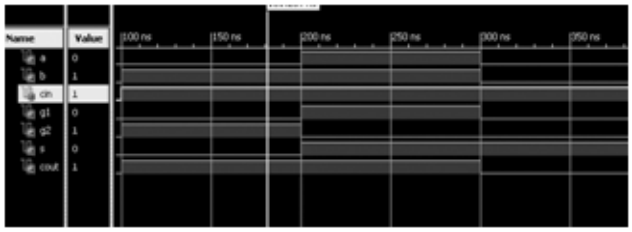

Figure 18 (b): Output waveforms of reversible adder

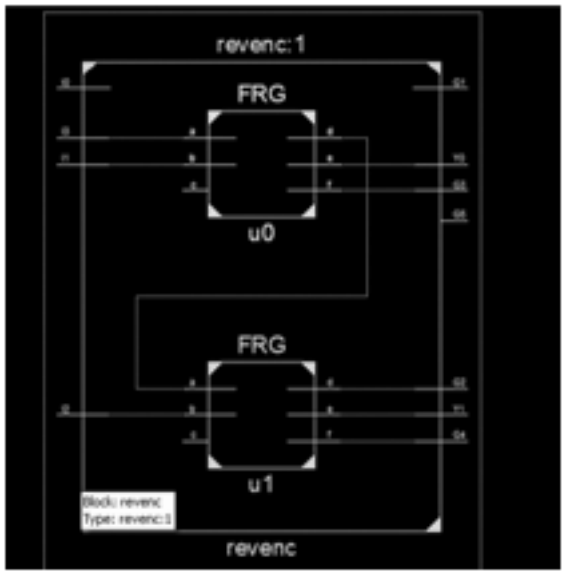

Figure 19 (a): RTL view of reversible encoder

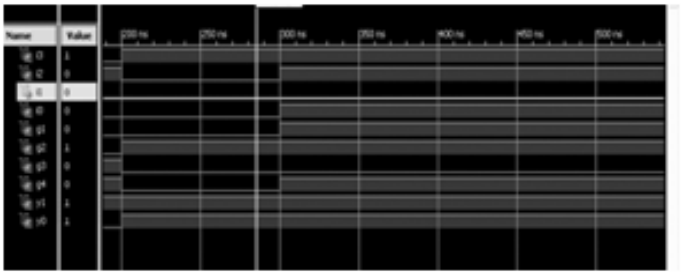

Figure 19 (b): Output waveforms of reversible encoder

Feyman gate, Fredkin gate, Peres gate MFRG gate, M gate and L gate are shown in Fig. 17 a, b, c, d, e and f respectively.The RTL schematic and output waveforms for reversible adder, reversible encoder, reversible multiplexer and reversible decoder are shown in Fig. 18, Fig. 19, Fig. 20 and Fig. 21 respectively.

5. CONCLUSION

In this paper various reversible logics like Feyman gate, Fredkin gate, Peres gate, M gate, L gate and modified Fredkin gateMFRG are implemented using VHDL coding in Xilinx 12.1. Also the combinational

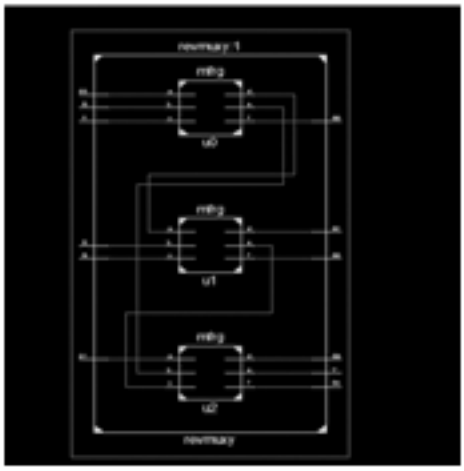

Figure 20 (a): RTL view of reversible multiplexer

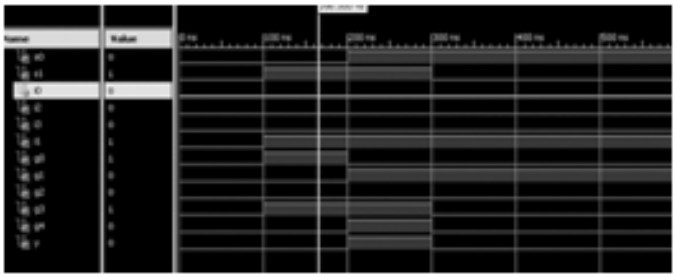

Figure 20 (b): Output waveforms of reversible multiplexer

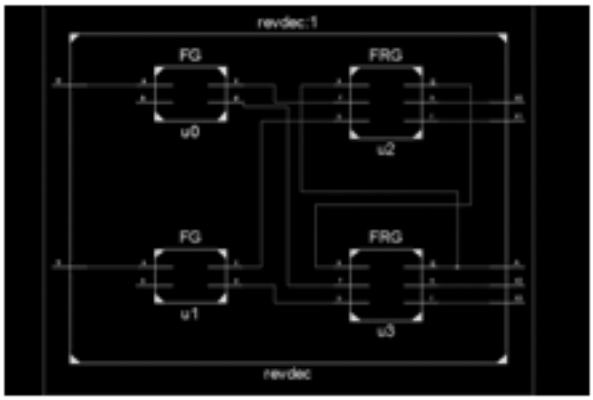

Figure 21 (a): RTL view of reversible decoder

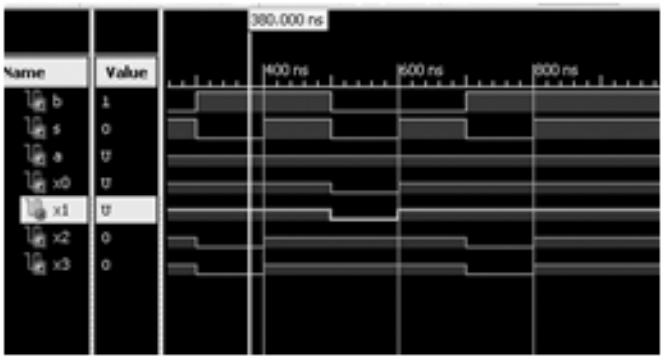

Figure 21 (b): Output waveforms of reversible decoder

logic circuits like full adder, decoder, encoder, demultiplexer and multiplexer are are designed using the above mentioned reversible logic gates and their RTL schematic and simulation results are presented in this paper. These reversible circuits can be used for the design of ultra low power digital circuits, quantum computers and for applications in cryptography and nanotechnology.

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