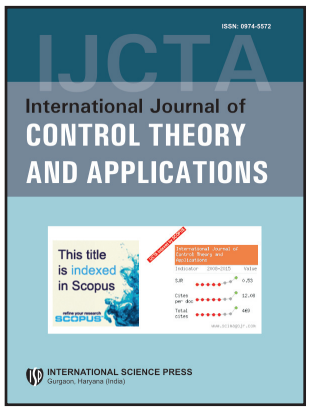

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Performance Analysis of All-Optical D-flip-flop

R. Manohari[a], K. Naga Maruthi[b] and Shanthi Prince[c]

[a]*Assistant professor, ECE Department, SRM University, Chennai, Tamilnadu-603203, India. Email: manohari.r@ktr.srmuniv.ac.in*
[b]*M.Tech. Student, ECE Department, SRM University, Chennai, Tamilnadu-603203, India. Email: kavuri.nagamaruthi@gmail.com*
[c]*Corresponding author, Professor, ECE Department, SRM University, Chennai, Tamilnadu-603203, India. Email: shanthi.p@ktr.srmuniv.ac.in*

Abstract: For digital signal processing, All-Optical flip-flops are the key elements. Based on Semiconductor Optical Amplifier (SOA) the systematic model for All-Opticalflip-flop is proposed and simulated. The strategy of optical pulse propagation in SOA based on cross-gain modulation (XGM) is used in this design. All-Optical D-flip-flop is simulated and its functions are verified with the help of truth table. All-optical D-flip-flop is designed using all-optical logic gates. The functioning of the D-flip-flop is analyzed for different data rates. The performance is analyzed based on Q-factor and BER. Further improvement can be achieved by modifying the operation parameters of SOA.

***Keywords*:** All-Optical Flip-flop, All-Optical Logic Gates, Cross gain modulation.

1. INTRODUCTION

Flip-flops can be used for secured optical communication, such as encryption and decryption techniques at transmittter and receiver respectively [1]. By using all-optical flip-flop, bottle neck due to Optical-Electrical-Optical (O-E-O) conversion can be avoided and also high data rate can be achived.

All-Opticalflip-flops are the key components for photonic digital processing in next generation optical networks and optical computing. Semiconductor Optical amplifier based devices have been proposed as suitable alternatives in All-Optical signal processing. Realization of future All-Optical switching networks depends on All-Optical signal processing functions such as All-Optical header recognition, switching, wavelength conversion, logic gates an D-flip-flops. Semiconductor optical amplifiers are useful building blocks for all-optical gates as wavelength converters and demultiplexers[2].The advantages of SOAs are their versatility and possibility of monolithic integration with other optical components like passive waveguides and couplers to perform more complex functions[3-7].

SOAs are compact, electrically pumped and have the large optical bandwidth. Moreover, they allow a wide flexibility in the choice of gain peak wavelength. The challenges related to SOA performance are polarization sensitivity reduction, Optical feedback reduction and decreasing the noise level of SOAs. Authors

have demonstrated a simple all-optical multilogic gate based on cross-phase modulation. Digital logic operations including XOR, AND, and OR of two input data signals are demonstrated using a single device[8].

By using the gain nonlinearity characteristics of cross gain modulation (XGM) in a semiconductor optical amplifier (SOA), XOR and AND gates can be demonstrated[9-13]. A novel frequency encoded AND logic gate has been proposed and successfully simulated by exploiting various non-linearities in SOAs[14].The gain nonlinearity characteristics of semiconductor optical amplifier are used to design the All-Optical gates[12-13].

The first step in designing a D-flip-flop is to realize All-Optical AND and NOR gates. Next by combining AND, NOR gates D-flip-flop is realized. In most digital applications, signal synchronization with an external reference clock is a basic feature. In this paper, All-Optical clocked D-flip-flop is proposed and demonstrated. The organization of the paper is as follows, section 2gives the design of the D-flip-flop and section 3 describes the design of All-Optical gates using SOA. In section 4 simulation results are discussed.

2. DESIGN OF D-FLIP-FLOP

Practical implementation of All-Optical signal processing unit requires integrated All-Optical devices for ease of manufacturing, installation and operation.

Cross Gain Modulation based wavelength conversion is one of the simplest schemes to achieve All-Optical wavelength conversion which employs gain saturation effect in the active region of SOAs.

The D-flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. This flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell.

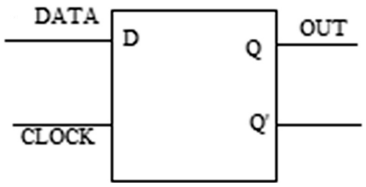

Figure 1: Symbol of D-flip-flop

The symbol of D-flip-flop is shown in figure1. The two inputs are D and clock. When the clock is active, the output Q is same as D input. The second output Q' is the complement of Q.

The D-flip-flop will act as a storage element for a single binary digit (Bit). Any input appearing (present state) at the input D, will be produced at the output Q by applying active clock signal. If in the present state D = 0 and CLK = 1, the next state will be Q = 0 and it is same as D .When the clock is high the output Q = D.

The truth table for D-flip-flop is shown in Table 1. (NC means No. change in the output, it remains same).

Table 1
Truthtable for D-flip-flop

CLK	*D*	*Q (t + 1)*	*Q′*
0	0	Q (NC)	Q′
0	1	Q (NC)	Q′
1	0	0	1
1	1	1	0

Only when the clock is '1', the D-flip-flop output is same as the input. Otherwise, the output (Q) of D-flip-flop is same as the previous output i.e. No. change Q(NC) in the output.

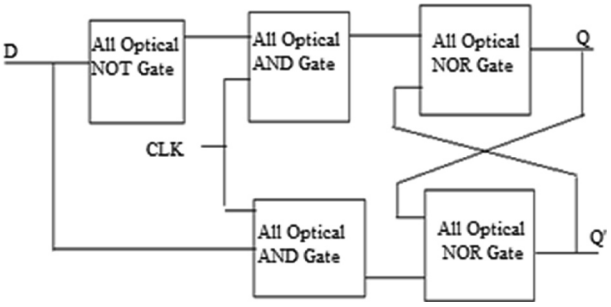

Figure 2: Block schematic of D-flip-flop

The block schematic for D-flip-flop is shown in Figure 2. The D input is given to All-optical NOT gate. The D input and it's complement are treated as one input to the two All-optical And gate. The other input to both the AND gate will be the clock signal. The output from the AND gates are used as one input of two All-optical NOR gate. The other input will be the signal from the feedback of outputs (Q and Q′). So, based on the above figure the D-flip-flop can be designed using All-Optical gates.

From the block schematic, it becomes obvious that to design All-Optical D-flip-flop, we need All-Optical logic gates, which are discussed in the following section.

3. DESIGN OF ALL-OPTICAL GATES USING MZI-SOA

3.1. MZI- SOA

The MZI-SOA is a device with two input/output ports on each side. The ports are bidirectional in the sense that the same port can be used as an input port or an output port. This is due to the bidirectional operation of the SOAs. The interferometer is comprised of two branches in which an SOA is placed. In a basic operation, the SOA acts as a nonlinear element, inducing an additional phase change on one of the signals propagating through it. This phase change is caused by another signal that can be co- or counter-propagating through the same SOA. From now on, the different configurations to achieve the logic Boolean functions and the specific use of each input/output port of the MZI-SOA will be analyzed.

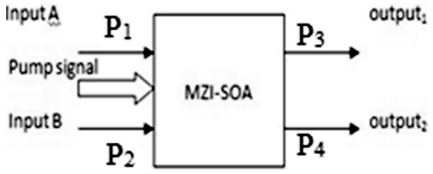

Figure 3: Functional Block diagram of MZI-SOA

The functional block diagram shown in Figure 3 consists of four ports. $Port_1(P_1)$ and $Port_2(P_2)$ act as input ports whereas $Port_3(P_3)$ and $Port_4(P_4)$ act as output ports. The pump signal acts as a control signal for SOA.

Output Equations of MZI-SOA are as follows:

$$Port_3(t) = \frac{P_{in}(t)}{4}\left\{G_1(t) + G_2(t) - 2\sqrt{G_1(t)\times G_2(t)}\times\cos\left[-\frac{\alpha}{2}\times\ln\left(\frac{G_1(t)}{G_2(t)}\right)\right]\right\} \quad (1)$$

$$Port_4(t) = \frac{P_{in}(t)}{4}\left\{G_1(t) + G_2(t) + 2\sqrt{G_1(t)\times G_2(t)}\times\cos\left[-\frac{\alpha}{2}\times\ln\left(\frac{G_1(t)}{G_2(t)}\right)\right]\right\} \quad (2)$$

where, $G_1(t)$-Gain of SOA_1; $G_2(t)$-Gain of SOA_2; P_{in}-power of incoming signal; α-line width enhancement factor.

3.2. Design of All-optical AND Gate

When both the inputs of AND gate are high the output is high. If anyone of the input is low, the output is low. The Boolean expression for AND gate is X=A.B, where A and B are input signals and X, is output. Block schematic of AND gate is shown in Figure 4 and its truth table in Table 2.

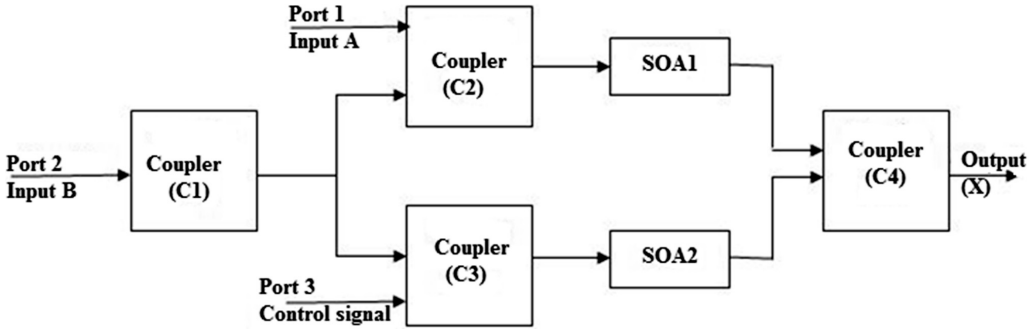

Figure 4: Block Schematic for AND Gate

The principle of operation for the AND gate is as follows, the data sequences to be compared are driven to the MZI-SOA. Data signals enter the device at ports 1 and port 2.While in port 3, a control signal is given. An optical pulse will be obtained at the output only in the case when both data signals are "1". When B = 0, A = 1 the gate does not produce any signal at the output. In the last case (shown in Table 2) in which B = 1 and A = 0 the comparison is enabled, but as the signal at port1 and the signal at port 2 are zero, No. power is obtained at the output of the device.

Table 2
Logical AND Gate truthtable

Input A	*Input B*	*Output X = A . B*
0	0	0
0	1	0
1	0	0
1	1	1

The data sequences are generated at 1545 nm wavelength with a power of 0.3mwusing optical Gaussian pulse generator. A continuous wave is generated at a wavelength of 1540 nm with a power of 0.25 mw. These signals are given to the MZI-SOA ports for performing AND operation. A Gaussian optical filter with 20 GHz bandwidth is used for filtering purpose. This filter is centered at 1540 nm wavelength so that only the desired signal is obtained. The resultant signal is the AND operation between the two data signals applied at port 1 and port 2 of MZI-SOA setup.

The layout of AND gate in Optisystem is shown in Figure 5 The sequence at the input of AND gate are 1110 and 1111. The corresponding optical pulses are shown in Figure 6 and Figure 7.

For the inputs 1110 and 1111, the logical AND operation output is 1110.It is verified with its truth table. The Output X of AND Gate is shown in Figure 8 shows the result of AND operation.

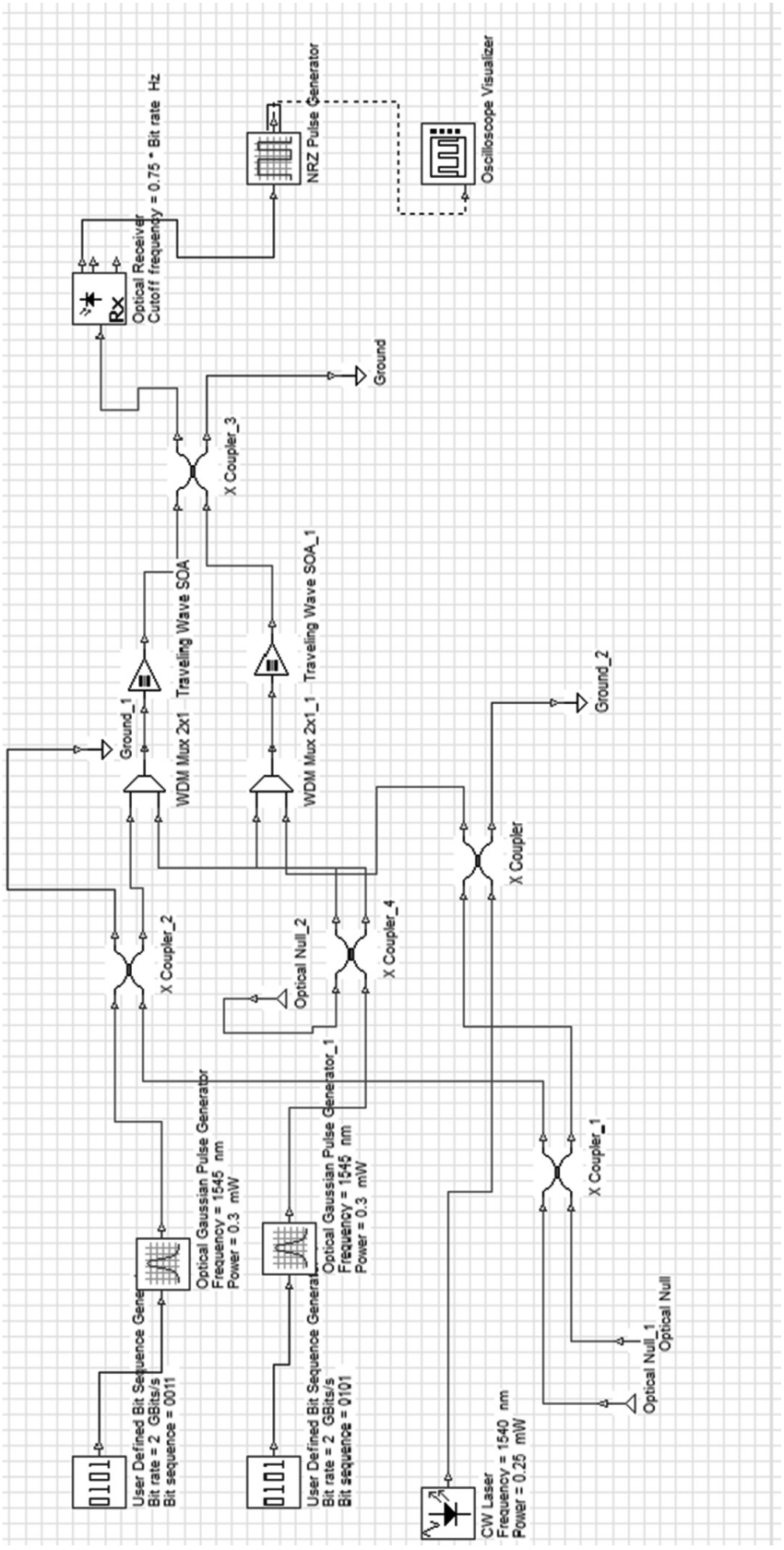

Figure 5: Simulation layout for AND Gate

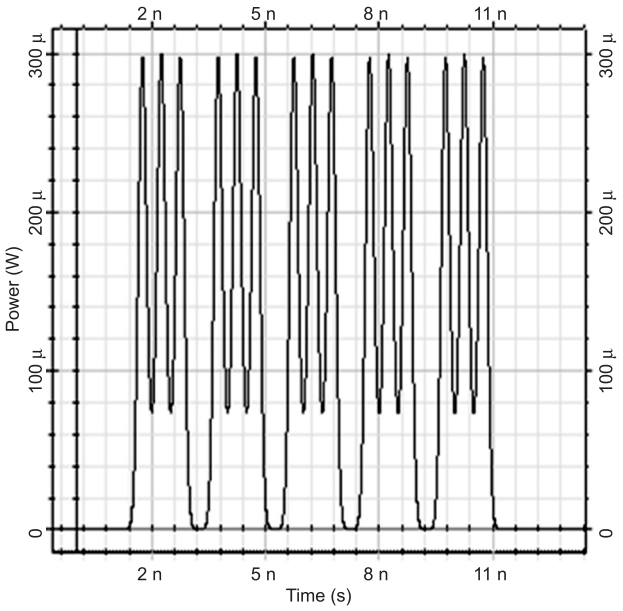

Figure 6: Input A (1110) for AND Gate

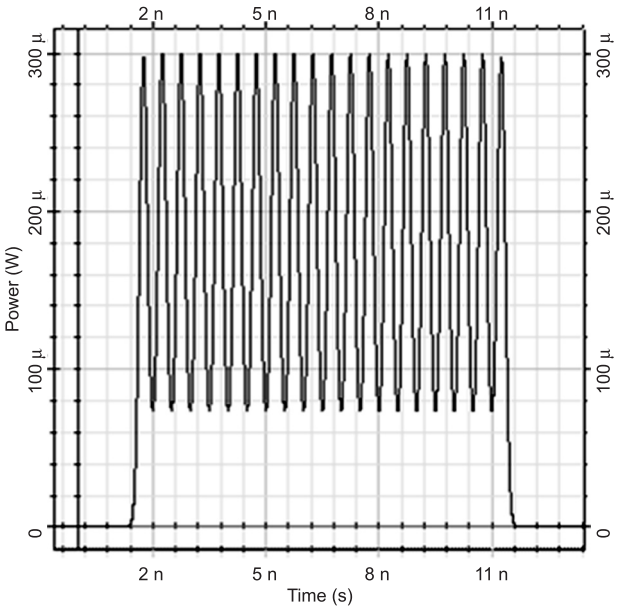

Figure 7: Input B (1111) for AND Gate

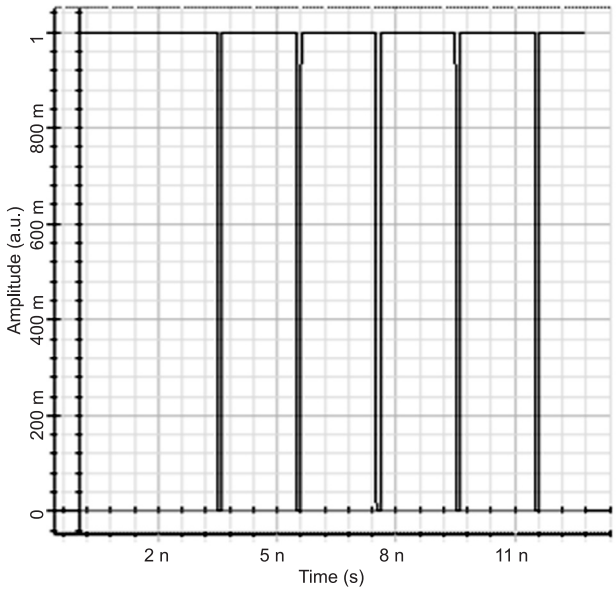

Figure 8: Output X (1110) of AND Gate

3.3. Design of All-Optical NOR Gate

In the NOR gate, the two data signals are coupled at the coupler (C1) and the coupled signal is given to SOA. The signals that are split are amplified by two SOAs and then coupled by a coupler (C3). Thus, it is carrying the OR operation between the two input signals. This is quite simple than AND operation because wavelength conversion is not used.

The block schematic for NOR gate is shown in Figure 9 and its truth table is given in Table 3. The two inputs are A and B. The output is high only when both the inputs are '0'. For the remaining combinations of input, the output is Low. That is, if one of the inputs is high then the Output is Low**.**

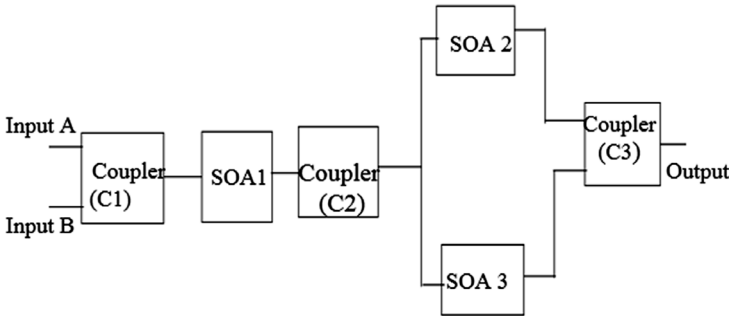

Figure 9: Block Schematic for NOR Gate

Table 3
Logical NOR Gate truthtable

Input A	*Input B*	*Output X = (A + B)'*
0	0	1
0	1	0
1	0	0
1	1	0

The layout of NOR gate in Optisystem is shown in Figure 10. The sequences at the input of NOR gate are 0011 and 0101. The corresponding optical pulses are shown in Figure 11 and Figure 12.

The sequence 0011 is the input A, and 0101 is the input B for NOR gate. Both sequences have same frequency and power.

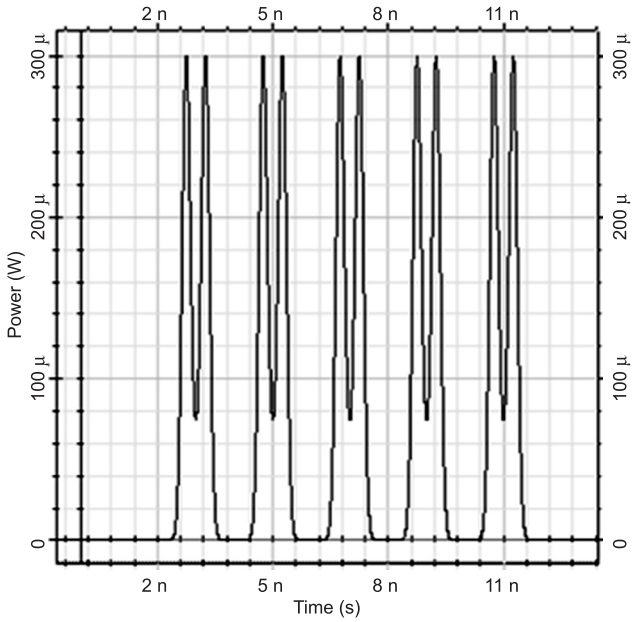

Figure 11: Input A (0011) of NOR Gate

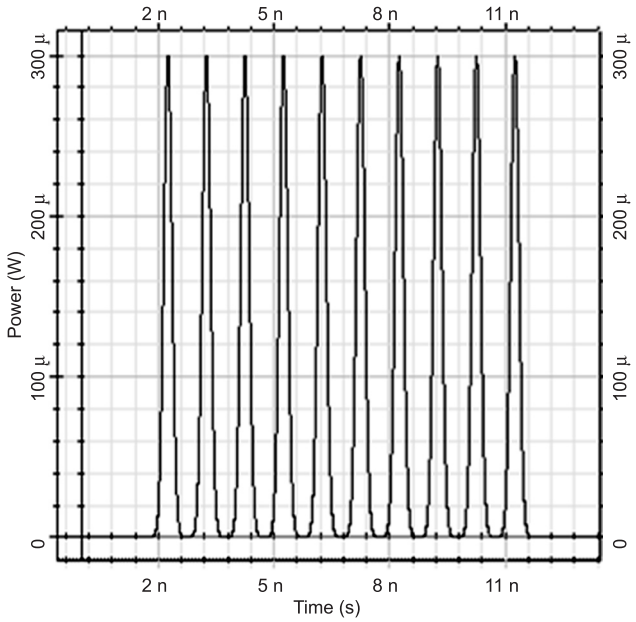

Figure 12: Input B (0101) of NOR Gate

When the inputs of NOR Gate are 0011 and 0101, then the Output of NOR gate is 1000 and it is verified with its truth table. The output sequence is shown in Figure 13.

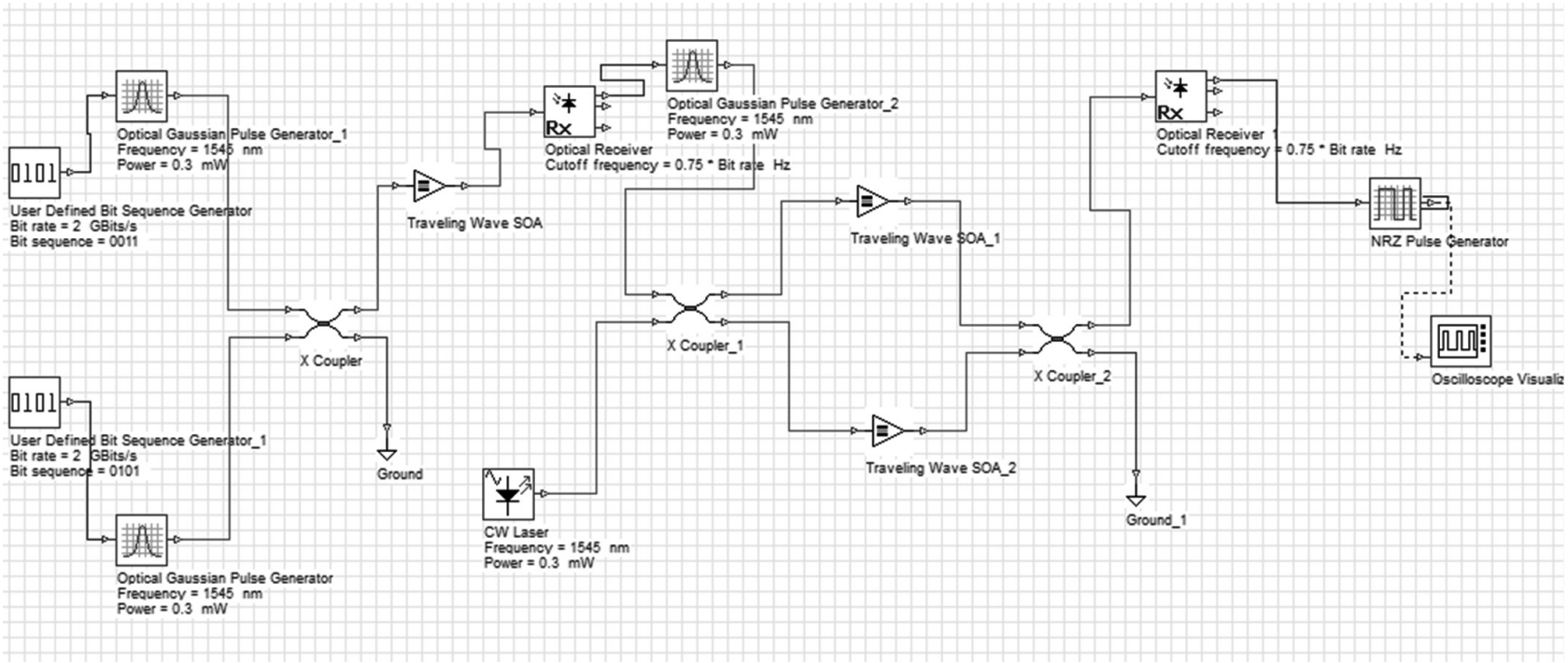

Figure 10. Simulation layout of NOR Gate

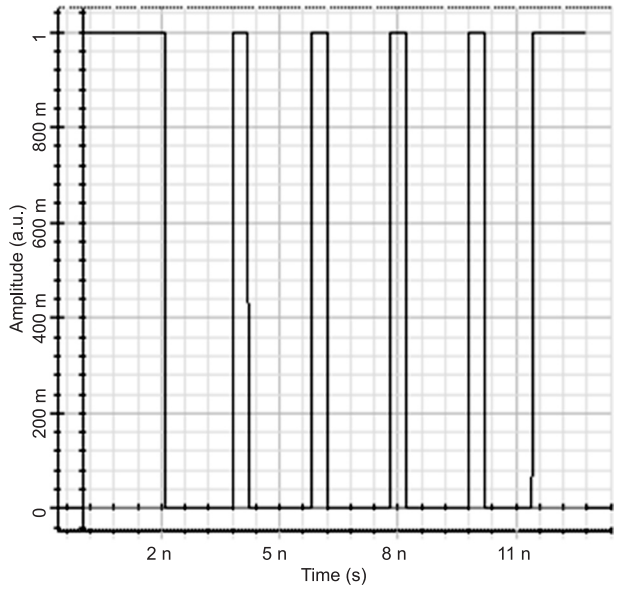

Figure 13: Output X (1000) of NOR Gate

3.4. Design of All-Optical NOT Gate

The NOT gate operation of one input port and one output port inverts the input signal, so whenever there is logic "1" at the input, logic "0" is obtained at the output, and vice versa. In MZI-SOA based NOT gate operation, two signals involved in this process: the original input data, and the control signal. The input data is the one to be inverted. SOA-MZI based NOT gate is shown in Figure 14.The NOT gate design consists of a control signal which is coupled to the input signal and is given to two SOAs. The two SOAs operated in opposite modes and gives reverse the output with corresponding input.

The block schematic of the NOT gate is shown in Figure 14.

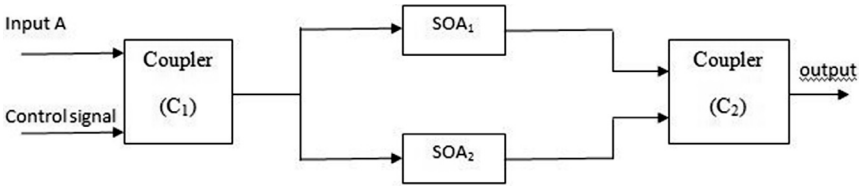

Figure 14: Block schematic of NOT gate

The truth table for the NOT gate is shown in Table 4. The output of the NOT gate is logic "1" if input data bit is "0" and logic "0" if input data bit is "1".

Table 4
Truth table for NOT gate

Input A	*Output* $Y = \overline{A}$
0	1
1	0

The simulation layout for the NOT gate is shown in Figure 15. In this setup, one data signal and one control signal are used. NOT operation is performed on the input data. The input data signal and control signal is given to both the input ports of the same coupler (C_1). The coupler splits the incoming signal and feeds it to both the SOAs. After passing through SOAs the output of both the SOAs is fed to the output coupler (C_2). The output coupler combines both the input signals and provides the output.

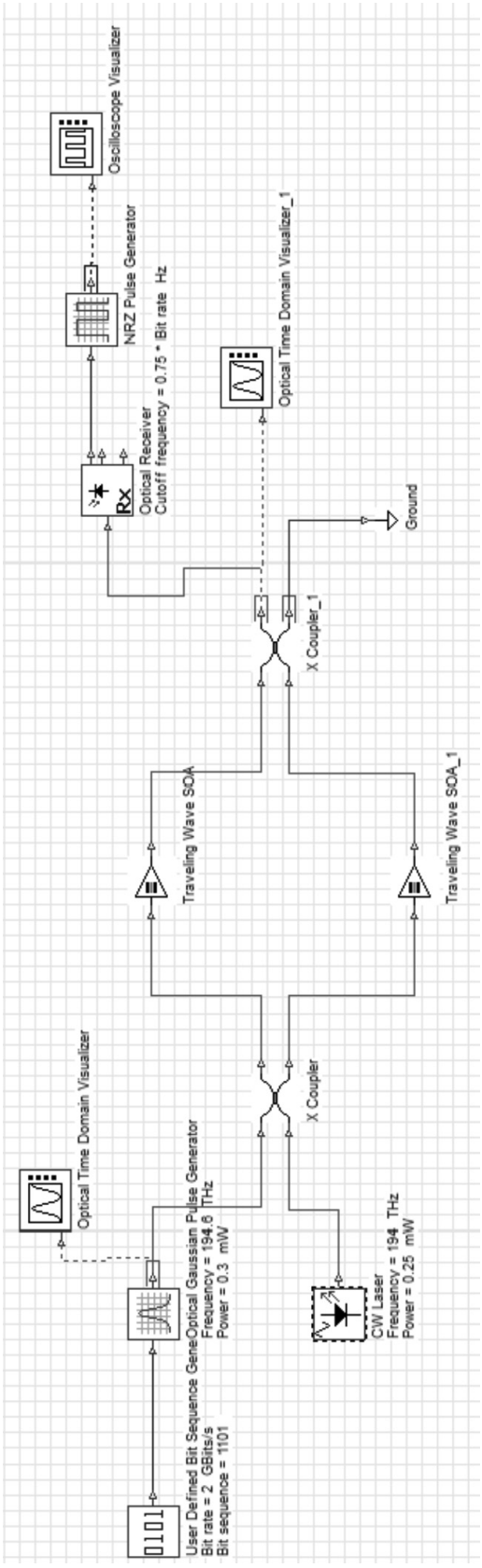

Figure 15: Simulation layout for NOT Gate

To verify the NOT operation in the designed NOT gate, the data sequences A = 1101 is given as inputs as shown in Figure 16. The signal is generated at a wavelength of 1540 nm (194.6 THz frequency) with a power of 0.3 mW, at a bit rate of 2 Gbps. The CW signal is generated at 1545 nm (194.6 THz frequency) with a power of 0.25 mW.

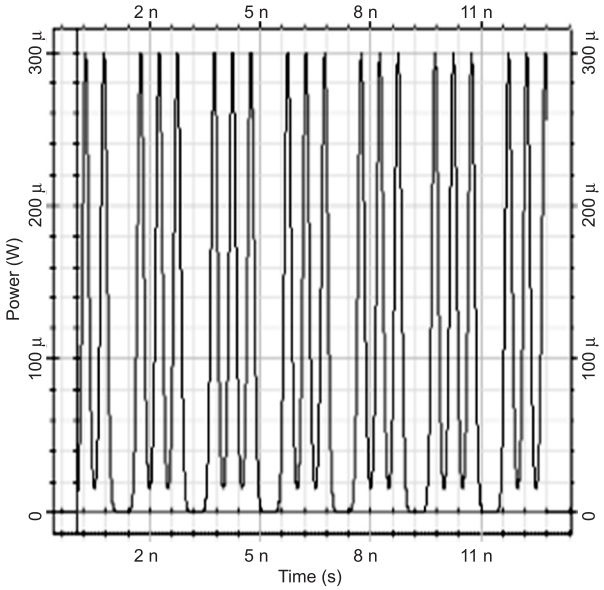

Figure 16: Input A (1101)

The result of NOT operation on signal is shown in Figure 17.

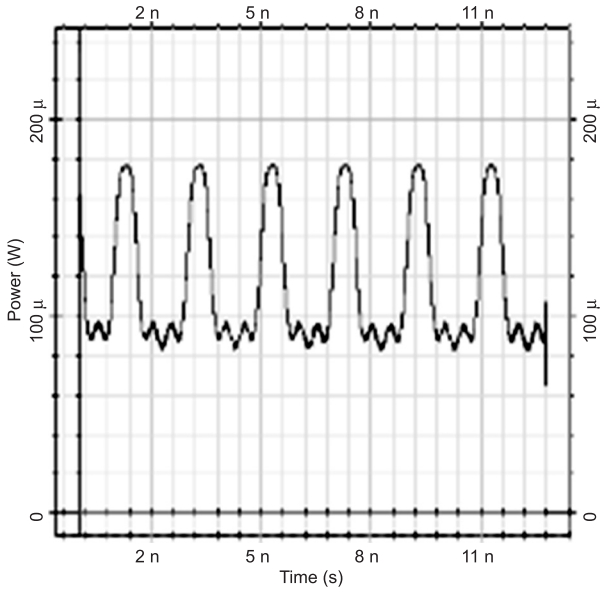

Figure 17: (a) Optical Output(0010)

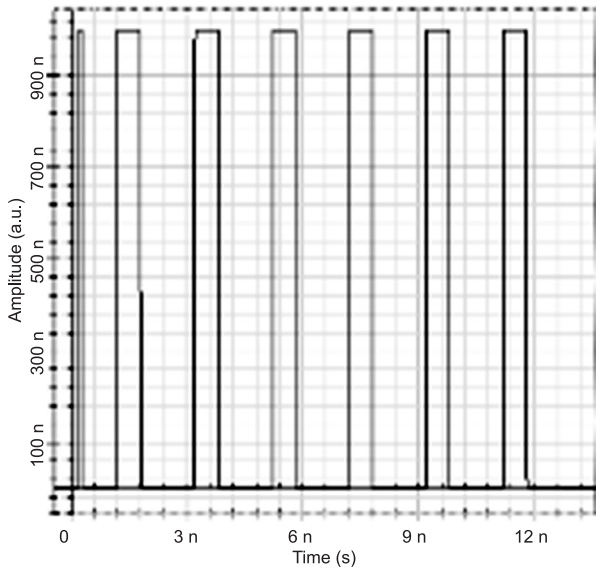

Figure 17: (b) Electrical Output(0010)

It is analyzed using Optical Time Domain Visualizer and Oscilloscope Visualizer. The output (Y) is obtained at the same wavelength i.e. 1540 nm at which the data signal is generated.

4. SIMULATION RESULTS OF ALL-OPTICAL D-FLIP-FLOP

The design of All-optical D-flip-flop shown in Figure 2, is simulated in Optisystem using the designed all-optical logic gates described in the previous section. The simulation layout of the All-optical D-flip-flop is shown in Figure 18.

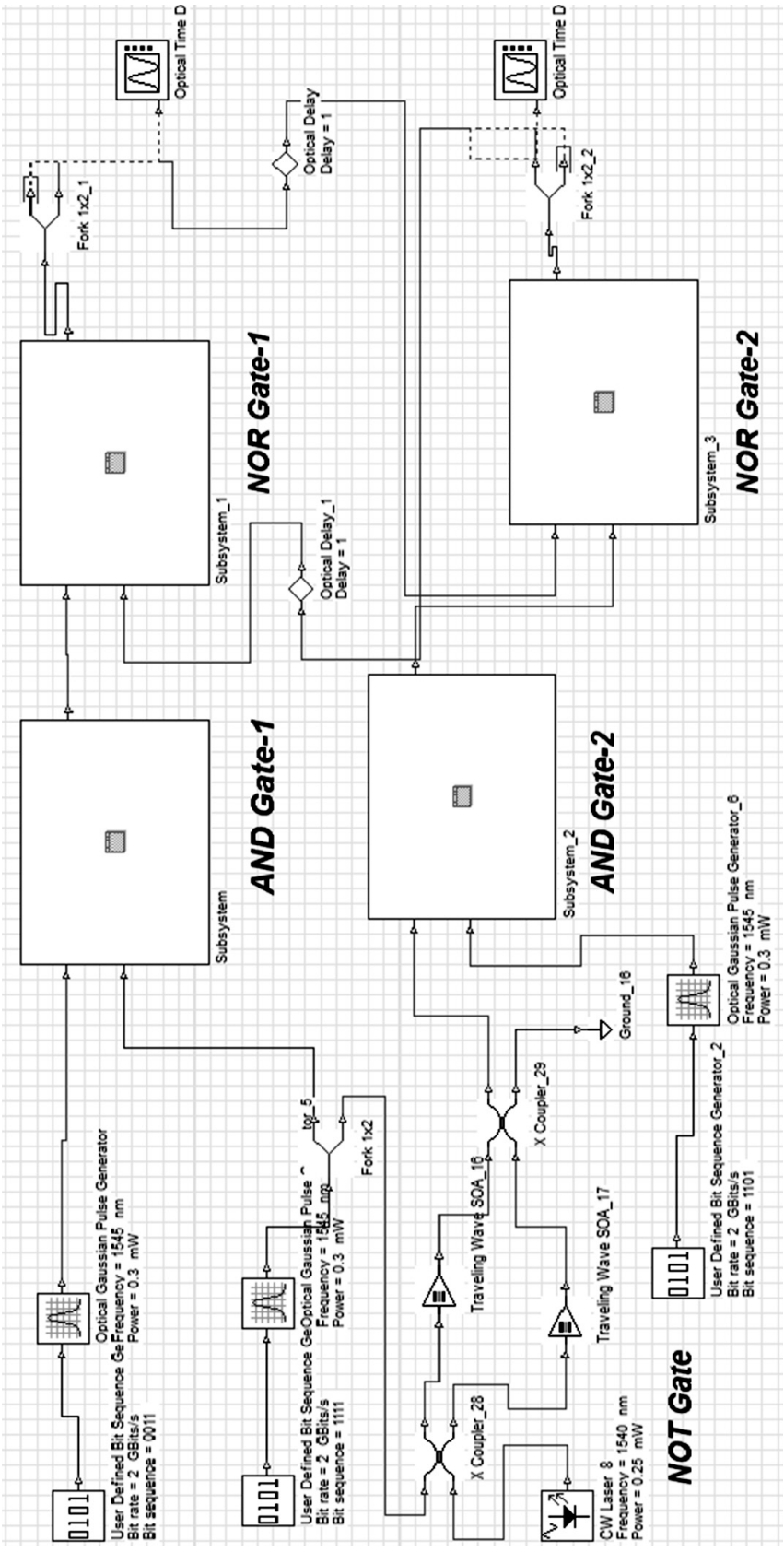

Figure 18: Simulation layout for D-flip-flop

The input sequence 0101 is given to D input of the designe D-flip-flop and the clock signal sequence is 1111. The corresponding optical pulses are shown in Figure 19 and Figure 20.

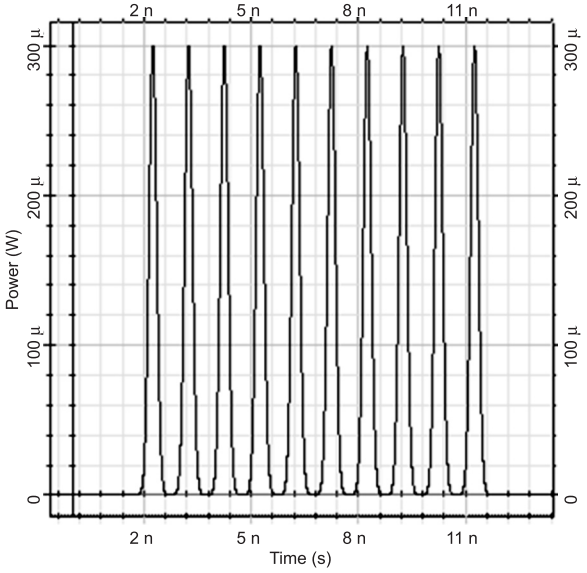

Figure 19: Input D (0101) of D-flip-flop

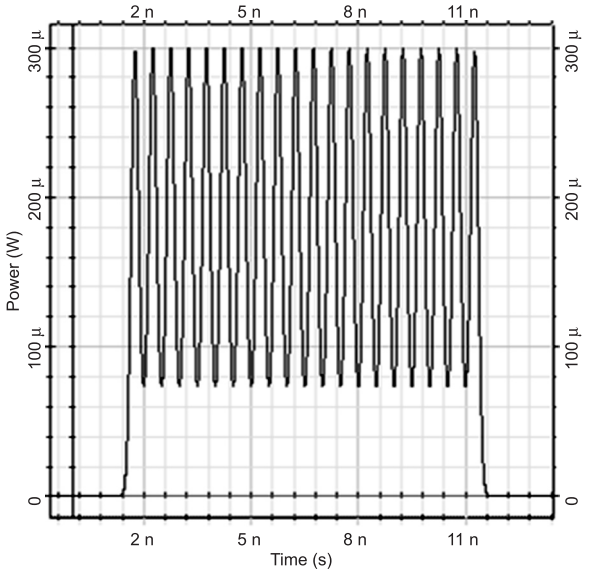

Figure 20: Input clock (1111) of D-flip-flop

The parameters used in simulation work are tabulated in Table 5.

Table 5
Parameters used in simulation work

Parameters	*Values*
Bit rate	2 Gbps
Frequency of CW Laser	194.04 THz
Power of CW Laser	0.25 mw
Frequency of Gaussian pulse Generator	194.6 THz
Power of Gaussian pulse Generator	0.3 mw

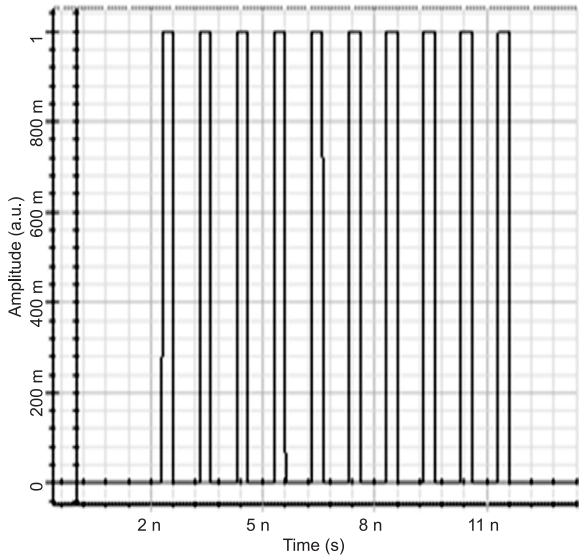

Figure 21: Output for Q in D-flip-flop

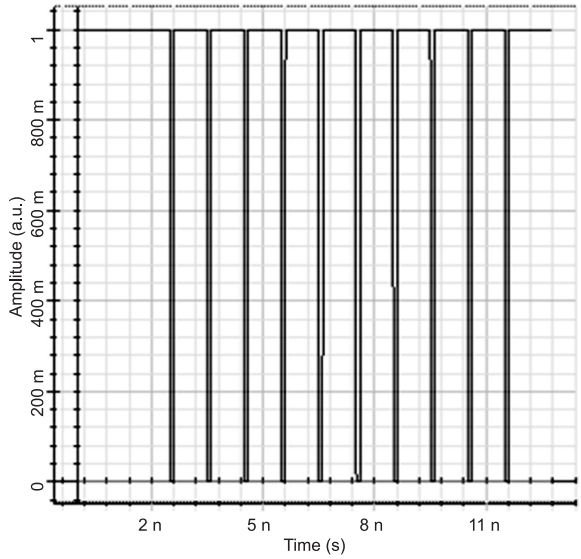

Figure 22: Output for Q′ in D-flip-flop

For the input sequence of D = 0101 and CLK = 1111, the output of D-flip-flop is Q = 0101 and Q′ = 1010. The output sequences are shown in Figure 21 and Figure 22. The complement of output Q is Q′. That outputs can be verified with truth table (Table 1).

The designe D-flip-flop is tested for different higher data rates with injection current of 0.22A. The performance of proposed D-flip-flop is analyzed based on Q-factor and BER which are tabulated in Table 6.

Table 6
Performance Analysis of D-flip-flop for various Data Rate

Bit Rate	*Q Factor*	*BER*
5 Gbps	4.534	$2.759 \times e^{-6}$
20 Gbps	3.96	$2.53 \times e^{-5}$
40 Gbps	4.312	$6.23 \times e^{-6}$
60 Gbps	5.2114	$7.78 \times e^{-8}$

From the performance table, it can be observed that with an increase in data rates till 60Gbps the performance measure Q factor improves. This may be attributed to non-linearity introduced due to the high data rate, since the working of SOA is based on non-linearities. Further improvement can be achieved if the operational parameters of SOA are adjusted.

5. CONCLUSION

Flip-flops being the building block for sequential circuits, designing an All-Optical flip-flop becomes essential to move towards All-Optical signal processing. In this work, D-flip-flop is design and simulated. The operation of D-flip-flop is analyzed at different data rates. The proposed D-flip-flop is capable of operating at high data rate. Further improvements can be made to achieve higher performances.

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