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A Hierarchical Control Approach for Voltage Unbalance Compensation in A Droop–Controlled Micro-Grid

K. Swathi* and K.Bhavana**

Abstract : The smart grid and micro-grid technologies are playing necessary role in power system due to their benefits over traditional utility grid system. In micro grid, control and management has many functions to keep up stability and to boost power quality of the system. In this paper, a hierarchical control is presented which incorporates primary, secondary and tertiary control levels are planned for micro-grids. The primary control level consists of DG's local controllers. Every DG local controller contains active/reactive power droop controllers, voltage and current controllers, virtual impedance loop. The secondary control level is intended to manage the compensation of voltage unbalance at PCC in an islanded micro-grid. Voltage unbalance compensation is achieved by sending proper control signals to the DG's local controllers from secondary controller. This can be achieved by proper control of distributed generators(DG's)interface converters. The design procedure of the system for compensating the voltage unbalance is mentioned thoroughly and also the simulation is done by using MATLAB/SIMULINK.

Keywords : Micro-grid; Distributed generation (DG); Hierarchical control; Voltage unbalance compensation.

1. INTRODUCTION

The smart grid is that the assortment of all technologies, concepts, topologies, and approaches that permit the silo hierarchies of generation, transmission, and distribution to get replaced with an end-to-end, organically intelligent, totally integrated environment wherever the business processes, objectives, and wishes of all stakeholders are supported by the economical exchange of knowledge, services, and transactions. A smart grid is so outlined as a grid that accommodates a large sort of generation choices, *e.g*. central,distributed, intermittent, and mobile. It empowers customers to move with the energy management system to regulate their energy use and scale back their energy prices[1],[2].

Control methods for DER units with in a very micro-grid are selected based on the desired functions and attainable operational eventualities. Controls of a DER unit also are determined by the nature of its interactions with the system and alternative DER units. The most control functions for a DER unit are voltage and frequency control and/or active and reactive power control. moreover, the power electronic interface device (*e.g*., An electrical converter within the case of dc-to-ac conversion) that is commonly accustomed connect the DG's to the electrical system will give many control functionalitie's. In fact, the main role of the DG electrical converter is to regulate output voltage phase angle and amplitude so as to control the active and reactive power injection. However, compensation of power quality issues also can be achieved through correct control ways.

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Among numerous power quality phenomena, voltage unbalances are quite common. Unbalanced voltages may result in adverse effects on equipment and on the power system, that is intense by the very fact that a little unbalance within the phase voltages will cause a disproportionately larger unbalance within the phase currents. under unbalanced conditions, the power system will incur additional losses and heating effects, and be less stable as a result of once the phases are balanced, the system is in a very better position to retort to emergency load transfers. The impact of voltage unbalance can even be severe on equipment like induction motors, power electronic converters and adjustable speed drives (ASD's). Thus, the International Electro-technical Commission (IEC) recommends the limit 2% for voltage unbalance in electrical systems. A major reason behind voltage unbalance is that the uneven distribution of single-phase loads, that will be continuously changing across a three-phase power system [4].

Compensation of voltage unbalance is usually done using series active power filter through injection of negative sequence voltage in series with the power distribution line.But, there are a couple of works based mostly on using shunt active power filter for voltage unbalance compensation. In these works, voltage unbalance caused by unbalanced load is compensated through balancing the line currents. In [5], some approaches are conferred to use the DG for voltage unbalance compensation. A technique for voltage unbalance compensation through injection of negative sequence current by the DG has been projected in [5]. By applying this technique, the line currents become balanced in spite of unbalanced loads presence. However, under severely unbalanced conditions, a large quantity of the interface converter capacity is employed for compensation and it's going to interfere with the active and reactive power provide by the DG.

In this paper the thought of micro-grid secondary control [6] is applied to compensate the voltage unbalance at PCC in an islanded micro-grid. among the proposed control structure, a PI controller is employed to generate the reference of unbalance compensation for the DG's of the micro-grid. This reference is transmitted to the DG local controllers which constitute the primary control level.

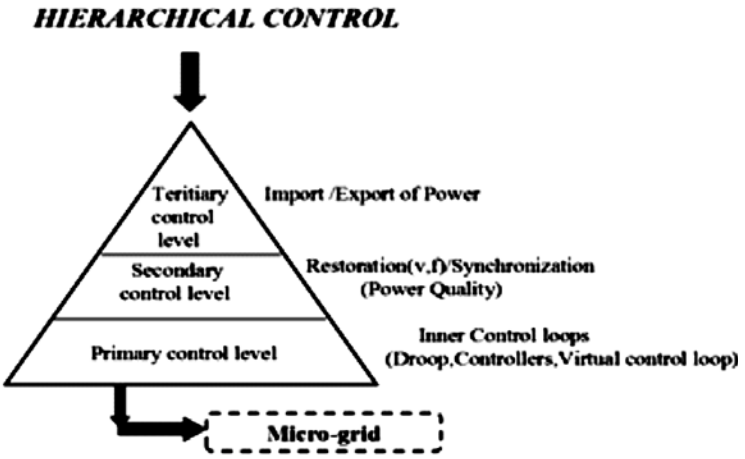
The rest of the paper is organized as follows. The structure of the micro-grid hierarchical control and also the details of secondary level are mentioned in Section-II. Section- III is devoted to the projected DG local control strategy. Section-IV includes simulation results. Finally, the paper is concluded in Section-V.

2. MICROGRID HIERARCHICAL CONTROL SCHEME

The control of the micro-grid could additionally be done based on the autonomous operation of DG's local controllers (decentralized control) or be managed by a central controller (centralized control). The centralized control will be achieved according to a hierarchical control structure that consists of various control levels. A hierarchal control structure consisting of three control levels is projected in [3]. The management levels are native micro-source and cargo controllers (MC/LC), micro-grid central controller (MGCC), and distribution management system (DMS). Once the micro-grid operates in grid-connected mode, MC's follow the commands from the MGCC. In islanded mode, MC's perform local improvement of the DG active and reactive power production, and fast load following. LC's are put in at the controllable loads location and act based on the commands of MGCC. Economic optimization of micro-grid operation considering market conditions and fuel consumption is additionally performed by the MGCC.

It is noteworthy that once the micro-grid operates in islanded mode, the voltage and frequency ought to be supported by the DG's, whereas in grid-connected mode the support is provided by the main grid. Frequency control could be a difficult drawback in islanded operation, since the micro-grid's primarily comprise converter connected inertia-less DG's. However, some virtual inertia may be provided by the facility droop controllers [6].

The hierarchical control theme of [6] is organized in three levels: primary, secondary, and tertiary. the primary control deals with the local control of the DG units. The secondary level is meant to restore the DG's output voltage frequency and amplitude deviations that are created by the power droop controllers and output impedances. The tertiary control level regulates the power exchange between the grid and also the micro-grid [6]. Since, inside the current paper, the micro-grid operates in islanded mode, this control level isn't considered.



The main focus of the current paper is on the voltage quality at PCC. The projected hierarchical control structure and the DG power stage are shown in Figure 1. As seen, the facility stage of every DG consists of a PV module, an interface electrical converter associated an LC filter. Z_{l1} models the distribution line between DG1 and PCC. For simplicity, only the power stage and tie line of DG1 are represented. The other micro-grid DG's have identical power stage, but, is connected to PCC through completely different line impedances.

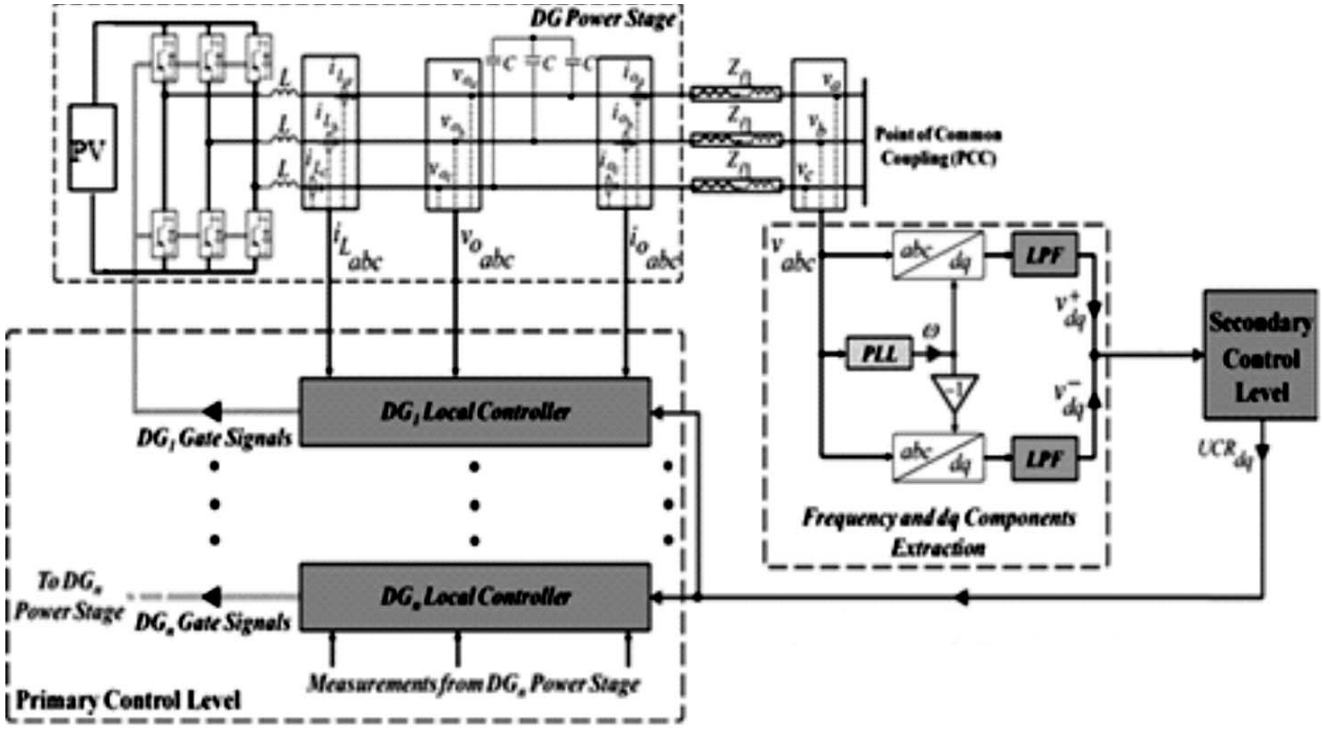


Fig. 1. Power stage and hierarchical control scheme.

As seen in Figure 1, the local controllers generate the gate signals for DG's interface inverters. The local controller of every DG consists of voltage and current controllers, virtual impedance loop, and active/reactive power droop controllers. additional details are provided within the next section.

The secondary controller manages the unbalance compensation of micro-grid PCC voltage by sending correct control signals to the DG's local controllers. As shown in Figure 1, micro-grid angular frequency (ω)is estimated by a phase-locked loop (PLL) block. Then, so as to extract PCC voltage positive and negative sequences, v_{abc} is transformed to dq reference frames rotating at the speeds ω and –ω , respectively.

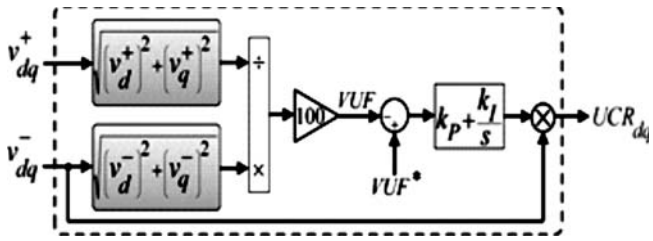


Fig. 2. Block diagram of secondary control level.

3. DG INVERTER LOCAL CONTROL SYSTEM

The DG local control system shown in Figure 3 is designed in αβ reference frame. So, Clarke transformation is used to transform the variables between abc and αβ frames.

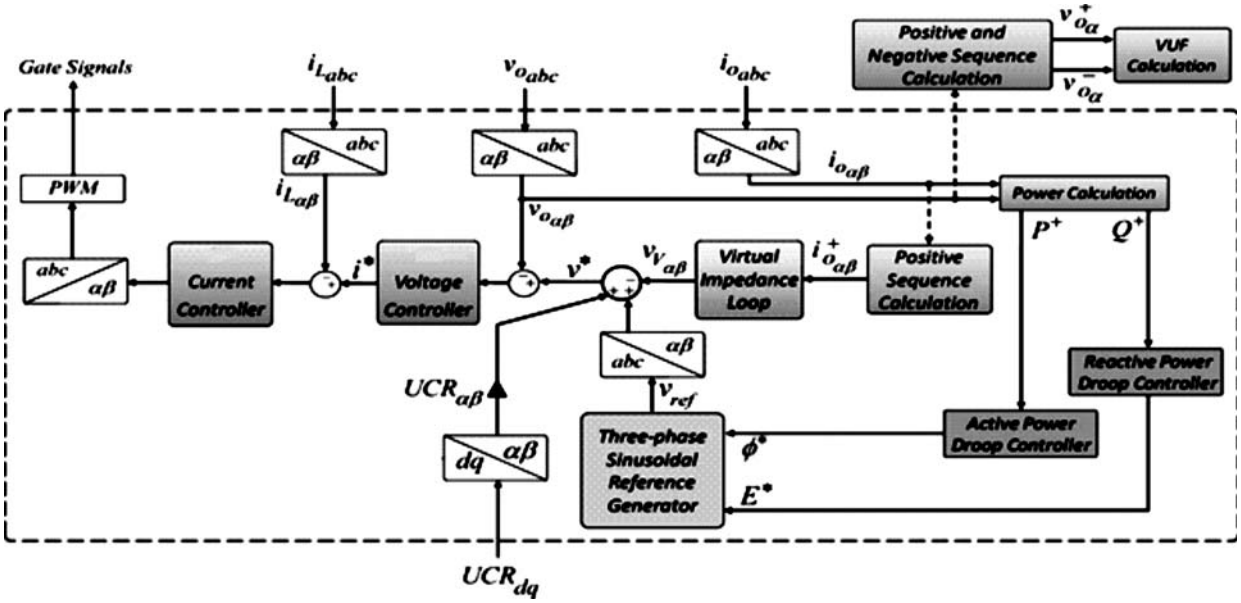


Fig. 3. Schematic diagram of DG local controller.

As shown in Figure 3, the voltage controller follows the references generated by power controllers and secondary level to generate the reference for the current controller. The output of the current controller is transformed back to abc frame to provide three-phase voltage reference for the pulse width modulator (PWM). Finally, the PWM block controls the switching of the inverter based on this reference. More details are provided in the following subsections.

A. Active and Reactive Power Control

Active and reactive powers may be controlled by the DG output voltage phase angle and amplitude,respectively. According to this, the subsequent droop characteristics are applied for the positive sequence active and reactive power sharing among DG's in an islanded micro-grid.

$$\phi^* = \frac{\omega^*}{s} = \frac{1}{s}[\omega_0 - (m_p + m_D{}^S)P^+] \quad (1)$$

$$E^* = E_0 - npQ^+ \quad (2)$$

Where,

1. s : Laplace variable;
2. E_0 : rated voltage amplitude;

3. ω : rated angular frequency;
4. P^+ : positive sequence active power;
5. Q^+ : positive sequence reactive power;
6. m_P : active power proportional coefficient;
7. m_D : active power derivative coefficient;
8. n_p : reactive power proportional coefficient;
9. E^* : voltage amplitude reference;
10. ϕ^* : voltage phase angle reference;
11. ω^* : angular frequency reference.

As can be seen in Figure 3, E^* and ϕ^* are used to generate the three phase reference voltage(v_{ref}) . This voltage is positive sequence component; thus, positive sequence powers (P^+ and Q^+) are used in (1) and (2). According to Figure 3, at first DG three-phase output voltage and current (v_{0abc} and i_{0abc} , respectively) are measured and transformed to αβ frame ($v_{0\alpha\beta}$ and $i_{0\alpha\beta}$, respectively). Then, positive and negative sequences of output voltage and positive sequence of output current are extracted [8]. Positive sequence current is fed to the virtual impedance block. Also, positive and negative sequences of output voltage are applied for VUF calculation. The details of this calculation are shown in Figure 4.

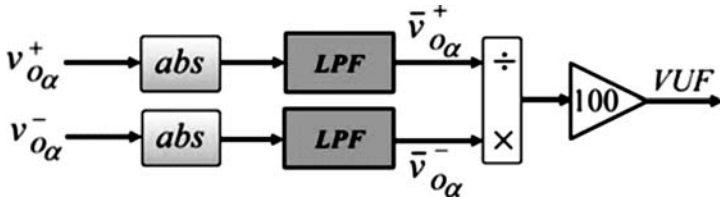


Fig. 4. Block diagram of VUF calculation in αβ frame.

As can be seen,α-components of DG output voltage positive and negative sequences are fed to VUF calculation block. Then, the average values of rectified wave-forms ($v_{0\alpha}^+$ and $v_{0\alpha}^-$) are calculated by applying two absolute functions (abs) and low-pass filters (LPF). LPF structure and parameters are exactly same as (1). Finally, calculation of VUF is done by division of $v_{0\alpha}^+$ and $v_{0\alpha}^-$.

B. Power Calculation

Based on the instantaneous reactive power theory [9], the instantaneous values of active and reactive powers should be calculated using (3) and (4), respectively:

$$p = v_{0\alpha}.\, i_{0\alpha} + v_{0\beta}.\, i_{0\beta} \quad (3)$$

$$q = v_{0\beta}.\, i_{0\alpha} - v_{0\alpha}.\, i_{0\beta} \quad (4)$$

C. Virtual Impedance Loop

Addition of the virtual resistance makes the oscillations of the system a lot of damped [7]. In distinction with physical resistance, the virtual resistance has no power losses, and it's attainable to implement it without decreasing the efficiency. Also, the virtual inductance is taken into account to make sure the decoupling of P and Q . Thus, virtual electric resistance makes the droop controllers a lot of stable. The virtual impedance will be achieved as shown in Figure. 5,where and are the virtual resistance and inductance, respectively. According to this figure, the subsequent equations are extracted.

$$v_{V\alpha} = R_v . i^+_{0\alpha} - L_v . \omega . i^+_{0\beta} \quad (5)$$

$$v_{V\beta} = R_v . i^+_{0\beta} + L_v . \omega . i^+_{0\alpha} \quad (6)$$

As shown in Figure 3, only positive sequence current is passing through virtual impedance. during this approach, increase of DG output voltage unbalance due to the negative sequence voltage drop on the virtual impedance are going to be avoided.

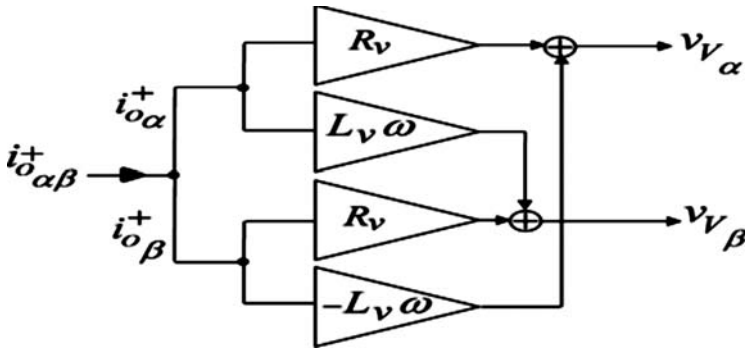


Fig. 5. Virtual impedance block diagram.

D. Voltage and Current Controllers

PI voltage and current controllers

The PI controller provides an infinite gain with a continuing variable, it get a fast response to a step reference without steady-state error, however is unable to trace a sinusoidal reference .In this paper, PI voltage and current controllers are as follows.

$$G_V(s) = k_{pV} + \frac{k_{iV}}{s} \tag{7}$$

$$G_I(s) = k_{pl} + \frac{k_{il}}{s} \tag{8}$$

where, kpV(K_pI) and k_iV(k_iI) are the proportional and integral coefficients of the voltage (current) controller, respectively.

PR voltage and current controllers

Due to the difficulties of using PI controllers to trace non-dc variables, proportional-resonant (PR) controllers are sometimes preferred to control the voltage and current within the stationary reference frame [10]. During this paper, PR voltage and current controllers are as (9) and (10)

$$G_V(s) = k_{pV} + \frac{2k_{rV}\cdot\omega_{cV}.s}{s^2 + 2\omega_{cV}\cdot s + \omega_0^2} \tag{9}$$

$$G_I(s) = k_{pI} + \frac{2k_{rI}\cdot\omega_{cI}.s}{s^2 + 2\omega_{cI}\cdot s + \omega_0^2} \tag{10}$$

Where, kpV(K_pI) and k_rV(K_rI) are the proportional and resonant coefficients of the voltage (current) controller, respectively. Also, ω_{cV} and ω_{cI} represent the voltage and current controller cut-off frequencies, respectively.

4. SIMULATION RESULTS

An islanded micro-grid of Figure. 6 is considered as the test system. This micro-grid includes two DG's with power stage and control system shown in Figures. 1–3. Power stage and control system parameters are listed in Tables I and II,III, respectively. Switching frequency of the DG's inverters is set to 10 kHz. As seen in Figure. 6 a single-phase load(Z_{UB}) is connected between phases "*a*" and "*b*"which creates voltage unbalance. A balanced star-connected three-phase load (Z_B) is also connected to PCC. In this figure, Z_{l1} and Z_{l2} represent the distribution lines between DG's and PCC. Unbalance compensation starts acting from t = 0.5 sec in case of PI and t = 0.2 sec in case of PR controllers VUF* is set to 0.5%.

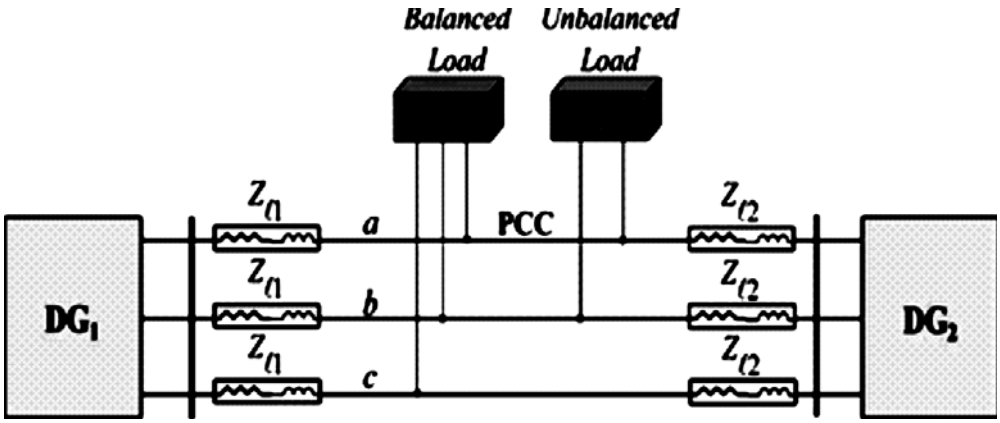


Fig. 6. Test system of simulation studies.

Table 1.

PV parameters	*Value*	*Booster converter*	
Short-circuit current, Isc	3.8A	Parameter	Value
Open-circuit voltage, Voc	21.1V	L	5μH
Irradience	800W/m2	C	50mF
Series resistance,Rs	0.01Ω	R	2.109Ω
Power output	200kW	Duty cycle	0.4

Table 2.

Inverter filter inductance	*Inverter filter capacitance*	*DG1 distribution line*	*DG2 distribution line*	*Unbalanced load*	*Balanced load*
L(mH)	C(F)	Zl1(Ω)	Zl2(Ω)	ZUB(Ω)	ZB(Ω)
1.8	25*e*-6	0.6 + *j*1.6965	0.2 + *j*0.5655	600	50 + *j*12.57

Table 3.

Primary control level							*Secondary control level*	
Power controllers					*Virtual Impedance*		*PI controller*	
m_d	m_p	n_p	E_0	ω_0	R_v (Ω)	L_v(mH)	K_p	K_i
0.00002	0.00002	0.13	230√2	2Π*50	1	4	0.5	7

PI Voltage controller		*PI Current controler*	
k_pV	K_iV	K_pI	K_iI
2	100	2	500

PR Voltage controller			PR current controller		
k_pV	k_iV	ω_{cv}	k_pI	k_iI	ω_{ci}
2	100	2	2	1000	2

The simulation layout of test system with hierarchical control system is as shown in figure. 7

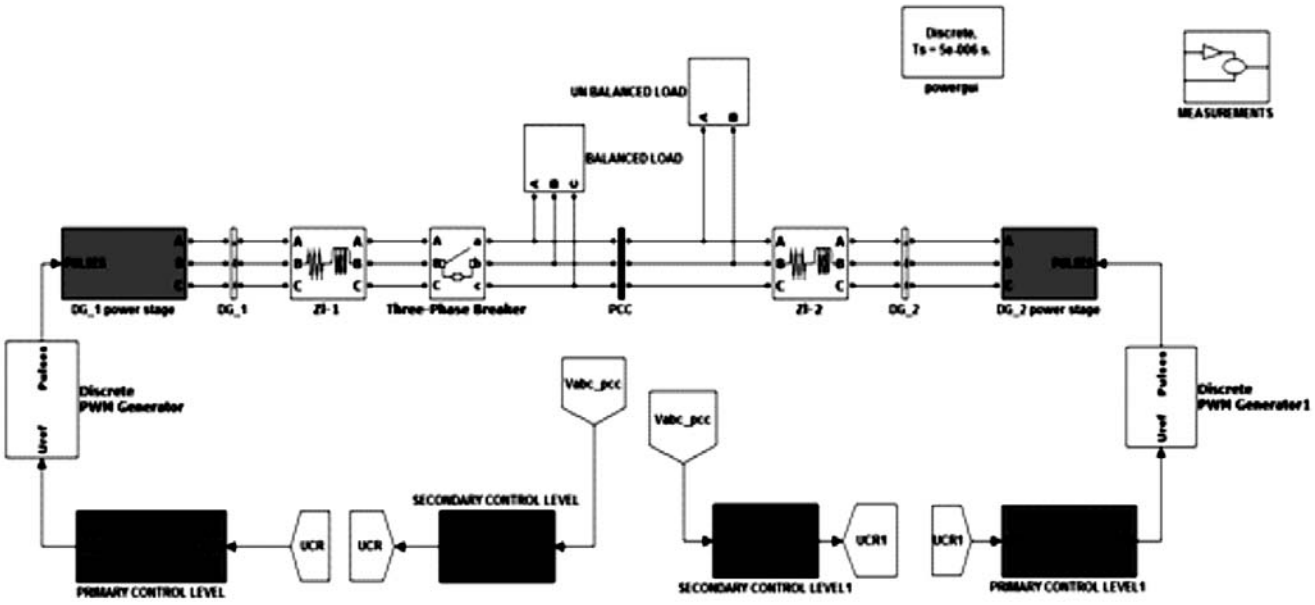


Fig. 7. Simulation diagram of hierarchical control system.

The simulations output of DG power (PV), voltage and DC booster output voltages are shown in figure 8(*a*), 8(*b*), 8(*c*) respectively.

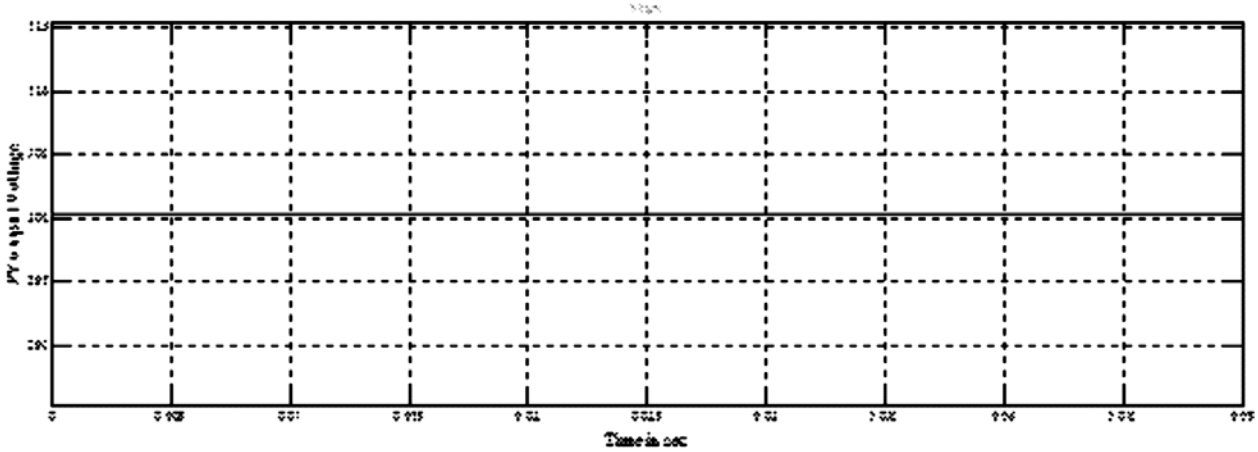


Fig. 8(*a*). PV output power.

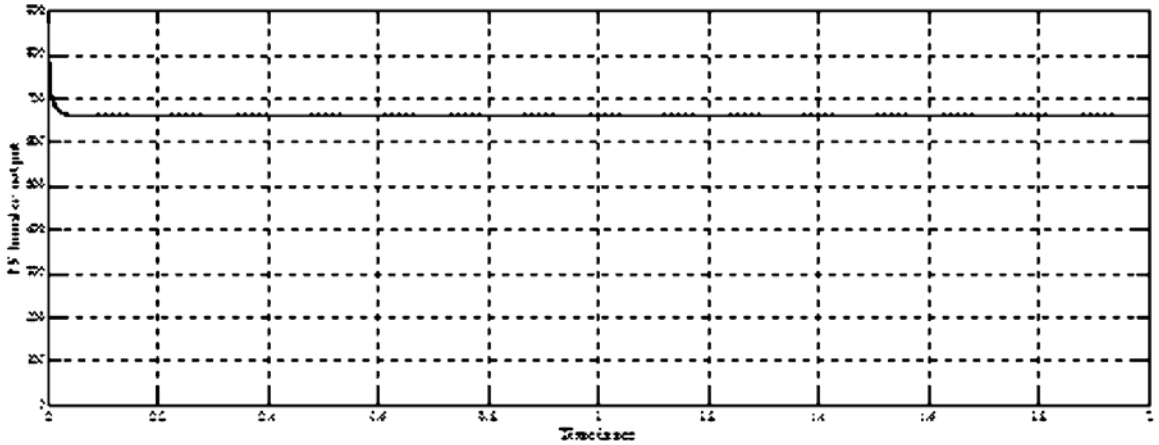


Fig. 8(*b*). PV output voltage.

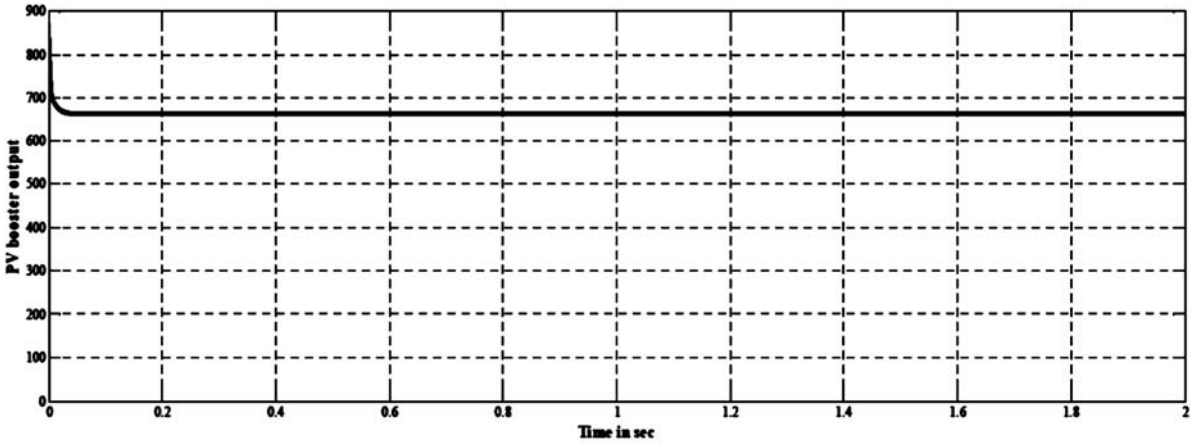


Fig. 8(*c*). Booster output voltage.

To provide more details,the simulation results of PCC voltages before compensation and after compensation with PI and PR controllers are shown in following figures 9(*a*), 9(*b*), 9(*c*).

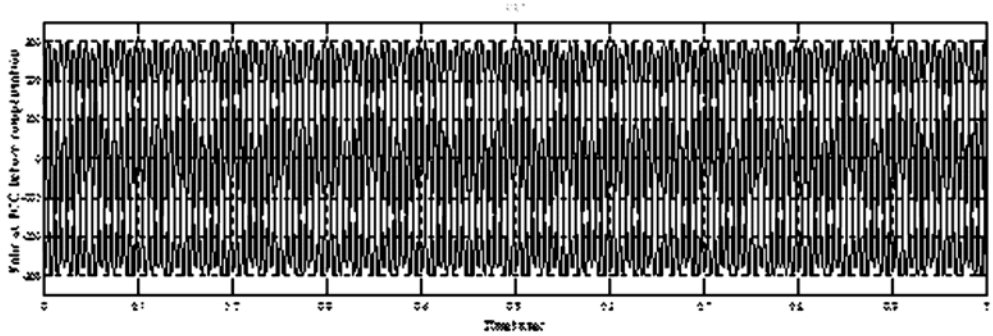


Fig 9(*a*). Voltage at PCC before compensation.

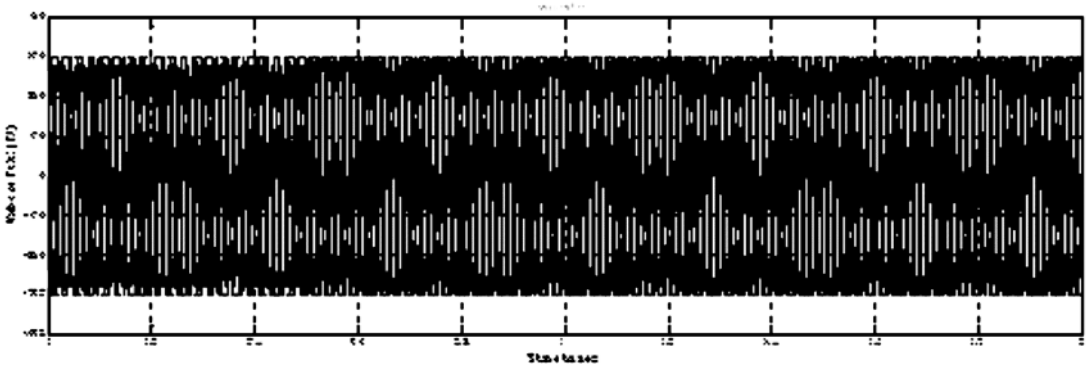


Fig 9(*b*). Voltage at PCC after compensation with PI.

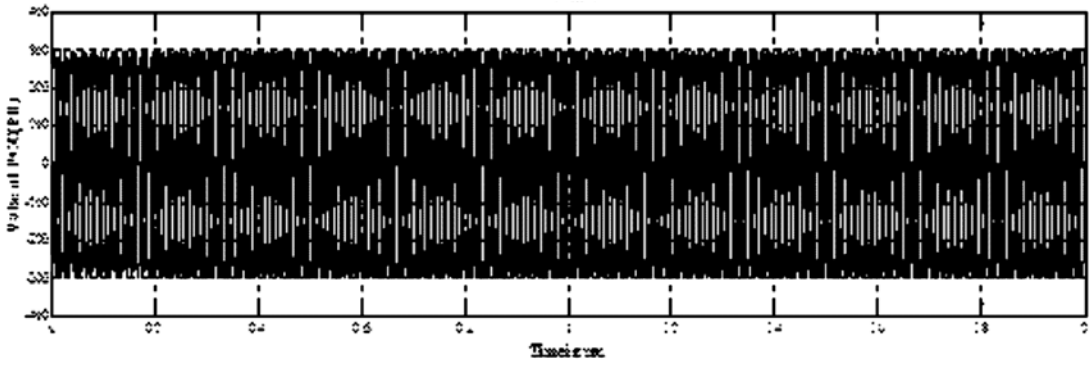


Fig. 9(*c*). Voltage at PCC after compensation with PR.

The simulation results of PCC negative sequence voltages in case of PI and PR controllers are shown in figures 10(*a*),10(*b*). As seen PCC negative sequence voltage is decreased when compensation starts.

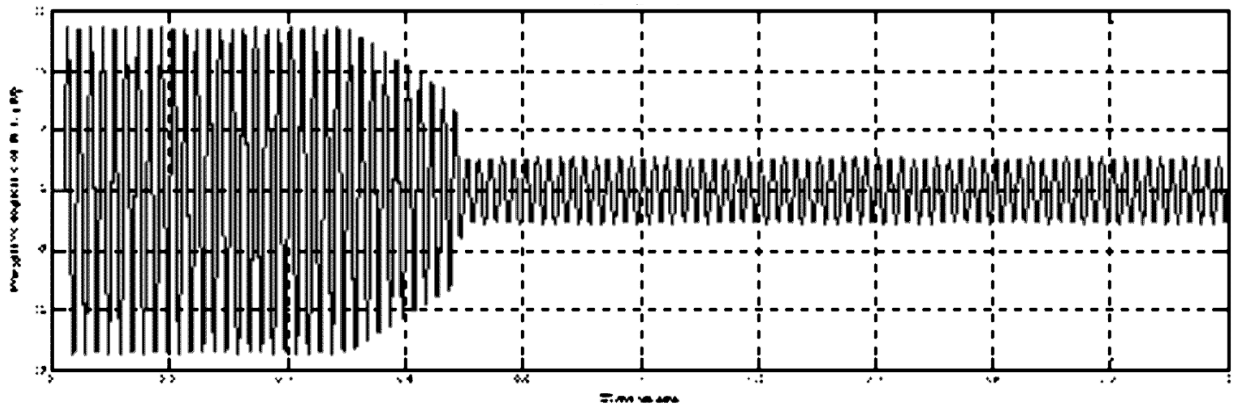


Fig. 10(*a*). Negative sequence voltage at PCC with PI.

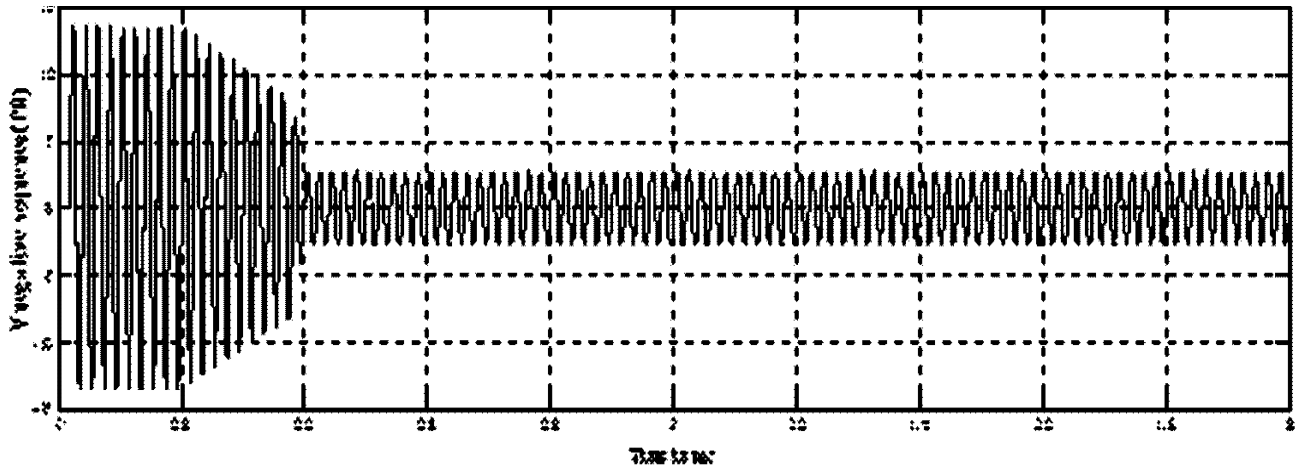


Fig. 10(*b*). Negative sequence voltage at PCC with PR.

As shown in Figure.11(*a*),11(*b*) VUF of PCC follows the reference value,properly in both the cases *i.e*.,PI and PR controllers. Also, it can be seen that the improvement of PCC voltage quality is achieved by sending proper compensation reference signal's to the DG inter phased inverter.

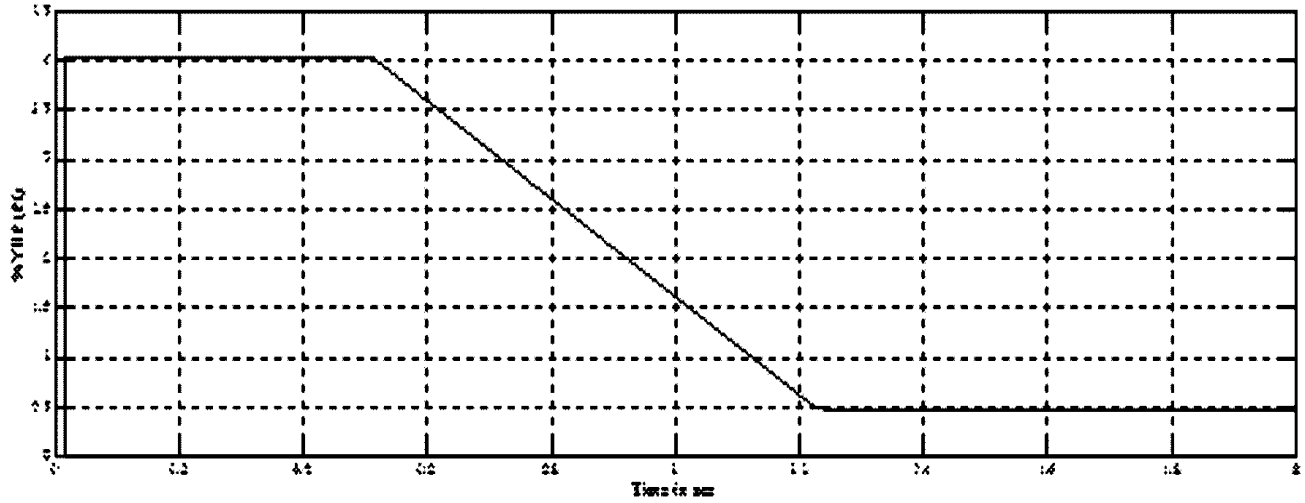


Fig. 11(*a*). VUF at PCC with PI.

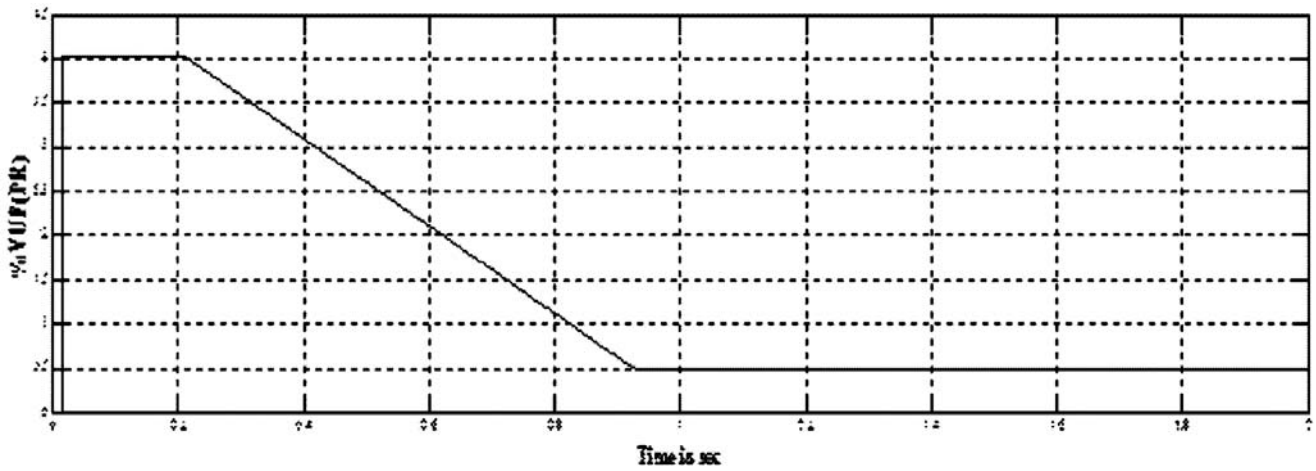


Fig. 11(*b*). VUF at PCC with PR.

5. CONCLUSION

A hierarchical control approach for PCC voltage unbalance compensation in an islanded micro-grid is projected. The control structure consists of DG's local controllers (primary level), and a central secondary controller. The secondary controller manages PCC voltage unbalance compensation by sending proper control signals to the primary level. The presented simulation results show that the PCC voltage unbalance is compensated to the desired value in case of both PI and PR controllers.

6. REFERENCE

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