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Design of Robust, Ultra Low-Power Efficient Full Adder Cell in sub-45nm Technologies

Gangadhar Reddy Ramireddy* and Yash Pal Singh**

ABSTRACT

Nowadays, there is a need to design microelectronic circuits which utilizes less energy and small area because of extensive growth of portable devices like laptops, digital watches and personal communication devices like mobile phones, and continuous shrinking of technology node. Many applications require circuits of high throughput, small area and consume ultra-low power. In this regard, this paper brings forward a novel full adder circuit that uses 10-Transistors and improved version of the proposed circuit. This full adder uses low power XOR gates to generate sum signal and a multiplexer of two transistors, to generate carry out signal. Generic Process Design Kit (GPDK) 45nm technology is employed in Cadence virtuoso design environment to design circuits which are simulated with Spectre simulator.

Keywords: LP XOR/XNOR Gates, Full Adder

1. INTRODUCTION

Full adder cell plays a key role in performing arithmetic operations in arithmetic logic unit in which operations of different types such as subtraction, division, shift operations etc. will occur. Signal processing circuits use the full adder cell as a key element to perform basic operations such as multiplications and additions of signals in digital filters. Data path of a state machine circuits uses full adders extensively for basic operations. The importance of the full adder cell is extended to microprocessors too for generating address. In view of the above theory, one can understand the importance of full adder cell. Hence, it is definitely worth to design a full adder cell with minimum number of transistors and rail to rail logic levels at output node. For the Systems which depend on arithmetic circuits, the performance shall improve by improving the performance of full adder cell.

Further organization of the paper is as follows. Section 2 discusses about the various full adder cells present in literature, which use less than 15 transistors for the design. Proposed novel 14 transistor full adder cell is discussed in Section 3. Simulation results are presented in Section 4, and finally conclusion has been given in the last section.

2. STATE OF THE ART OF 1-BIT FULL ADDER

For the last three decades, full-adder cells had designed with static CMOS logic styles and dynamic logic styles. Different logic styles like traditional Complementary Metal oxide Semiconductor(CMOS) style, Complementary Pass Transistor Logic(CPL), transmission gate logic, double pass transistor logic, Transmission Gate Logic (TGL) used in implementing Full-adder functionality. Full adder implemented with static CMOS logic style is the basic cell is the basic cell designed with 28 transistors. In addition complementary pass transistor logic style full adder provides output with less delay. However, the disadvantage comes with two NMOS logic networks (One for each signal rail) and more number of nodes and high wiring complexity. The advantage of a full adder designed with Double Pass Transistor Logic

* Department of Electronics and Communication Engineering Sunrise University, Alwar, Rajasthan, India, *Email: rgangadharreddy@outlook.com*

** Department of Electronics and Communication Engineering Sunrise University, Alwar, Rajasthan, India, *Email: ypsingh10@rediffmail.com*

(DPL) is, it provides full swing at the output node. The more power consumption due to large PMOS transistors limits the usage of DPL logic circuits. Reto Zimmermann and Woltgang Fichtner had done the work to find which logic style is better, and they had also presented the comparison of different logic styles [1]. It is explained how a full adder is designed with different logic styles like Complementary Metal oxide Semiconductor (CMOS), Pass Transistor Logic etc. Each design with a logic style has its own advantages and disadvantages. Suppose if we take a full adder designed with CMOS logic style, the circuit performs better at all nodes. It gives good output voltage swing but the main flaw is the number of transistors (28) required to build full adder. At lower technology nodes this cell consumes more power and area.

In modern days, double gate (FinFET) MOSFETS and carbon nanotube devices have come into picture to design full adder cells. The advantage of double gate transistor is, it provides better control over the channel. Because of this we can minimize gate leakage currents in a transistor. Carbon nanotubes have very large current density, which is even greater than metal conductors like copper. So when full adder designed with FinFETS or Carbon nanotubes, it shows better performance. But the main challenge present before the VLSI engineers is the lithography process of making a FinFET and carbon nanotubes [2], [3].

In this paper, we have considered eight 1-bit full adders from literature to compare with the proposed circuits. All these eight full adder circuits use less than 15 transistors to obtain full adder functionality. A 6-

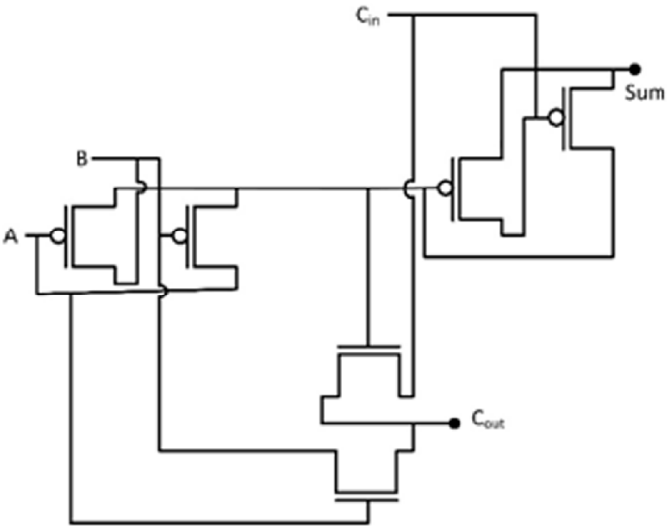

Figure 1: 6-T Fulladder[4]

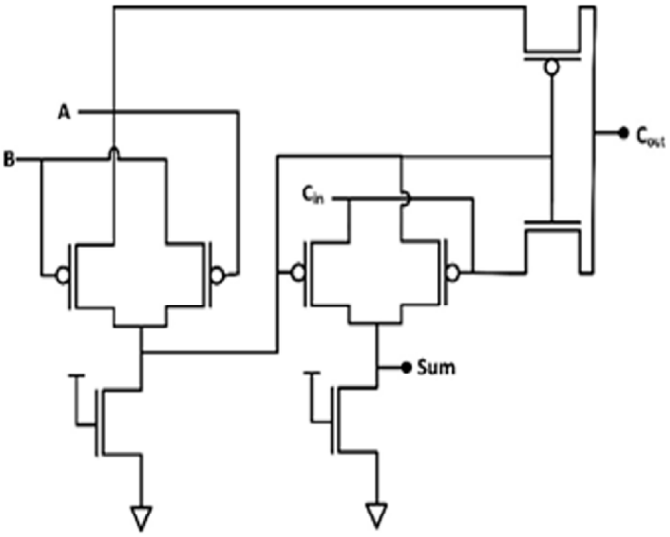

Figure 2: 8-T Full adder[5]

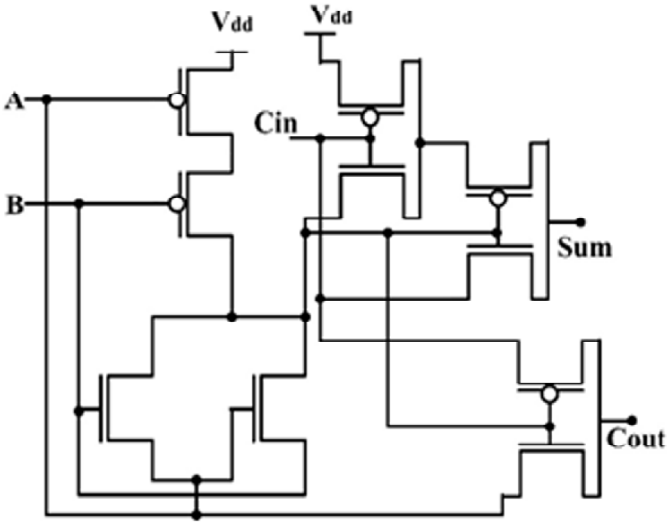

Figure 3: 10-T FullAdder-1[6]

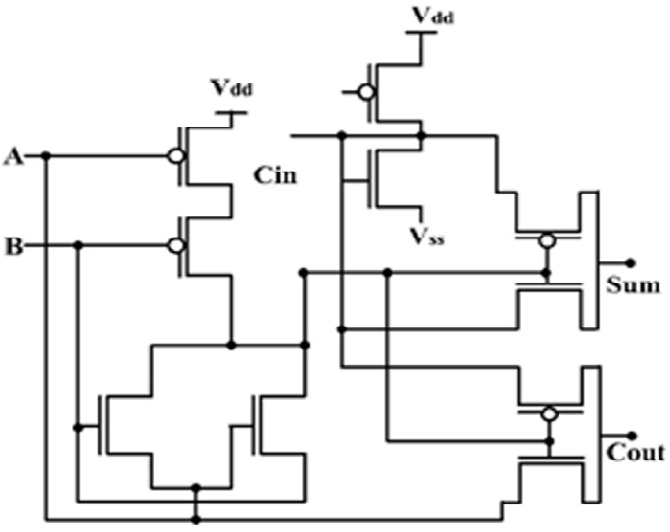

Figure 4: 10-T Full Adder-2[6]

transistor full adder was designed with the aid of two novel transistor XOR Gates [4]. The 6-transistor is shown in Fig. 1. Fig. 2 shows an 8-transistor full adder [5]. From [6], two 10-transistor circuits are taken and these two 10-transistor full adders are shown in Fig. 3 and Fig. 4.

R. Shalem et al. proposed a low count 10 transistor full adder, named Static Energy Recovery Full adder (SERF) [7]. SERF adder is shown in Fig. 5. Latter a new full-adder circuit using double gate FinFET transistor and Gate Diffusion Input (GDI) technique [8]. Fig. 6 depicts a 10 Transistor full adder designed with GDI technique. In [6], authors proposed 14-Transistor full-adder-1 and is depicted in Fig. 7. Fig. 8 represents 14T full adder-2 [9]. This full adder cell uses novel XOR, XNOR gates and transmission gates to generate the sum and carry out with 14 transistors half of the PMOS and another half NMOS.

3. PROPOSED METHOD

The full adder functionality can be represented in many ways so far in literature. The logic function for the newly proposed full-adder is represented as

$$Sum = \overline{C_{in}}(A \oplus B) + C_{in}(A \square B) \quad (1)$$

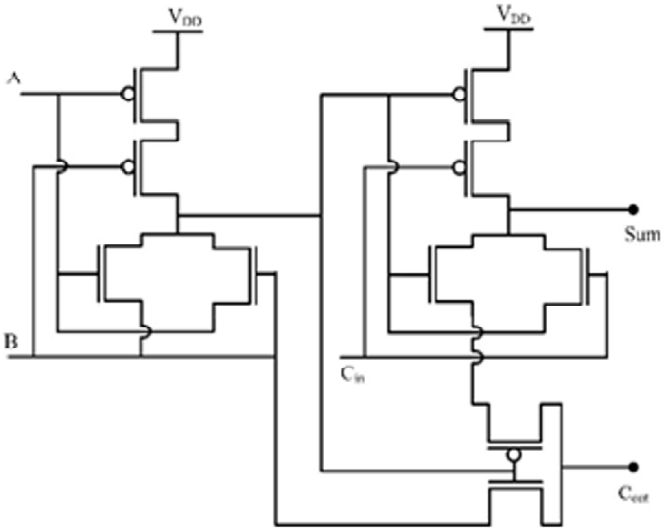

Figure 5: Static Energy-RecoveryFA[7]

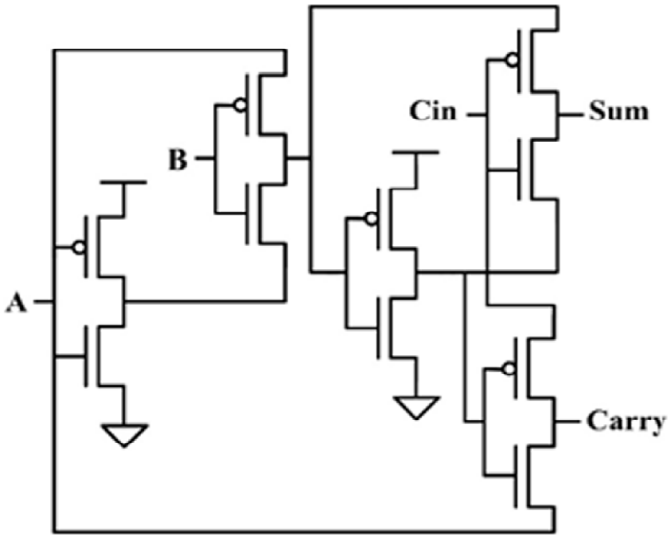

Figure 6: 10-T GDI Logic FA[8]

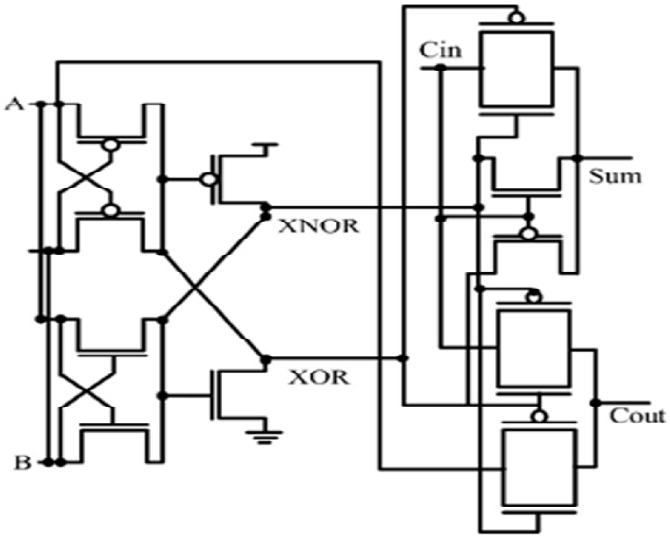

Figure 7: 14 TFA-1[6]

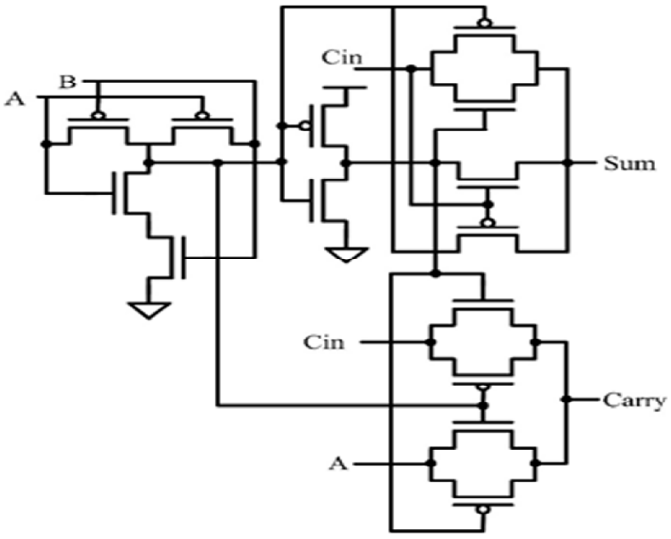

Figure 8: 14 T FA-2[9]

$$Carry = (A \oplus B)C_{in} + (A \square B)A \quad (2)$$

Eq. (1) can be implemented with two Low Power (LP) XOR/XNOR gates which are proposed in [10]. Eq. (2) can be implemented with a 2 to 1 multiplexer, implemented with two transistors one is NMOS and another is PMOS, this is possible of complementary control signal which are intermediate signals XOR/ XNOR.

Based on the logic expressions in Eq. 1 & 2, the 1-bit full adder can be implemented with only 10 transistors. The proposed 10 transistor full adder is depicted in Fig. 9. This circuit requires only non-complementary inputs. A and B input signal are applied to the first XOR gate. The output of the first XOR gate is $A \oplus B$. This signal is applied to the second XOR gate along with Carry input signal. The output of the second XOR gate is $A \oplus B \oplus C_{in}$. So, sum signal is obtained at the output node of second XOR gate. Now, we will analyze the operation for carry out signal. By analyzing the truth table of 1-bitfull adder, the following conclusions can be drawn.

- When the $A \oplus B$ signal is high, carry out signal follows the carry in signal.
- When $A \oplus B$ signal is low, carry out signal follows input A or B signal.

By using this property, a multiplexer is used to implement it. $A \oplus B$ Signal is given as a control signal to the multiplexer. Single NMOSFET and single PMOSFET are used to form a multiplexer gate. For this multiplexer one input is carry in signal and it is applied to NMOSFET, another is A signal and it is applied to PMOSFET. The output of the multiplexer is carry out signal.

So, only 10 transistors are required to construct the novel full adder circuit. The problem with the proposed 10 transistor full adder cell is that at the output node, full rail to rail logic levels are not appearing. This is because of the two transistor multiplexer, is providing output voltages with the loss of Vth. So, to get the complete voltage swing at output node, transmission gate logic is used. In this way, the loss of threshold voltage at output can be eliminated. The designed full adder is named as the proposed novel 14T full adder and it is depicted in Figure 10. The authors in [11] have done a comparison of different types of XOR/XNOR gate in literature with the Low Power (LP) XOR/XNOR gates in terms of leakage power.

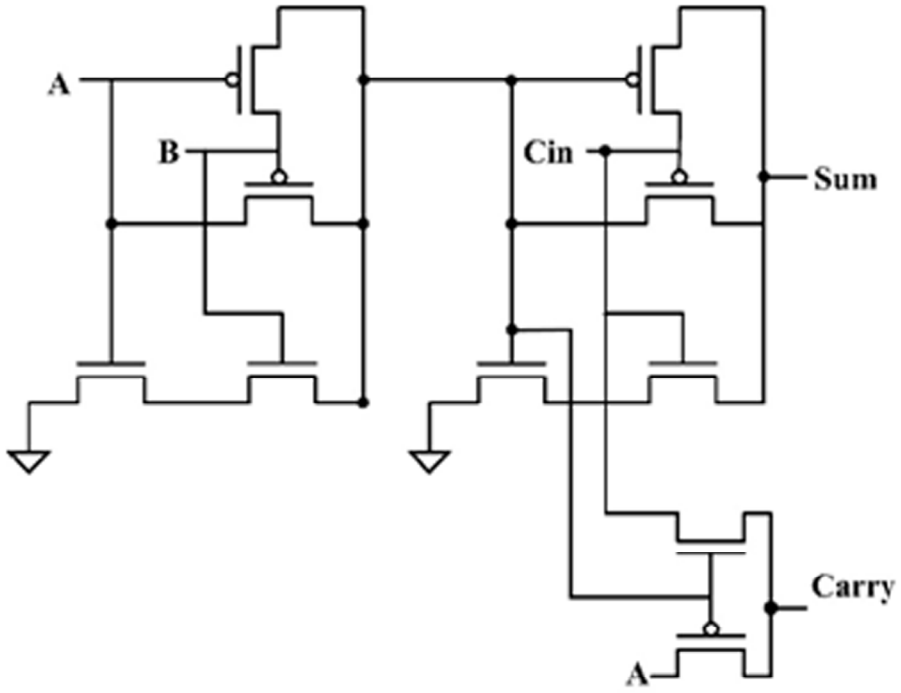

Figure 9: Proposed novel 10T Full adder

This study has shown that the leakage power of LP XOR/XNOR gate is the lowest. Leakage power is the dominating factor in power consumption at sub-micron technologies. So, in this work LP XOR/XNOR gates are used to design the full adder circuits.

4. SIMULATION RESULTS

All designed circuits in this paper are simulated using Spectre simulator in Virtuoso Design Environment provided by Cadence Software. Designed circuits are captured using Generic Process Design Kit (GPDK) and 45nm technology transistor models are used. Simulations are done under GPDK45nm technology file provided by the Cadence Design Systems. The input combinations are taken from 000 to 111 and the simulation time is 20ns.

Furthermore, Table 1 gives the information of different types of full adders presented in this paper and also shows with which logic style each full adder is designed. Most of the full adders in this work considered

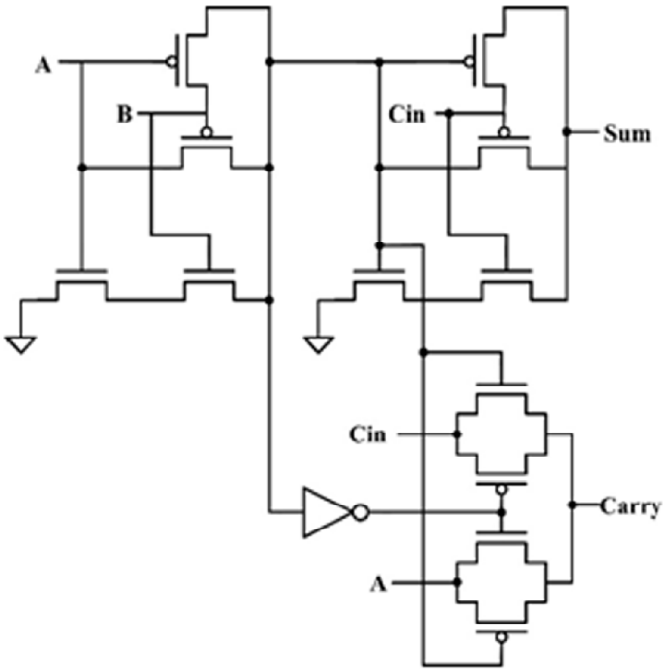

Figure 10: Modified novel 10T Full Adder (Proposed novel Full Adder 14T Full Adder)

Table 1
Features of Full adder designs under comparison

Full-Adder	*# of Transistors*	*Circuit Type*	*Voltage Swing*
6-T FA	6	PTL	Degraded
8-T FA	8	PTL	Degraded
10-T FA-I	10	PTL	Degraded
10-T FA-II	10	PTL	Degraded
GDI 10-T FA	10	GDI Logic	Degraded
14-T FA-I	14	PTL+TG	Full
14-T FA-II	14	PTL	Full
SERF	10	PTL	Degraded
Proposed 10-T FA	10	PTL	Degraded
Proposed 14-T FA	14	PTL+TG	Full

PTL - Pass Transistor Logic, TG - Transmission Gate Logic, GDI- Gate Diffusion Input

are which are designed with pass transistor logic. Based on the simulation results and waveforms obtained, it can be mentioned that the 6-T, 8-T, 10-T FA-I, 10-T FA-II, full adder designed with GDI logic, and self-energy recovery full adder circuits give degraded carry out and sum signals at output. 14-T FA-I and 14-T FA-II along with, the two proposed full adders with low power XOR gate and pass transistors give full swing at output node. In the proposed full adder, if we observer the carry out structure, the carry out signal is coming from the output of a pass transistor. NMOS FET has week one characteristic and PMOS FET has week zero characteristic, so the output is a degraded signal.

Table 2 presents the simulation results of all 1-bit full adders considered in this work. From Table 2 it can be analyzed that the proposed 10 Transistor full adder gives better power delay product figure than that given by other full adder circuits. Next to proposed 10 transistor full adder proposed 14 transistor full adder gives better performance. Transistor count of the adders is checked in order to investigate their impact on power dissipation of a circuit. Even though a circuit is designed with less number of transistors, the output may be degraded This can be observed for the case of 6T 1-bit full adder cell.

Supply voltage variations cause delay uncertainty. It is very important issue in high performance VLSI circuits and some system design use multi supply voltages (voltage islands) in order to minimize the power. So, it is an essential task to verify the circuit behavior at lower supply voltages. Average power and delay values of proposed 14 transistor and 10 transistor full adders at different supply voltages are tabulated in Table 3 and Table 4 respectively.

Temperature fluctuations varies with the threshold voltage, carrier mobility, and saturation velocity of a MOSFET. Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for

Table 2
Simulation results of various full-adders

Full Adder	*Average Power(nW)*	*Delay(pS)*	*PDP(×10–17 J)*
6-T FA	1000	18	1.8
8-T FA	1500	58	8.7
10-T FA-I	104	144	1.4976
10-T FA-II	113.9	191	2.175
GDI 10-T FA	113	125	1.4125
14-T FA-I	156.5	20	3.12
14-T FA-II	146	149	2.175
SERF	70	50	0.35
Proposed 10-T FA	85	20	0.17
Proposed 14-T FA	**118**	**23**	**0.27**

Table 3
Simulation result of proposed 14-T Full adder at Various Supply Voltages (V_{dd})

Vdd(V)	*Average Power(nW)*	*Delay(pS)*	*PDP(×10–17 J)*
1.4	205.1	14	0.287
1.3	187.1	17	0.3179
1.2	139.1	20	0.2782
1.1	118	23	0.27
1	101	24	0.2424
0.9	87.74	32	0.2808
0.8	81.82	40	0.32728
0.7	119.1	48	0.57168

Table 4
Simulation result of Proposed 10-T Full adder at Various Supply Voltages (Vdd)

V_{dd}(V)	*Average Power(nW)*	*Delay(pS)*	*PDP(×10–17 J)*
1.4	379	38	0.14402
1.3	308.3	57	1.7573
1.2	243.7	94	2.2907
1.1	86	22	0.1892
1	149	336	05.0064
0.9	115	900	1.035
0.8	80.31	1000	0.32728

Table 5
Average Power and Delay of Proposed 10T Full Adder at different Temperatures

Temperature(^{o}C)	*Average Power(nW)*	*Delay(ps)*
-20	180.5	200
-10	182.9	191
0	185.5	184
10	187.8	178
20	190.2	173
30	192	170
40	195.2	166
50	198.5	164
60	200	163
70	203	161
80	206	161

reliable circuit operation under temperature variations. Propagation delay of a circuit is a function of the drain saturation current produced by active transistors. So the designed full adder cell is simulated at different temperatures, propagation delay and average power is noted. Table 5 gives the information of average power and delay of the proposed 10T full adder at cell at temperature range from -20^{0}c to+80 ^{0}c.

The proposed full adder simulation waveforms have shown in Fig. 12 and 13. By observing the simulation waveforms, it can be said that, 6, 8, two 10 transistor full adders, GDI logic based full adder, two 14

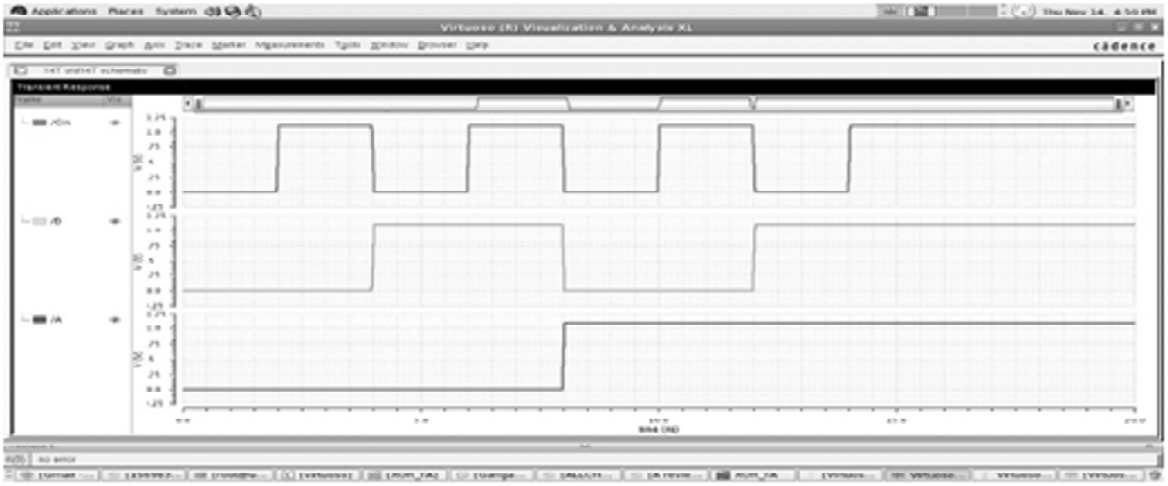

Figure 11: Waveform of test pattern

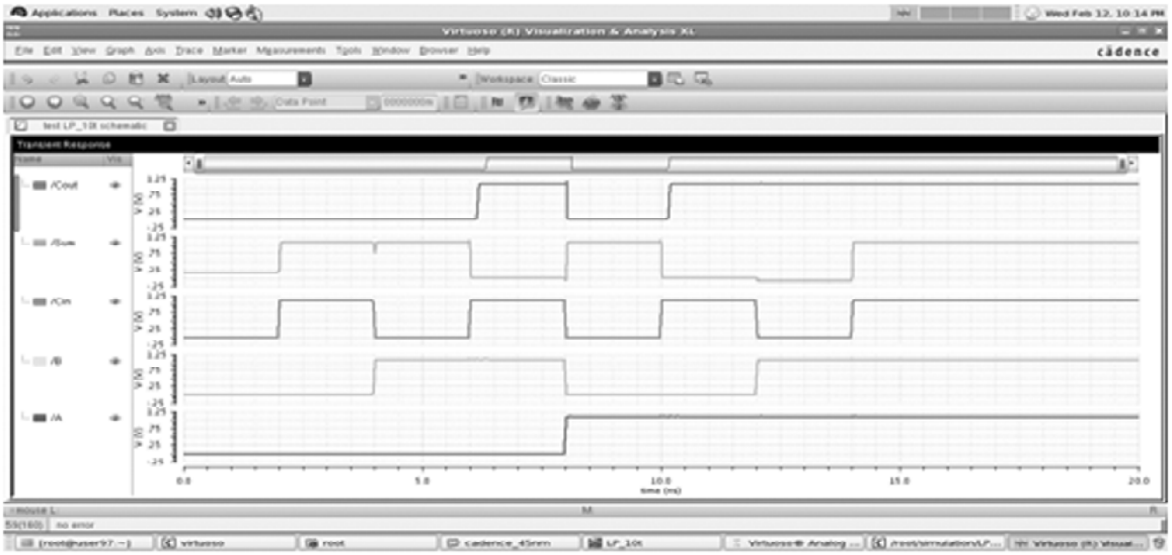

Figure 12: Simulation waveform of proposed 10T full adder

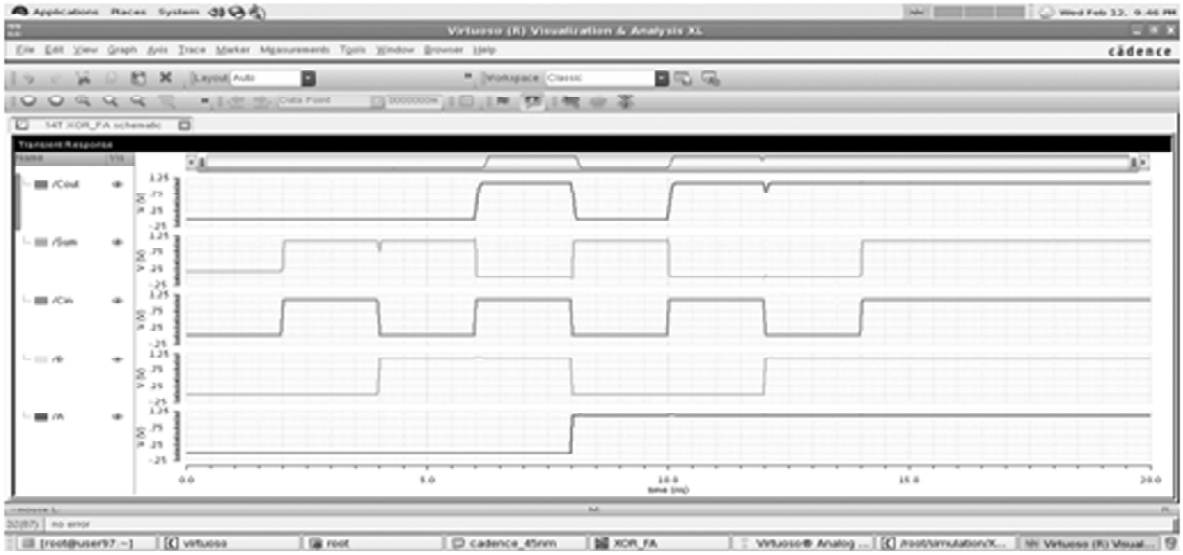

Figure 13: Simulation waveform of proposed 14T full adder

transistor full adders and static energy recovery full adder circuits are not producing the correct functionality of the full adder logic for the given input signals. The proposed full adder circuits working properly for the input combinations (ABCin) from 000 to 111. The input pattern is given in Fig. 11

5. CONCLUSION

In this paper, a novel 10 transistor full adder is proposed and is modified to give the better logic levels at the output node. Parametric analysis of 14T and 10T full adder shows that the proposed circuit works at 45nm technology node effectively well. From Table I, it is showed that the proposed novel full adder consumes less power and worst case delay is also less compared to existing full adder cells. Based on the observation of simulated output waveforms, it can be said that the proposed full-adder circuit has better output voltage swings than that of 10T and 10T GDI full-adder circuits existed in the literature.

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