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Tunable Resistor and Grounded Capacitor Based Square Wave Generator Using CMOS DCCII

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ABSTRACT

The novel implementation of the square wave generator with the current mode device of the CMOS second generation differential current conveyor (DCCII) as an active element with the grounded resistor and grounded capacitor has been proposed in this paper. This circuit offers the advantage of electronic tunability of its duty cycle with externally connected resistor, and capacitor. The proposed circuit has been compared with the existing square wave generators and its advantages are tabulated. The gpdk 180 nm technology has been used for designing and simulation of the proposed circuit using Cadence virtuoso. And it is verified experimentally with the commercially available CFOA of AD844AN.

Keywords: Current mode device; Differential current conveyor; Square wave generator.

1. INTRODUCTION

Of many electronic circuits, square wave generator is being used as a basic building block. For this reason many square wave generator ICs like NE555 have come in to existance, which produces continuous square wave with the external connection of few passive components to the IC [1]. The generated square waveform frequency or time period can be varied in a wide range by the tuning of passive components. In contrast to this gaining reputation from its advantages, these ICs are suffering from other disadvantages of complexity of the internal circuitry and duty cycle is however not tunable with itself. And also these ICs are not useful for high speed applications because of lower slew rate and constant gain-band width product.

The microelectronic technologies have been affected by the requirement of very low supply voltage and power consumption [2]. The excessive speed and the precision are becoming extra requirements for signal processing applications. And the concurrent provision of these hassles is more complicated while the optimum resolution is applied [3]. The new trend of current mode is being used for the implementation of analog signal processing applications for the last two decades [4]. In current mode (CM), the signals are being routed are in the form of currents. Where as in the case of voltage mode (VM) circuits, the signals are being processed in the form of voltage. Compared to that of voltage mode, current mode offers higher bandwidth and signal linearity. As these circuits are implemented for smaller supply voltage operation, lower supply

voltage is needed for operation. In contrast to the conventional voltage-mode methodology, current mode approach for signal processing has gained momentum because of its added advantages viz. steady state of operation, less power consumption, improved bandwidth, compatible operation at lower supply voltages, more dynamic range [5]-[8]. The advancements in the applications using current mode is because of transcend of analog building blocks (ABBs) [9]-[18]. The first current mode active element with the property of current differencing namely second generation differential current conveyor (DCCII) [19] has been introduced in addition to the above mentioned ABBs. The DCCII is the combination of advantages included in the CCII [20] with the property of current differentiation taken from CDBA. For doing current differentiation both the ABBs looks the same but DCCII has the additional terminal voltage as in CCII, this terminal offers high input impedance which is vital for cascading in VM circuits.

From the development of current conveyor, the current-mode circuits have gained much interest in the by gone period [21]. From the above mentioned advantages in the current mode devices and the need of square wave generators for instrumentation applications [22], a novel second generation differential difference current conveyor (DCCII) has been improved and using this DCCII one square wave generator has been proposed in this paper.

2. CIRCUIT OPERATION

The DCCII is a four terminal device with three input terminals and one output terminal, with a current differencing property. The terminal Y provides the high impedance and it is useful in the amplifier applications. The difference of the current flowing across the input terminals X_P and X_N is appeared at the output terminal Z. And also the applied potential across the Y terminal is copied into the X_P and X_N terminals.

The second generation differential current conveyor can be represented symbolically is shown in Fig. 1.

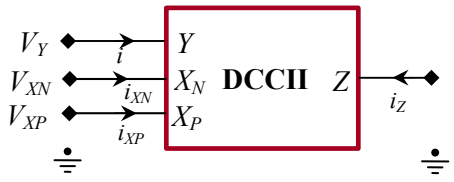

Figure 1: the Symbolic notation of the DCCII

The ideal input and output terminal relations are given by the hybrid matrix as follows:

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ i_Z \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ V_Y \end{bmatrix} \quad (1)$$

The CMOS realization of the DCCII is shown in Fig. 2. The CMOS DCCII is composed of three parts. One is the mixed translinear loop which makes the potential at Y terminal is copied into the X_P and X_N terminals, this operation is performed by the transistors M_1-M_4, M_{18} and M_{19}. The biasing current is provided by the transistors M_5-M_{10} and M_{12}. Finally, the remaining transistors M_{11}, M_{13}-M_{19}, M_{20} and M_{21} will produce difference of the currents across the X_P and X_N terminal. The Table I shows the aspect ratios of these transistors.

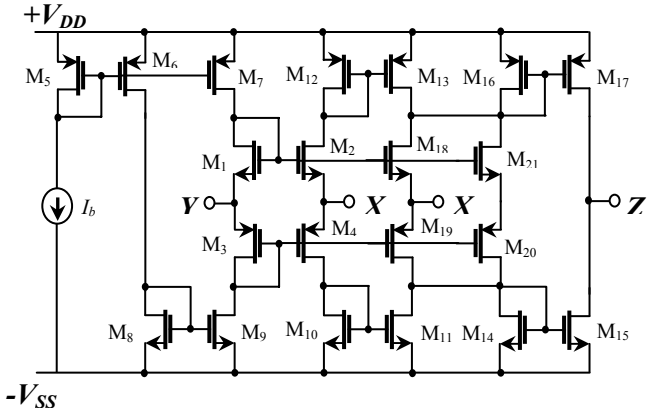

Figure 2: The CMOS realization of the DCCII [19]

Table 1

The Transistors Aspect Ratios Shown In Fig. 1

Transistor	*W (μm)*	*L (μm)*
M_3, M_4, M_{19}, M_{20}	50	0.35
M_5-M_7	30	2.0
M_{12}, M_{13}, M_{16}	30	1.0
M_{17}	50	2.0
M_1, M_2, M_{18}, M_{21}	20	0.35
M_8, M_9	10	2.0
M_{10}, M_{11}, M_{14}	10	1.0
M_{15}	20	2.0

The terminal relations between input and output terminals can be expressed in the behavioral model is shown in Fig. 3.

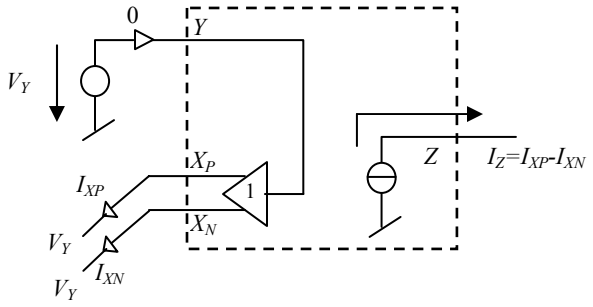

Figure 3: Behavioral model of the DCCII

3. PROPOSED CIRCUIT

The proposed square wave generator with single DCCII, two resistors and a grounded capacitor is shown in Fig. 4.

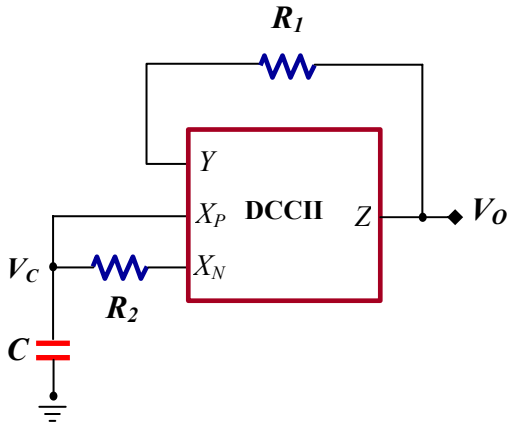

Figure 4: Proposed square wave generator

The expression for the time period (T) can be derived from the terminal relations of DCCII given in eq. (1) and by applying basic network analysis to the proposed circuit is shown in Fig. 4.

$$\frac{V_0 - V_Y}{R_1} = I_0 \tag{2}$$

Where 'I0' is output current. From node VC,

$$I_{XN} = \frac{V_C - V_{XN}}{R_2} \tag{3}$$

From hybrid matrix (1), can rewrite the above eq. as

$$I_{XN} = \frac{V_C - V_Y}{R_2} \tag{4}$$

By applying KCL at node Vc

$$\frac{V_0 - V_{XN}}{R_2} = I_0 \tag{5}$$

$$I_{XN} = \frac{V_C}{R_2} \tag{6}$$

$$I_{XP} = V_{XP} SC \tag{7}$$

Again from eq. (1), can write

$$I_0 = I_{XP} - I_{XN} \tag{8}$$

$$\frac{V_0 - V_C}{R_1} = V_{XP} SC - \frac{V_c}{R_2} \tag{9}$$

From eq. (9)

$$V_0 = V_C R_1 \left(SC - \frac{R_1 + R_2}{R_1 R_2} \right) \tag{10}$$

From, the eq. (2) & eq. (5),

$$V_0 = \left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_C \tag{11}$$

From equating eq. (10) & eq. (11), can obtain S as

$$V_C R_1\left(SC-\frac{R_1+R_2}{R_1R_2}\right)=\left(\frac{1}{R_1}+\frac{1}{R_2}\right)V_C \tag{12}$$

$$S=\frac{2(R_1+R_2)}{CR_1R_2} \tag{13}$$

Where $S=j\omega$, and in which ω is the angular frequency in rad/s, from eq. (13), the frequency of operation, can be notated as follows.

$$f=\frac{(R_1+R_2)}{\pi CR_1R_2} \tag{14}$$

The time period of the proposed circuit at the output terminal V_0 can be expressed as

$$T=\frac{\pi CR_1R_2}{R_1+R_2} \tag{15}$$

Table 2

Comparison Table

Ref.No.	*Device*	*No. of Active Elements*	*No. of Passive Components*	*Grounded Capacitor*	*Grounded Resistor*
[23]	OA	2	4	No	No
[24]	CCII	2	5	No	Yes
[25]	CFOA	2	5	Yes	No
[26]	OTA	2	7	No	No
[27]	OTRA	2	3	Yes	Yes
[28]	MO-CTA	2	3	Yes	No
[29]	MO-CCCCTA	2	3	Yes	No
Proposed	DCCII	1	3	Yes	No

From the above table it can be concluded that only the proposed circuit, with minimum number of components, offering grounded capacitor and a resistor with DCCII as the single active element. And the chip area required for tape out of this circuit is very less when compared to the other circuits where it requires only the single

active element and two passive components. As it has grounded capacitor it offers more accurate results in the IC which is highly recommended by design engineers.

3. SIMULATION AND EXPERIMENTAL RESULTS

The circuit in Fig. 4 was simulated using Cadence and the model parameters of 0.18 µm CMOS process. Figure 5 depicts the typical output waveforms of the proposed square wave generator with charging-discharging across the capacitor. The selected values of the passive components in faithful output is R_1 = 50 kΩ, R_2 = 3 kΩ, and C = 100 nF. The measured time period of the output waveform is T=0.86 ms.

The linear variation of the time period against the variation of capacitor by fixing R_1 = 50 kΩ, R_2 = 3 kΩ is shown in Fig. 6. The variation of capacitor value is from 1nF to 0.4 µF.

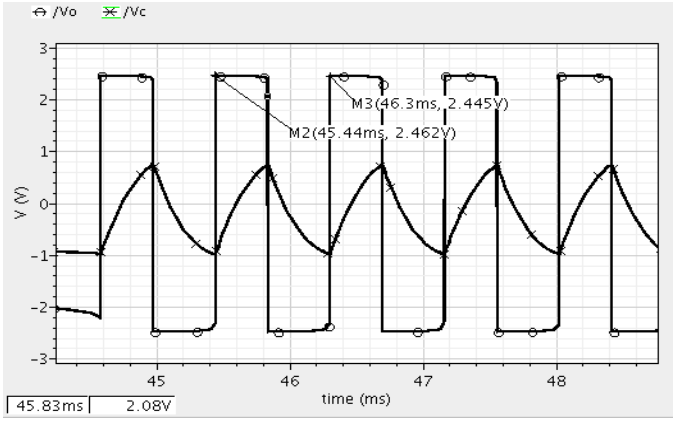

Figure 5: The output waveform across output and capacitor node of the proposed circuit

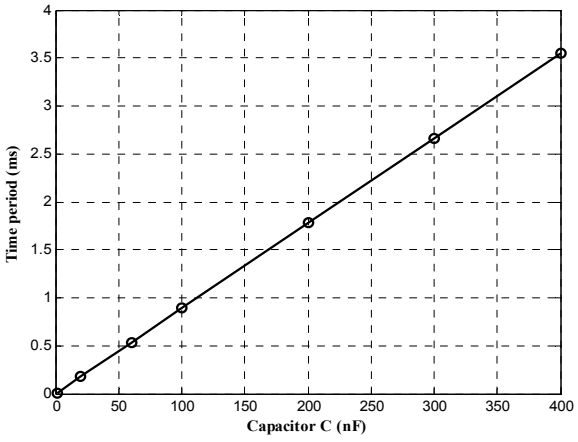

Figure 6: The graph of Time period (T) Vs Capacitor (C) at R_1 = 50 kΩ, R_2 = 3 kΩ.

Similarly, by maintaining R_1 = 50 kΩ and C = 100 nF the variation of the time period against the value of resistor R_2 can be plotted is shown in Fig. 7.

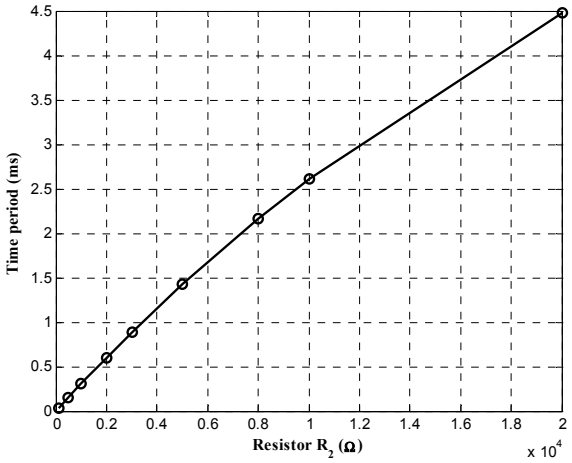

Figure 7: The graph of Time period (T) Vs Resistor R_2 at C = 100 nF, R_1 = 50 kΩ.

The variation of the time period against the value of Resistor R_1 plotted is shown in Fig. 8. For this task R_1 varies within the range of a few ohms to few kilo ohms by keeping the other components at C = 100 nF and R_2 = 3 KΩ.

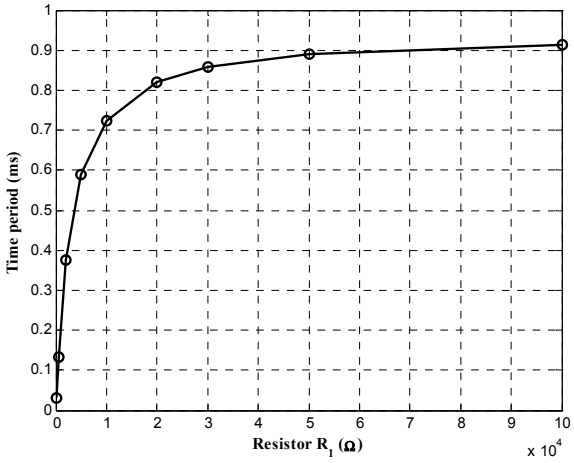

Figure 8: The graph of time period (T) Vs resistor R1 at C = 100 nF, R2 = 3 kΩ

For simulation and tunability, the supply voltage of ±2.5 V has been considered with a biasing current of 400 μA.

The theoretical model of the DCCII can be realized practically by using the commercially available Analog Devices AD844AN. The equivalent model of the DCCII can be achieved by using the two AD844AN ICs. For all the measurements, the supply

voltage taken is as V_{DD} = -V_{SS} = 5 V. By considering the passive components R_1=1 kΩ, R_2=6 kΩ and C=100 nF the operating frequency of 1.01 kHz is achieved.

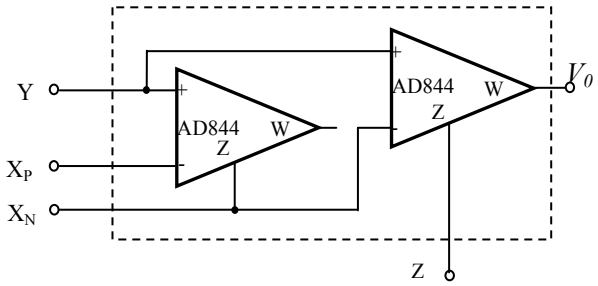

Figure 9: Hardware equivalent model of the DCCII using AD844AN

Figure 10 shows the photograph of the oscilloscope output of the proposed square wave generator. In Fig. 10, the horizontal and vertical scales are 0.5 ms/div and 1 V/div respectively. And from the Fig. 5 and Fig. 10 it has confirmed both experimental and simulated results as well as copes up with the mathematical notation of the time period of the proposed circuit.

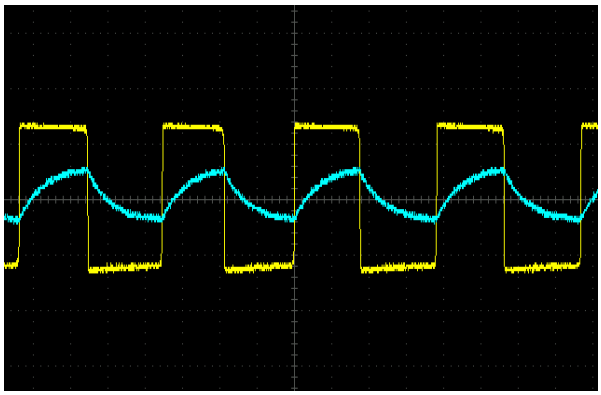

Figure 10: Typical output waveform of Fig. 3. Scale: X-axis 0.5 ms/div & Y-axis 1 V/div

6. CONCLUSION

By using DCCII as a main active element and with two resistors and one capacitor, the square wave generator has been designed. This circuit provides the advantage of the grounded capacitor which makes the circuit more precise while doing the IC fabrication. Another benefit is cascadable while making interconnection with the other VM applications. The proposed model has been compared with the other CM and VM square wave generators and its merits have been justified. The proposed circuit has

proved that both the simulated and experimental results confirmed in good agreement with the theoretical analysis.

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