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REVIEW OF FLASH-SAR ADC WITH PIPELINE OPERATION SUITABLE FOR BETTER PERFORMANCE

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Abstract: this paper presents the review of the conversion process of analog signal to digital signal by combing Flash-SAR ADCs. These parameters are considered for better performance, good efficiency and an excellent Quality of the signal. The paper gives an introduction about the characteristics of the ADC such like resolution, errors etc. The main focus here is to improve the overall performance via combining the two individual ADCs via help of the pipeline mechanism.

Key Words: Conversion process of ADCs, ADCs parameters, ADCs errors, Combine ADCs (Flash ADC, SAR ADCs & combine ADCs)

1. INTRODUCTION

Generally, in real world the data available is analog in nature. For processing an analog signal, first it needs to be converted into a digital signal because all the electronic devices can handle only digital signals. There are many advantages of digital signals such as they are used for storing purpose, less noisy compare to an analog signal, better encryption feature for security purpose and many more. Analog to Digital converter (ADCs) are used for conversion an analog signal to digital equivalent, ADC is an electronic device which plays a lead role in the electronics world. Bless of the VLSI are high performance and device miniaturization. So the chip become smarter for performing multiple operations [3], [8]. ADC is used in radar application, flash memory, mobile, recording studio, receiver of telecommunication, LCD or LED television and many more [11].

2. CONVERSION PROCESS OF THE ANALOG SIGNAL TO DIGITAL SIGNAL

An analog signal is continuous time signal which can't be stored, so we cannot analyze this signal for further purpose. So we need to convert this analog continuous signal to digital (discrete) signal with the help of the different types of ADCs such as SAR, Flash [18], etc. Basically three steps have been followed for doing a conversion. First sampling, then quantization and finally digitizing. Sampling is the process at which breaking down the analog value in terms of set of discrete values. Then quantization takes only few discrete values which values are available. And via help of the encoding process, this discrete value is converting into the digital values [18, 19].

As shown the table 1, we have 0-6 volt peak to peak signal. Separate them in terms of discrete states with 1.5 volt range for each and every state. Now we have four numbers of different

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quantization levels which are illustrated in table 1 and each level assigns the corresponding value in terms of digital form [20].

Table 1
Quantization & encoding for different voltages range.

Voltage Range (V)	*Quantization Levels*	*Encoding*
0 - 1.5	1	00
1.5 - 3.0	2	01
3.0 - 4.5	3	10
4.5 - 6.0	4	11

Conversion process also follows the Nyquist rate. For the faithful reproduction of the input signal, sampling frequency is at least twice number of the input analog signal [15], [18, 19].

$f_s = 2f_m$

Where f_s is a sampling frequency and f_m is the input signal frequency.

Figure 1 depicts a simple representation of the ADC. First the analog signal is given as input and then ADC performs the sampling, quantization and digitization; finally we get a digital output [15].

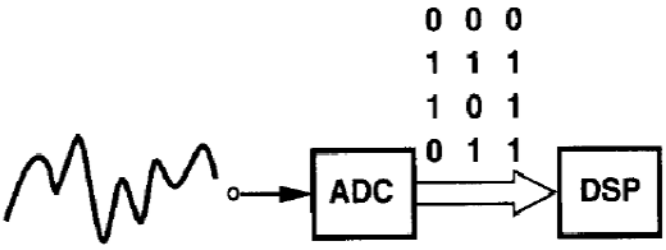

Figure 1 Digitization process of a natural signal [15].

Figure 2, is a modified version of simple ADC. It is used where higher sensitivity of conversion is required. Two blocks are added to the simple ADC. First block is an amplifier, which amplifies the input signal. Because generally output of sensor node is in analog form but sometimes the amplitude of this signal is just few microvolt to few hundred millivolt. So due to weakness of the signal, ADC can't perform the operation. So, first it needs to be amplified. Amplification is just boosting the level of the amplitude. And then second block is filter for avoiding the unwanted frequencies above half of the sampling rate [14, 15].

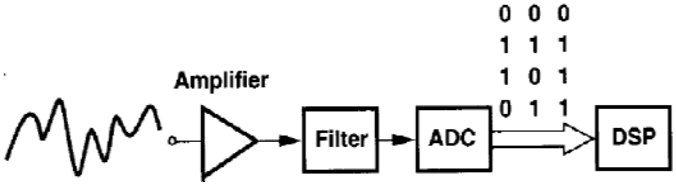

Figure 2 Amplification and filtering of the input signal for higher sensitivity [15].

In ordinary way, the analog signal may slowly vary with time (Such like: Temperature measurement) and an analog signal may speedily vary with time (Such like: Audio recording). Before applied the signal to ADC, we require a sample and hold circuitry for sampling purpose.

3. ADCS PARAMETERS

Basically, there are various parameters for ADCs, with help of them we test the performance of an ADC.

1. Resolution: In given figure 3 denoted that the output of ideal 3 bit ADC and plot of the digital output against a normalized analog input.

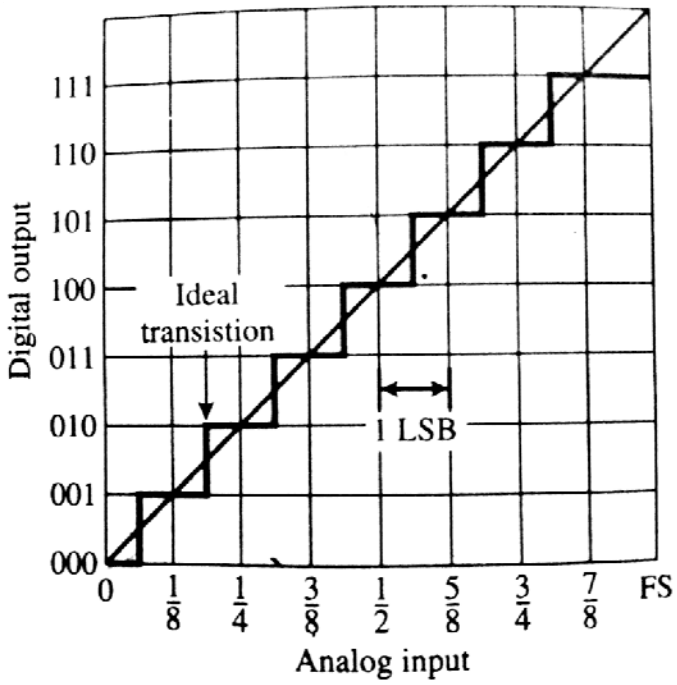

Figure 3 input-output relationships for an ideal 3 bit ADC

The resolution of ADCs is defined through this way,

Resolution = 2^n

Where n is the represented as a number of digital outputs. Since the applied input single is analog voltage and assumed that it's a continuous, number of discrete (digital) output is refer as a Resolution [20]. The ratio between the full scale input voltage range (FSR) of the device to the resolution gives the minimum change of input voltage to cause a change of one digital count at the output. And equation is that

$$\Delta V i \text{ for 1 LSB} = \frac{\text{FSR}}{2^n}$$

Where FSR is full scale input voltage range, which is specified into manufacturer's datasheet. Where n is an amount of digital outputs. The ratio of above equation is simply denoted as a 1 LSB shown in a figure 3 [19, 20].

Since a digital count begins with 0, so that the maximum full scale voltage to cause the output to be all logic 1 is a one least significant bit (LSB) less than the value of full-scale range.

$$V_{ifs} = \text{FSR} - 1 \text{ LSB}$$

Here V_{ifs} is maximum input voltage to cause all logic ones at the output of the ADCs. In general, any input voltage is given from the output-input equation of the ADC.

Digital output code = binary equivalent of D

Where D represents as a number of LSBs and it's found from

$$D = \frac{V_{in}}{1\ LSB}$$

V_{in} is describing the applied input voltage [3, 5, 20].

2. Signal to noise ratio: SNR is a very important parameter for any kind of ADCs. It measures the power of signal and also power of noise. And finally give the amount of signal is distorted [3, 14], [18]. So, higher value of SNR is acceptable.
3. Spurious free dynamic range (SFDR): In the output, the ratio of the fundamental or base signal to the strongest spurious signal. It's divulged to measure in specify DACs and ADCs [11].

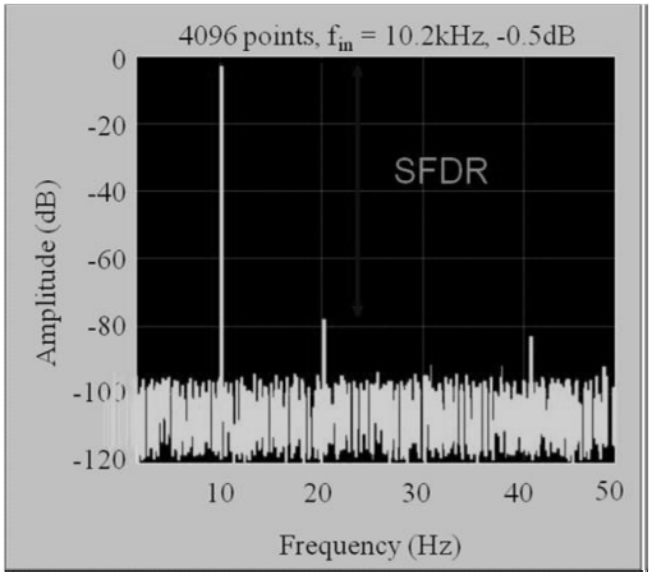

Figure 4 Spurious free dynamic ranges [14].

As per the requirement, dynamic range is a range at which output follows to input. Due to the non-linearity, sometime harmonics are generated, so that the operating ranges for which spurious response are minimal. It's called the SFDR [9, 14]. In figure 4, SFDR is given in particular frequency.

4. Power dissipation: Basically, there are two types of power dissipation.

   1. Dynamic power dissipation

   2. Static power dissipation

   For a low power operation, these types of power dissipation are to be considered [29].

   In ADCs, power dissipation depends upon the fabricated area of the chip. If fabricated area is larger, then chip consumed more amount of power. But if fabrication of ADCs is done using CMOS technology, then it does consume lesser area [15, 18].

4. ADCS ERRORS

For the conversion process, various types of errors may occur such as:

1. ***Quantization error:*** Basically, a difference between the original signal and digitized signal, it's called the quantization error (quantization noise) as shown in figure 5 [3], [11]. Hence the error of the amplitude at the sampling instant is in between zero (0) and half of one LSB (±1/2LSB). It occurs due to the lesser number of finite resolutions of the digital signal and it's unavoidable for all types of ADCs. This error is by default available in any types of ADCs. This error is reducing by the higher number of resolution of ADCs [14].

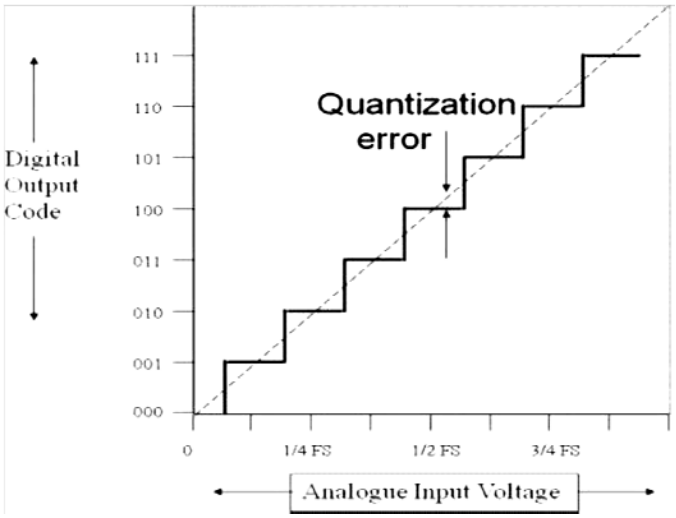

Figure 5 Quantization error [17].

2. Non-linearity: All types of ADCs, non-linearity is always present due to their physical imperfections, and output is deviated from a linear function of their applied input. As an ideal transfer characteristics curve is a straight line. But due to the non-linearity, curve of the ADCs may not follow the straight line of ideal transfer characteristics. This error can be alleviated through calibration techniques or prevented by testing [11]. Non-linearity error reduces the effective resolution of the ADCs, also reducing the dynamic range of the signals. This error is by default available in any types of ADCs. Basically, few parameters consider for linearity are Integral Non-linearity (INL) and Differential Non-linearity (DNL).

   (a) Integral Non-Linearity (INL)

   It's a maximum deviation between the point of an actual code transition and its corresponding ideal transition. Integral Non-linearity is measured in LSBs, and calculated after gain and offset errors have been compensated [9], [14]. If the transition is occurring later than ideal, then it's called positive Integral Non-Linearity (INL). In other side, if the transition is occurring earlier than ideal, then it's called negative Integral Non-Linearity (INL) [17]. As shown in figure 6. It's measured in LSBs.

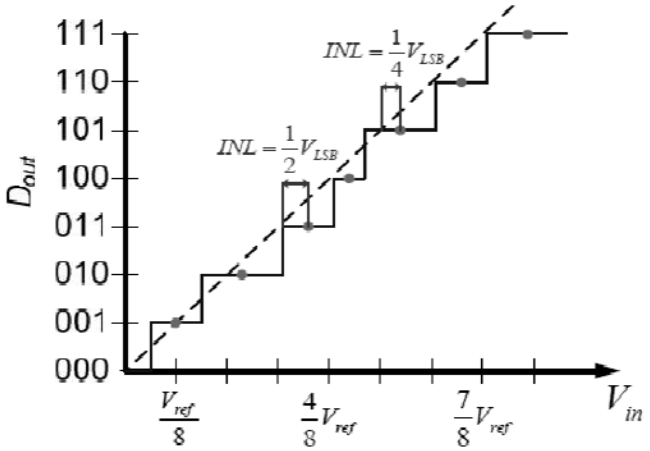

Figure 6 Integral Non-linearity [17].

   (b) Differential Non-linearity (DNL)

It's a measure of maximum deviation from the ideal step size of 1 LSB. This may result in either narrow or wide code width when compared to ideal code. This can result in missing code as well [9], [14]. The error in DNL is measured in LSB [17]. As shown in figure 7.

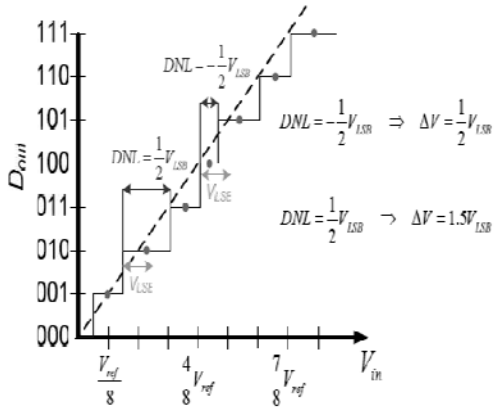

Figure 7 Differential Non-linearity [17].

3. Aliasing: If the input signal is changing much faster than the sampling rate, then the digital signal reconstruction from the analog signal isn't same as original one, but at this time some spurious signal is generated. It's called aliases. And. this issue is called aliasing [11]. To prevent for aliasing, put the low pass filter at beginning side of the ADCs. When input signal is apply, first it passes out from the low pass filter and filter is to remove the unwanted frequencies and provide the noise less frequency. So this type of filter is called an aliasing filter [14]. As shown in figure 8.

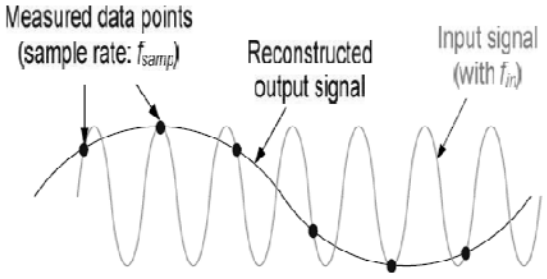

Figure 8 Aliasing [17].

5. TYPES OF ADCS

There are several types of ADC's and several methods are available for implementing electronic ADCs.

1. FLASH ADC: Flash ADC is the fastest ADC, and is also called as parallel ADC. Due to the parallel mechanism, its conversion rate is much faster than the other ADC's And this types of ADC's are suitable for higher bandwidth Application such as Radar, Setup Box, Solid state Drive and many more. But there are some drawbacks such as consumption of large amount of power due to the ladder circuitry of resisters and as well as high amount set of comparators [21, 22]. It's suitable for lower resolution ADC. For higher resolution, flash consumes more amounts of power as well as higher amount of area on the chip.

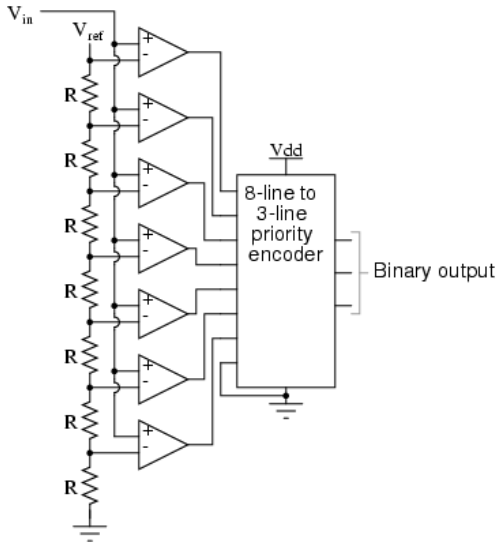

Figure 9 3 Bit FLASH ADC [24].

The above figure shows the building block of the flash ADC, For N-bit conversion, requires 2^n number of resisters and (2^n-1) comparators (also requires preamplifiers) [20, 30]. First, 2^n resisters are provided to the reference voltage for each comparator. The reference voltage of each comparator is 1 LSB (least significant bit). If input signal voltage is greater than the reference voltage, then the comparator output is Logic '1'. Conversely, if input signal voltage is less than the reference voltage, then the comparator output is Logic '0' and finally all outputs are collected by priority encoder [16, 20]. Priority is a means for resolving simultaneous inputs. In other words the highest input has the priority [23].

As a demand of high performance and high sampling rates, flash ADC is a major choice for faster conversion. Due to its simple architecture, the rate of conversion in it is much higher than the other ADC's [4, 6]. For acquiring high resolution, large amount of comparators are required but, as a result the junction capacitance will vary. The input signal is dependent upon capacitance as a result flash ADCs have a higher distortion at high frequencies and this reduces the effective number of bits (ENOB). [5, 6]

2. Successive Approximation Register(SAR): Successive-approximation is also another type of analog to digital converters (ADCs). And it represents a majority of the ADC domain for its medium conversion rate and it also has a quite good resolution. Its conversion speed is around 4-7Msps with good resolution. One of the advantages is that it consumes less amount of power and its package density is manageable in terms of fabricated area. [23].

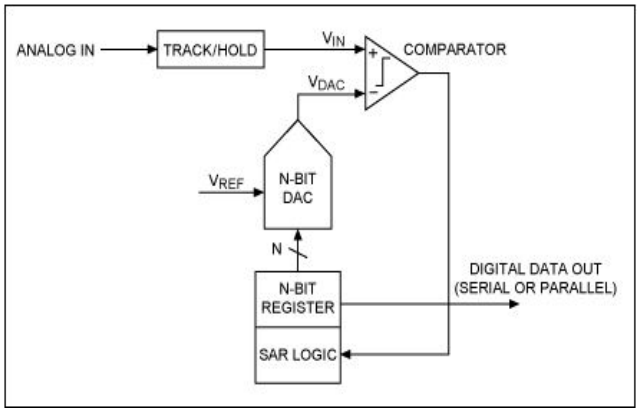

Figure 10 SAR ADC [24]

There are various ways to build or implement the SAR ADC. SAR consists of a DAC, a successive approximation register (SAR) and a comparator. As shown in figure 10. Input terminal is required for applying analog input voltage (VIN) and digital data is collect from the output terminal. SAR has three control terminals which decide overall operation of ADC. Conversion process is initiated by start conversion terminal. And end conversion terminates the conversion process. So the conversion process is successfully completed. One more external clock terminal is used for allotting the time to complete each conversion process. The N-bit SAR register follows the binary search algorithm. When start conversion is initiated, then the digital output of register is going to a DAC (digital to analog converter). Finally DAC is converting the digital signal to analog signal (VDAC). And output of DAC is compared with the VIN. If voltage of VIN is higher than the voltage of VDAC, then output of comparator is logic '1'. Conversely, if voltage of VIN is lower than the voltage of VDAC, then output of comparator is logic '0'. Comparison process is starting with MSB and ending with LSB. When comparison has been completed, then SAR is generated at the end conversion signal. Finally, digital output is present at the N-bit register. [12, 23, 24].

3. Combine ADCs (Pipeline Operation): As earlier, we have talked about the individual flash and SAR ADCs. In many digital as well as wireless applications [1], high speeds ADCs are required for faster operation. Researches are going on for desiging energy efficient ADCs which have been directed towards SAR ADCs. For a wide variety of applications, improved bit conversion rate per is required per each step. Sequential operation of ADCs limits the sampling rate, which is undesirable. Some mechanisms offer two bits per step such as SAR ADCs [25] and (TI-ADCs) time interleaved ADCs [31] had been proposed for elimination of sampling rate limitation. In short N/2 clocks are required for N bits determination. These topologies boost the ADC speed, but it consumes more area as well as power. Because this design has requires several number of comparators and reference generators.

   New architectures have been introduced which can be combined with two or more different types of ADCs for improving the overall performance [26, 27, 28]. Flash has advantage of higher conversion rate and SAR has advantage of high power efficiency. Combining both the advantages we can get a hybrid structure of the flash-SAR ADC. As shown in figure 11.

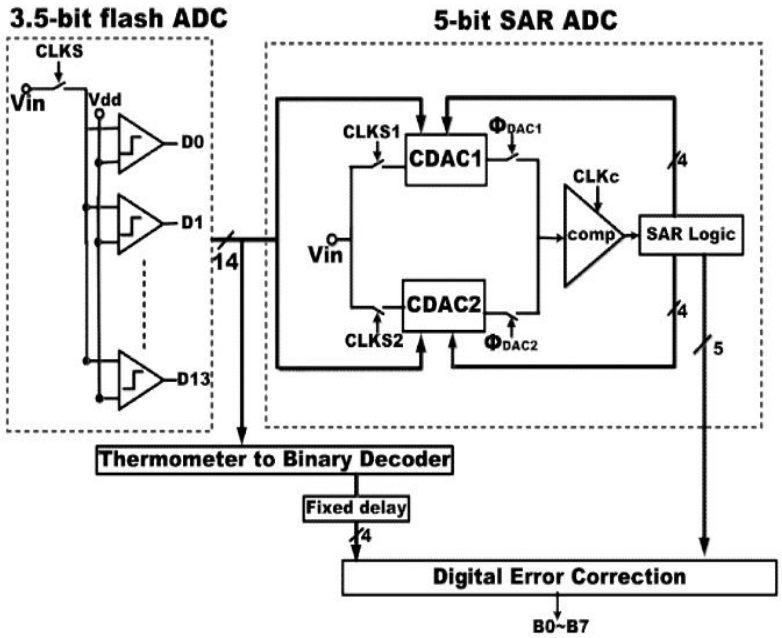

Figure 11 Combine Flash-SAR ADCs [1].

Due to the sequential structure, the performance of the flash and SAR have a limited conversion rate. If power consumption and complexity are not considered, then conversion rate may be improved. So that, improving the conversion rate by adding one more capacitive digital to analog converter (CDAC) for providing a concurrent operation of flash and SAR. As shown in figure 11 [1]. For improving power efficiency on flash ADC, MUX based flash ADC's are used. Because by using this technique, number of preamplifiers and comparators can be reduced for high resolution [30].

6. RESULT AND DISCUSSION

As a talk about the flash-SAR ADCs, overall performance would be increasing to place an Additional CDAC in parallel manner of SAR. So the sampling rate is going to be double.

Less number of bit overlapping between flash and SAR ADCs. So this mismatch probability is an endurable and no compromises for the overall performance.

Table 2
Flash-SAR/sigma-delta

Combination of ADCs	*Functionality*
Flash-SAR	Increasing the sampling rate. Less number of bit overlapping. Data Latency is low.
Flash-Sigma delta	Limitation of Sampling rate. More number of bit overlapping. Data latency is high due to the low sampling rate.

As given the table 2, sampling rate is limited in the flash-sigma delta ADCs. Because lower conversion rate of sigma delta ADC. So number of mismatch can't be tolerable.

In flash-SAR, attach the more number of CDAC in parallel manner for improving the conversion rate of ADCs.

7. CONCLUSION

In this review work, parameters and errors are considerations for design any kind of ADCs. Flash has a higher conversion rate, but less efficient for high resolution as well as consumes large fabrication area. SAR has a medium speed of conversion rate, but highly efficient structure in terms of power dissipation. In a combined hybrid flash-SAR ADCs, that utilizes the pipeline operation between them. This combined structure improves the conversion rate and is highly efficient in terms of overall performance, but there is a tradeoff between area and power.

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