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BER Evaluation of LDPC Decoder with BPSK Scheme in AWGN Fading Channel

Neha Mahankal*, Sandeep Kakde* and Atish Khobragade**

ABSTRACT

Low Density Parity Check (LDPC) codes nowadays use in modern system due to their excellent performance. LDPC codes are advantageous in terms of throughput, bit error rate and power dissipation in digital communication system. As per the requirement of high throughput, layered decoding algorithm of LDPC coding technique is being generally adopted with low computational complexity. The layered decoding algorithm can be applied to improve convergence speed and lower the bit error rate. In this paper, we present the mathematical analysis of simplified Min Sum Based Column Layered Decoding Algorithm with example and also shown improved bit error performance over AWGN Channel. We propose an integrated version of Min Sum Algorithm and Column Layered Decoding Algorithm which reduces complexity and Improve Bit Error Rate performance by 0.135. Reduced complexity and high speed decoder finds application in Wireless Sensor Networks and mobile communications.

Keywords: LDPC codes; Layered decoding algorithm; low computation complexity; simplified min sum based column layered decoding algorithm; bit error performance.

1. INTRODUCTION

LDPC codes and Turbo codes have very low bit error rate for low signal to noise ratio. But on comparing the decoding algorithms of turbo codes and LDPC codes, the LDPC decoding algorithm has more parallelization, low implementation complexity and low decoding latency [1]. Low density parity-check code (LDPC) is an error correcting code used in noisy communication channel to reduce the probability of loss of information. LDPC code mainly depends on the parity check matrix which contains low number of 1's and number of 0's [2]. These matrices can be efficiently represented by bipartite (Tanner) graph. Their main advantage is that they provide a performance which is very close to the capacity for a lot of different channels and linear time complex algorithms for decoding. Lower density parity check code has excellent error correction capability which is measured as BER. The major implementation complexity in column layered decoding is associated with variable node unit (VNU), predominantly when the messages corresponding to multiple sub blocks in column layer are processed in parallel. . As only addition operations are performed in a VNU [11-13], it is very well-situated to employ arithmetic optimization to minimize the critical path. The intrinsic message loading latency is minimized in the column layered decoding because decoding can start as soon as the intrinsic messages corresponding to one block column are available. This paper is organized as follows. Section I highlights an introduction part. Section II describes the previous work. Section III describes simplified min sum based column layered decoding algorithm. Section IV focuses on the MATLAB Implementation of modified column layered decoding algorithm. Section IV concludes the paper.

* Department of Electronics Engineering, Y C College of Engineering,Nagpur, Maharashtra, India, *Emails: nehamahankal1@gmail.com, sandip.kakde@gmail.com*

** Department of Electronics Engineering, Rajiv Gandhi College of Engineering, Nagpur, Maharashtra, India, *Email: atish_khobragade@rediffmail.com*

2. PREVIOUS WORK

The common method of decoding is to verify if the computed codeword satisfies all parity check constraints of the transmitted codeword at one iteration. If it is not satisfies then gain process starts from first step and verifies at the end of each iteration. Once it verifies decoding process is terminated. In wireless communication generally there are two types of nodes which are sensor node and base node. Sensor node can transmit/ encode data and base node can receive/decode data. In [3] the authors of investigates the possibility of implementing short length in wireless sensors network's in which data can both transmit and receive information. Thus it indicates that LDPC codes with smaller block length are acceptable for typical throughput and data transmission. Basic decoding algorithms of LDPC decoder is min sum algorithm (MSA) and sum product algorithm (SPA) which are based on message passing scheme. MSA is approximation of SPA only the computation complexity is less in MSA. To improve performance and other parameters like throughput and memory requirements of MSA, authors of [4] introduced Offset Min Sum decoding algorithm of 5 bit which could achieve same Bit Error Rate (BER) performance as that of SPA. It is suitable for WIMAX technology. As WIMAX technology uses microwaves for the transfer of the data. Generally it can be used for high speed applications and wireless mobile networking at a distance of few kilometers. In this paper, their important parameter is an efficient architecture that employs the value reuse property of MSA.

In Low Density Parity Check codes, R. Gallager's described that received information can be decoded by using iterative updating of information [1][4]travelling between check node and variable node. It can be shown by using tanner graph. Turbo decoding message passing (TDMP) algorithms is well appreciable for decoding process for low quantized bits. TDMP is also called as horizontal layered decoding algorithm. It significantly reduces average number of iterations [10]. Similar to TDPM, another decoding algorithm was implemented, the shuffled decoding algorithm, which has same working only the difference is that shuffled decoding algorithm has high complexity. Hence it is difficult to implement VLSI implementation of shuffled decoding algorithm. Due to approximation of shuffled decoding algorithm authors of [5] introduces layered decoding scheme. Layered decoding scheme has two approaches, these are, column layered and row layered. In column layered decoding scheme message updating can be perform column layer by column layer. In row layered decoding message updating between check nodes and variable nodes can be perform row layer by row layer. In proposed paper we prefer column layered decoding scheme as the convergence speed of row layered decoding algorithm is more as compared to column layered also hardware complexity is more in row layered decoding scheme [6-9].By using min sum based column layered decoding algorithm the check node computation is optimized to remove most of the unnecessary comparisons so that computation complexity can significantly reduces but the average number of iterations remains same.

3. SIMPLIFIED MIN SUM BASED COLUMN LAYERED DECODING ALGORITHM

Let H be a parity check matrix with M rows and N columns. Each row represents check node and each column represents variable node. Let N(c) = {v:Hcv=1} denote the set of variable nodes that associated with check node and M(v)={c:Hcv=1} denotes the set of variables that associated with variable node. Let Iv represents intrinsic message for variable node V. The proposed min sum based column layer decoding algorithm is described with pseudo code.

PSEUDO CODE OF MIN SUM BASED COLUMN LAYERED DECODING ALGORITHM

1. INITIALISATION

   Lcv=Iv for V=0,1,….,N-1, C=0,1,….,M-1

2. ITERATIVE DECODING

   For Iter=1,2,…..,maximum iteration number

{

2.1 Horizontal Step: for each check node C that is connected to variable node V

$$Rcv = \prod_{n \in N(c)/v} Sgn(Lcn) \times \min_{n \in N(c)/v} |Lcn| \quad (1)$$

2.2 Vertical step: For each variable node V that is connected to check node C

$$Lcv = Iv + \propto \times \sum_{m \in M(v)/c} Rmv \quad (2)$$

$$Lv = Iv + \propto \times \sum_{m \in M(v)/c} Rmv \quad (3)$$

3. Hard Decision

Make hard decision by using sign of Lv.

0 for positive sign

1 for negative sign

Terminate the decoding if valid codeword is found

}

4. MATHEMATICAL ANALYSIS

Let us consider the parity check matrix [H], It is given by

V=1 2 3 4 5 6

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}$$

Figure 1: Sparse H Matrix

Tanner graph of the above matrix can be drawn as shown in fig 2.

Transmitted codeword is [0 0 1 0 1 1]

And Received message is [-0.1 0.5 -0.8 1 -0.7 -0.5]

[1 0 1 0 1 1]

Consider α =0.75

Intrinsic message can be generated by using formula

$$ri = 4yi \propto$$

Iv=ri

Where i = number of elements in codeword

i=1,2,3,.....

r1=4*(-0.1)*0.75=-0.3

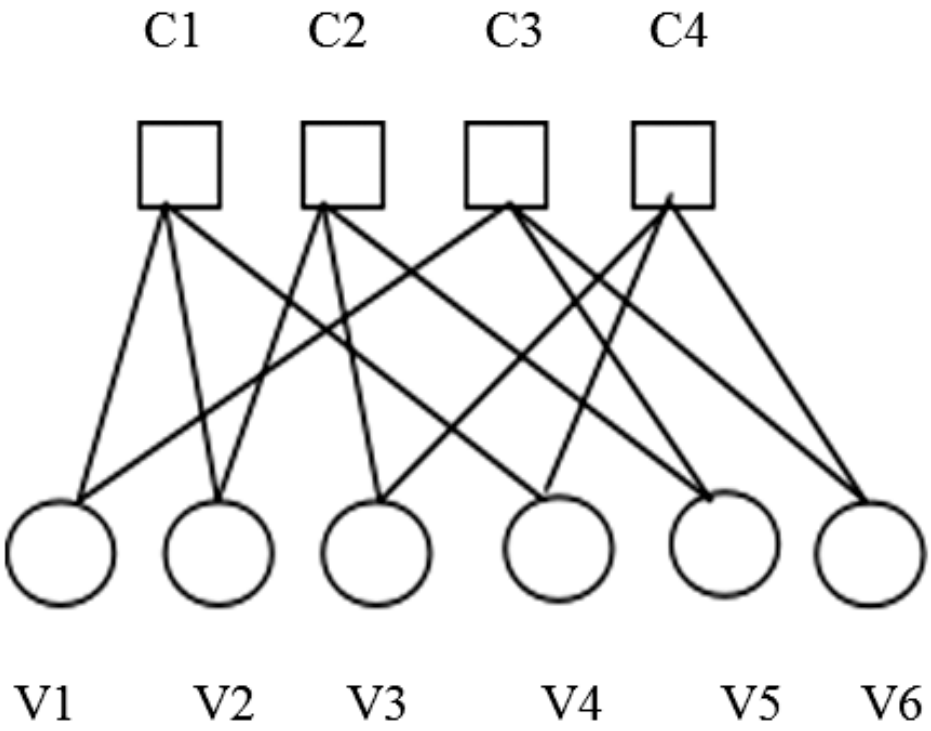

Figure 2: Tanner graph of above parity check matrix

r2=1.5

r3= -2.4

r4=3

r5= -2.1

r6= -1.5

r= [-0.3 1.5 -2.4 3 -2.1 -1.5]

Steps of Algorithm:

Initialisation:

Lcv=Iv for v=1,2,3,4,5,6 C=1,2,3,4

L11=L31=r1=-0.3

L12=L22=r2=1.5

L23=L43=r3=-2.4

L14=L44=r4=3

L25=L35=r5= -2.1

L36=L46=r6= -1.5

Horizontal step: for each check node c that is connected to variable node, computes

$$Rcv = \prod_{n \in N(c)/v} Sgn(Lcn) \times \min_{n \in N(c)/v} |Lcn|$$

Rcv :- Check to variable message conveyed from check node C to variable node V

R11= (+* +) * 1.5 = 1.5

R12= (- * +) * 0.3= -0.3

R14 = -0.3

R22=2.1

R23= -1.5

R25= -1.5

R31= 1.5

R35= 0.3

R36= 0.3

R43= -1.5

R44= 1.5

R46= -2.4

$$Rcv = \begin{bmatrix} 1.5 & -0.3 & 0 & -0.3 & 0 & 0 \\ 0 & 2.1 & -1.5 & 0 & -1.5 & 0 \\ 1.5 & 0 & 0 & 0 & 0.3 & 0.3 \\ 0 & 0 & -1.5 & 1.5 & 0 & -2.4 \end{bmatrix}$$

- Vertical step: for each variable node v that is connected to check node c, computes

$$Lcv = Iv + \propto \times \sum_{m \in M(v)/c} Rmv$$

Where Lcv:- variable to check message conveyed fro variable node to check node

L11= -0.3+(0.75*1.5)= 0.825

L12= 1.5+ (0.75*2.1)=3.075

L14=4.125

L22=1.275

L23=-3.525

L25=-1.875

L31=0.825

L35= -3.225

L36= -3.3

L43= -3.525

L44= 2.775

L46=-1.275

$$Lv = Iv + \propto \times \sum_{m \in M(v)/c} Rmv$$

$$Lcv = \begin{bmatrix} 0.825 & 3.075 & 0 & 4.125 & 0 & 0 \\ 0 & 1.275 & -3.525 & 0 & -1.875 & 0 \\ 0.825 & 0 & 0 & 0 & -3.225 & -3.3 \\ 0 & 0 & -3.525 & 2.775 & 0 & -1.275 \end{bmatrix}$$

L1= -0.3+(0.75 *(0.825+0.825))= 0.93

L2= 1.5 +(0.75* (3.075+1.275))= 4.76

L3=-7.68

L4=8.175

L5=-5.92

L6=-4.93

- Hard decision:

if sign of Lv is + then — 0

Otherwise 1

New received codeword from Lv is [0 0 1 0 1 1] This is same as transmitted codeword. Flowchart of the algorithm for developing the MATLAB code is as shown in Figure 3.

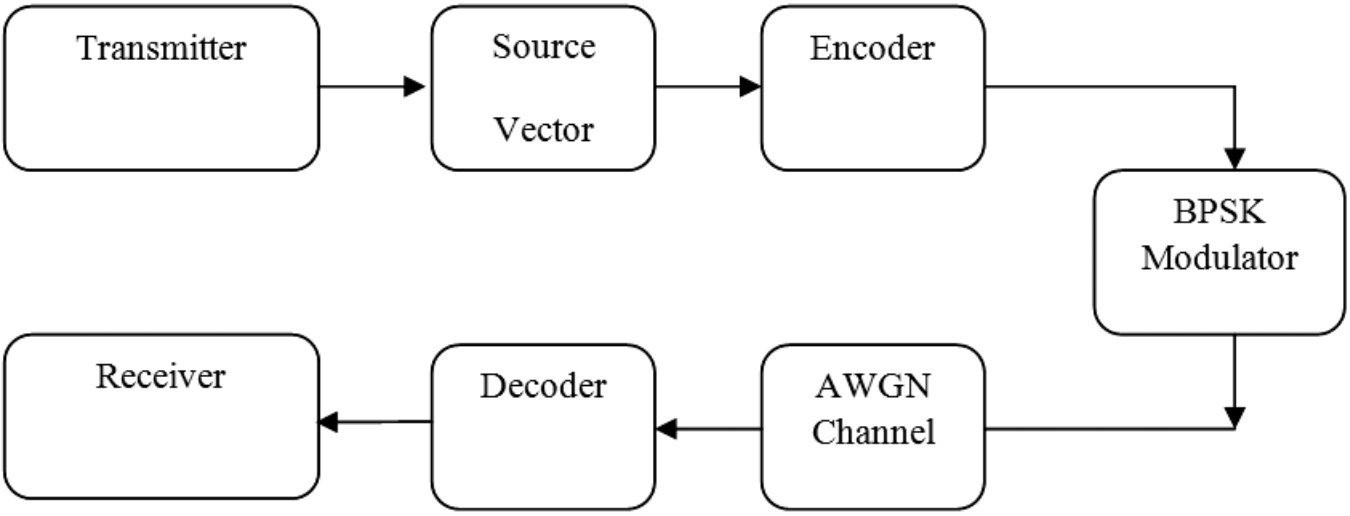

Figure 3: Flowchart

5. MATLAB IMPLEMENTATION RESULTS

First, we simulate the performance of layered decoding of LDPC code assuming block length of (3584, 4096). According to the simulation results in Fig. 4, we find the decoding error performance curve of

Table 1
Input Parameters

Modulation	BPSK
Channel	AWGN
(M,N)	(3584,4096)
Code rate	7/8

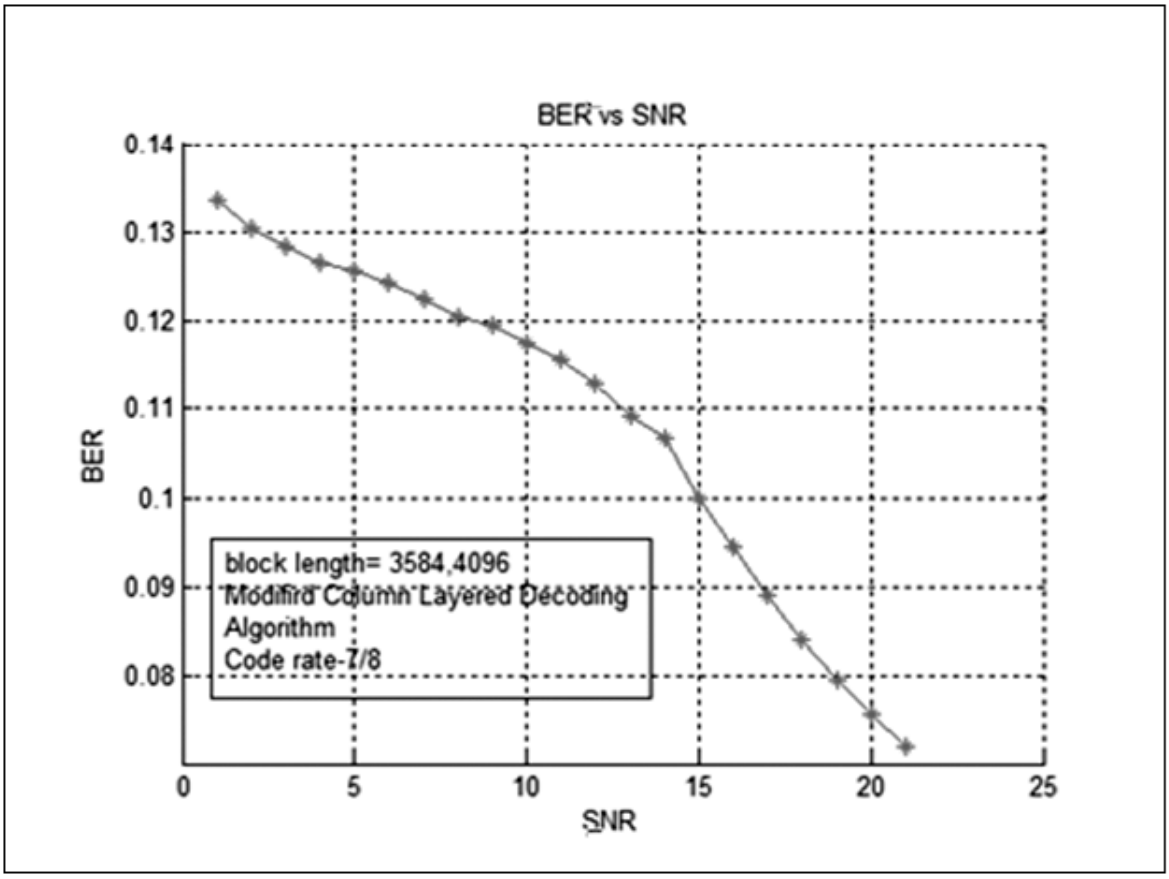

Figure 4: The simulation result of block length (3584,4096) LDPC code

column layered decoding algorithm. All the code is written in MATLAB for the code rate 7/8.The results of this paper are therefore valuable to determine best possible LDPC codes for low bit error rate applications such as wired and wireless sensor networks.Fig 4 shows the simulation result of LDPC decoder having block length (3584, 4096) using BPSK scheme and AWGN channel.

Table 2
BER for SNR

LDPC Decoder	
SNR (dB)	*BER*
1	0.135
5	0.125
10	0.117
15	0.1
20	0.075

6. CONCLUSION AND FUTURE WORK

This paper presented the mathematical analysis and MATLAB implementation of basic min sum based column layered decoding algorithm for LDPC decoder with a appropriate example having only one iteration. Also BER performance of this algorithm is simulated in MATLAB for a block length of (3584, 4096). As the LDPC block length becomes larger and larger, it becomes very complicated to manually code and connect all the variable and check nodes of sparse parity check matrix. Future work includes the development of HDL for the block length (3584, 4096). As the channel BER is low, the efficiency of code increases very

rapidly. The existing layered decoding algorithm based LDPC decoder implementations suffer from low bit error rate and throughput, which avert them from being used in practical wireless application systems. To surmount this problem, we present optimization techniques for a parallel LDPC decoder with algorithm optimization, fully memory access for communication systems. Experimental results exhibit that the proposed LDPC decoder achieves a bit error rate of 0.135 bps.

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