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A novel Low-Voltage Sense Amplifier for Flash Memory

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ABSTRACT

A new low-voltage and high-speed sense amplifier based on very simple direct current-mode comparison is presented in this paper. It adopts low-voltage reference current generator implemented through trimmable resistor instead of reference cell to avoid the immutable voltage drop across the reference cell to generate adaptive reference current, thus enabling the sense amplifier to work with low power supply voltage at about 1V. The proposed sense amplifier was simulated in a flash with a 65nm flash technology. Simulated results show a read access time of 28.5 ns with a power supply voltage of 1 V and slow corner at 125 ℃.

Keywords: flash memory, sense amplifier, trimmable resistor, low-voltage.

1. INTRODUCTION

The flash memories are widely used as nonvolatile storage in electronic systems such as mobile telephones, digital video cameras, microcontroller etc. The ever-increasing need for portable electronic equipment with high speed and low power consumption is accelerating the design of flash memories targeting high speed as well as low power consumption. To satisfy the low-power constraints in the digital circuit domain, the customary way is to reduce the power supply voltage [1]-[3]. To satisfy the requirement of very low power consumption in portable applications, the power supply voltage has been scaled down. The sense amplifiers used to retrieve the stored data in flash memory, are one of the most critical circuits in flash memories, which is strongly related to the read access time. Accordingly, the sense amplifier as an important part of flash memory will also vary to be adapted to the low voltage and high speed.

There are many researches on sense amplifier in the literature [4]-[8]. The solution presented in [4] needs transistor with special low-threshold-voltage, which will require additional masks. Consequently, the die cost will be added due to additional masks. The solutions presented in [5]-[8] are based on current-code approach for enhancing sensing speed. In the mode, the selected memory cell current is directly compared with reference current usually generated through another cell in the same array of memory cell during read operation. However, the threshold voltage of diode-connected transistors in current mirror transistors limits the power supply voltage in these solutions, which will lead to that they can't work with low power supply voltage. The solution presented in [9] is based on voltage-mode approach in which cell current will be converted into voltage to be compared with reference current by a comparator. It takes use of body-drain-driven transistor to increase headroom. As is known to all that cell current limits the current-to-voltage conversion speed. Consequently, the solution can't acquire high sensing speed when it works with low power supply voltage. The solution presented in [10] avoids the use of diode-connected in current mirror by biasing drain and gate at appropriate voltage, which enable the solution to work with low power supply voltage without the limitation of threshold voltage in current mirror transistor. However, the solution has some disadvantages over its structure. The reference current will be greatly affected by the current accuracy of transistors M3 and M5. In addition, the pre-charge speed of bit lines is quite slow, which results in that the solution is not suitable for high-speed read operation.

The paper focuses on a new low-voltage sense amplifier based on trimmable resistor for flash memories, capable of operating at low power supply without using special low-threshold-voltage transistor or diode-connected MOS transistors in current mirror. The low-voltage sense amplifier removes the immutable limitation

of the voltage drop on reference cell by using trimmable resistor to substitute for reference cell in reference current generating circuit. The voltage drop across trimmable resistor can vary with the need of the power supply voltage, which enable the new sense amplifier to work at low power supply voltage.

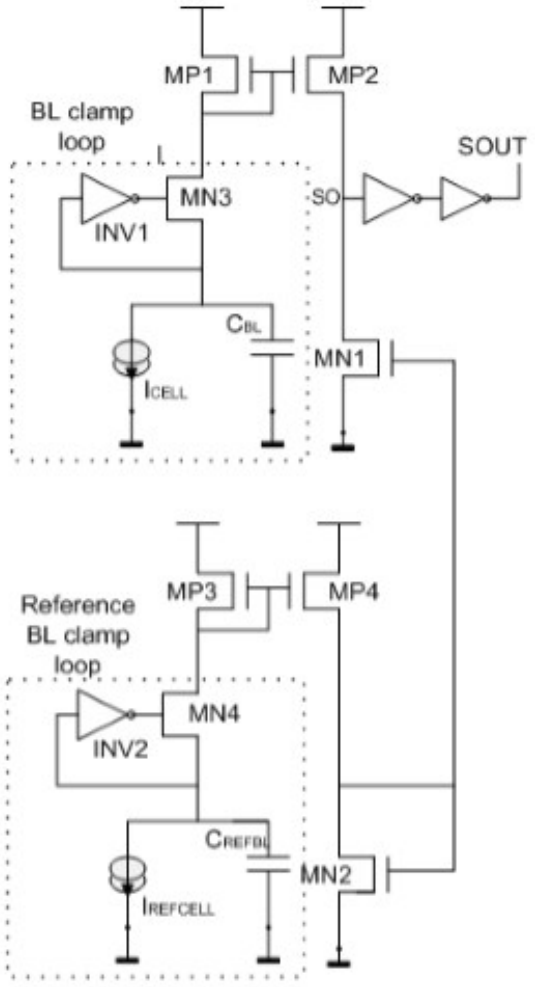

Fig.1 Differential sense amplifier based on current-code

2. CONVENTIONAL CURRENT-MODE SENSE AMPLIFIER

2.1 Conventional Current-Mode Sense Amplifier

A typical sense amplifier based on current-mode approach is illustrated in Fig.1, composed of memory cell current extraction path extracting selected memory cell current, reference current extraction path extracting reference current and sensing output circuit generating output signal that corresponds to digital data stored in selected memory cell by sensing voltage converted by differential current between reference current and selected memory cell current. ICELL is the cell current flowing through BL clamp loop and then is mirrored one time by current mirror. IREFCELL is the reference current flowing through the reference BL clamp loop and then is mirrored two times by current mirror. ICELL and IREFCELL then are compared generating differential current converted into differential voltage on node SO, and SOUT representing the output logical value is then issued from the comparison result. In addition, BL clamp loop circuit is responsible for guaranteeing the minimal mismatching between BL voltage and reference BL voltage, which guarantees matching between ICELL and IREFCELL.

However, the structure still has some limitations. Firstly, the structure can't work with low power supply voltage due to the necessary voltage drop across reference cell to generate adaptive reference current and the mirror pair. As can be seen that the lowest power supply voltage is given by

$$V_{DD(MIN)} = V_{BL} + V_{DS(MNS)} + V_{TH(MP1)} + V_{OV(MP1)} \quad (1)$$

Where VBL is at least designed as 1Vth thanks to the need for guaranteeing the size of cell current, which result in the lowest work voltage is at least equal to 1.5V. Secondly, the structure can't realize very high read speed. The voltage on node SO may be any value since the relation between ICELL and IREFCELL is not determined during pre-charge, and even worse, it will take long time to charge or discharge node SO, which directly affects read speed and even leads to error during fast access time. Thirdly, the structure possesses low sense precision. The process mismatch between devices is large due to advent of current mirror pairs in the structure. In addition, the channel modulation effect is fatal for sense accuracy due to the large output swing on node SO. Fourthly, the structure has large power consumption. When read operation is carried out, the reference current is used only one time and much cell current simultaneously occurs due to many bits of read operation. Consequently, the equation of power is expressed as follows:

$$I_{VDD} = N * (I_{CELL} + I_{REF-COM} + I_{BL-PRE}) + I_{REF} \quad (2)$$

Where N is the number of sense amplifier required during one read operation, IREF-COM is the reference comparison current, and IREF-COM =ICELL*0.35, and data-0.35 is reference current trip point, IREF is

the current of reference current generator. IBL-PRE is BL pre-charge current. Finally, the structure has the bad power noise. Taking account of high read access speed, the large capacitance can't be inserted into immediate node. When the VDD suddenly varies, the gate of PMOS transistor (MP1, MP2, MP3, MP4) or the gate of NMOS transistor (MN1, MN2) can't in time keep up with the variation, which directly leads to current gap between ICELL and IREFCELL, and even worse, causes error switches on node SO thus error SOUT.

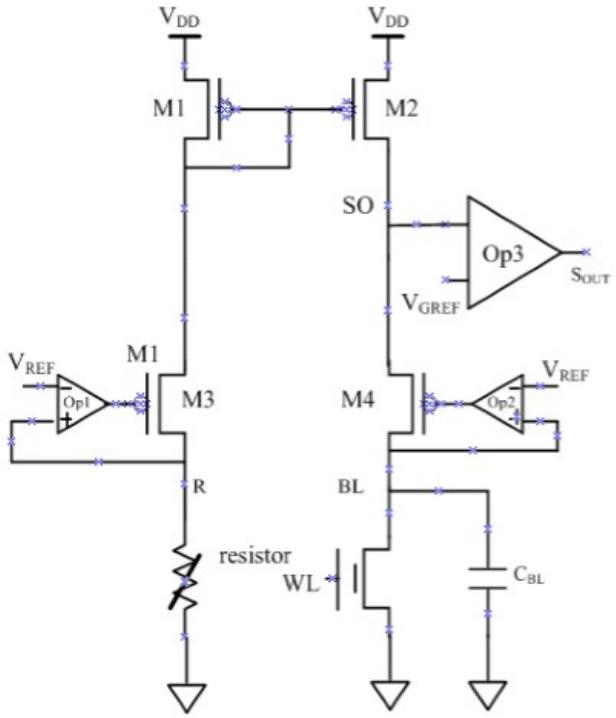

Fig.2. Circuit diagram of the proposed sense amplifier.

3. LOW-VOLTAGE SENSE AMPLIFIER

3.1 Description of new structure

The new sensing structure is illustrated in Fig.2, making much improvements compared to traditional structure. Firstly, the reference current is not generated by reference cell, but based on trimmable resistor, consequently, the voltage drop across R may vary with the need of power supply voltage, which enable the new structure to work at low power supply voltage. Secondly, two inverters used to control bit-line voltage in both BL clamp loop and reference path are replaced with operation amplifiers, which not only further lowers the power supply voltage required by biasing the bit-line voltage to desirable VREF but also reduces voltage variation due to the variation of temperature and process. Finally, the sensing output circuit uses an operation amplifier with one input generated by a global reference voltage VGREF generator for enhancing read access speed. When a read operation occurs, the system firstly completes pre-charge and maintains a stable voltage on the selected bit-line. Once pre-charge stage ends, the memory cell current ICELL flowing through transistor M4 into node SO is directly compared with reference current IREF mirrored by current mirror to node SO. Consequently, the voltage, VSO, converted from differential current between memory cell current and reference current is compared with global reference voltage, VGREF, by the comparator Op3 in the output circuit and then the comparison result is issued as output signal SOUT. In addition, the global voltage reference block provides a good voltage reference to be compared with voltage on node SO for right and high-speed output.

3.2 First Oder Modeling

Issues associated with protection of human rights and

First order modeling is necessary to drive the design before simulations. The objective of the sense amplifier is to achieve performance target in terms of access time and low voltage. We will firstly discuss the lowest work voltage from reference current generator circuit, sense core circuit.

the minimum power supply voltage for sense core circuit illustrated in fig.2 is given by

$$V_{DD,CELL} = V_{BL} + V_{DS(M4)} + V_{DS(M2)} \quad (3)$$

Where if

$$V_{BL} = V_{REF} = 0.7V \quad (4)$$

$$V_{DS(M4)} = 200mV \quad (5)$$

$$V_{DS(M2)} = 100mV \quad (6)$$

and then combine (3)-(6), we get

$$V_{DD(CELL)} = 1V \quad (7)$$

The lowest operation power supply voltage of the reference current generator circuit illustrated in fig.2 is given by

$$V_{DD(REF)} = V_R + V_{OV(M1)} + V_{T(M1)} + V_{DS(M3)}, \quad (8)$$

Where the voltage VR on node R can be regulated according to the need of power supply voltage. For example, when VT(M1), VOV(M1), VDS(M3) are respectively set at below voltage value.

$$V_{T(M1)} = 0.7V \quad (9)$$

$$V_{OV(M1)} = 0.15V \quad (10)$$

$$V_{DS(M3)} = 0.05V \quad (11)$$

Combine (9)-(11), if VR is set at 0.1V, we will get

$$V_{DD(REF)} = 1V \quad (12)$$

Consequently, the reference path can also work at low power supply voltage at 1V.

According to the equation (7) and (12), we can infer that the new structure of sense amplifier can work with low power supply voltage at about 1V.

Secondly, the read operation delay required in new sense amplifier is divided into three sections. The first section is the time TBL required for pre-charging the bit-line voltage to a desirable and stable voltage value. The second section is the time TSO required for differential current between ICELL and IREF to charge or discharge the lumped capacitance on node SO and the equation is given by

$$T_{SO} = \left(\Delta V * C_{SO}\right)/\Delta I \quad (13)$$

Where

$$\Delta V = \left|V_{SO} - V_{GREF}\right| \quad (14)$$

$$\Delta I = \left|I_{CELL} - I_{REF}\right| \quad (15)$$

CSO is metal line capacitance and parasitic capacitance on node SO, including CM2dg, CM4, Cdynamic (Dynamic Comparator Op3) and junction capacitance. The capacitance must be minimized taking amount of high-speed read access. The final section is the time Tdynamic required for sense output circuit to sense difference between VSO and VGREF and then issues the result in the form of SOUT. Consequently, the equation of read operation delay of new sense amplifier is given by

$$T_{total-delay} = T_{BL} + T_{SO} + T_{dynamic} \quad (16)$$

In addition, the global voltage VGREF must be designed carefully for optimizing the relation between read access time and read precision. It is apparent that the voltage VSO varies in [VBL, VDD], thus the voltage VGREF is designed to be nearly equal to (VBL+VDD)/2 through VGREF generator.

SIMULATION RESULTS

To verify the performance of the proposed sense amplifier, simulations are carried out and the corresponding simulation results are given in the paper. The simulated waveforms of the proposed sense amplifier under condition where VDD=1V are shown in Fig.3. Read voltage margin is defined as the voltage drop between VSO and VGREF at the beginning of dynamic sense enabled. As can be seen that read access time is divided into three sections including bit-line voltage precharge time , the time needed for charging or discharging capacitor of node SO to desirable value and dynamic sense pulse, which is identical to the anylysis in the first order model.

It well known that flash memory stores data-0 and data-1 in term of the charge quantity stored in floating gate of a memory cell. The quantity of electric charge implemented through injecting or extracting electrons into or from the floating gate of a memory cell corresponds to differential cell current in given bit-line voltage by affecting its threshold voltage. The simulated access time with respect to the selected memory cell current has been reported (VDD=1V, T=125 °, Normal Process) in Fig.4 where the cell current is distributed by the cell current of 0-data and 1-data. As can been observed new system need smaller sense time than old system, and sense time is not sensitive to cell current in individual region. A very limited access time variation can be expected due to the memory cell current variation with the proposed sense amplifier.

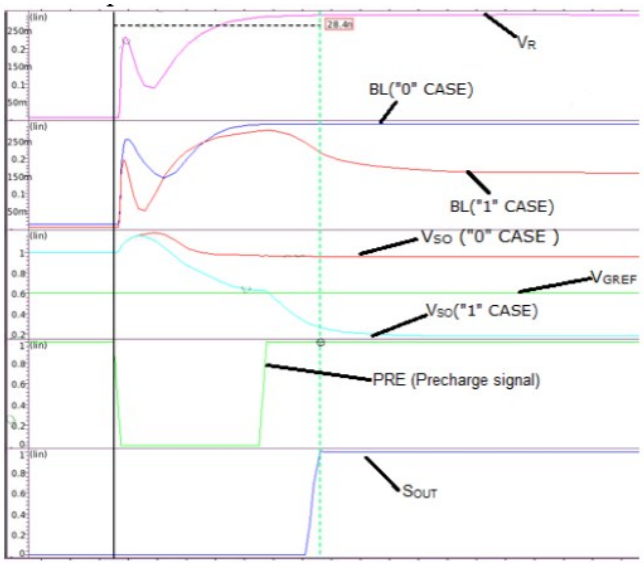

Fig.3. Simulated results of the proposed sense amplifier

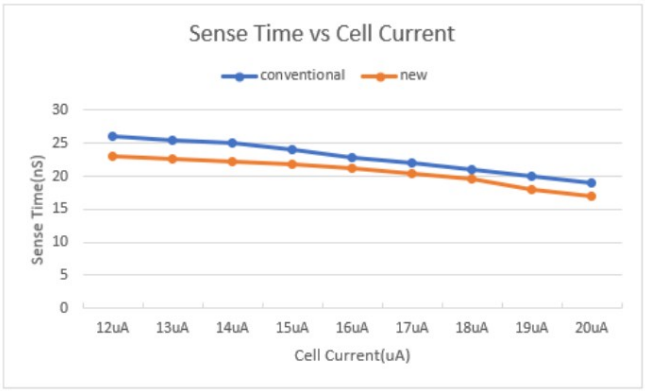

Fig.4. Sense time with respect to cell current

As the power supply voltage scales down, the performance of the sense amplifier degrades. Fig.5 illustrates the sense time with respect to the power supply voltage ranging from 1V to 1.9V using new proposed sense amplifier. As is clear that the sense time sensitivity is decreased using the proposed sense amplifier compared to the usual structure. Simultaneously, for VDD values at 1.5V, the proposed sense amplifier still works robustly but the usual one does not do. Therefore, the proposed sense amplifier is very suitable for low-voltage applications.

According to those above simulation results, the new structure has advantages over conventional sense amplifier that not only can it robustly work with low voltage at 1V while consuming smaller consumption than conventional sense amplifier but also it has smaller read access time than conventional structure.

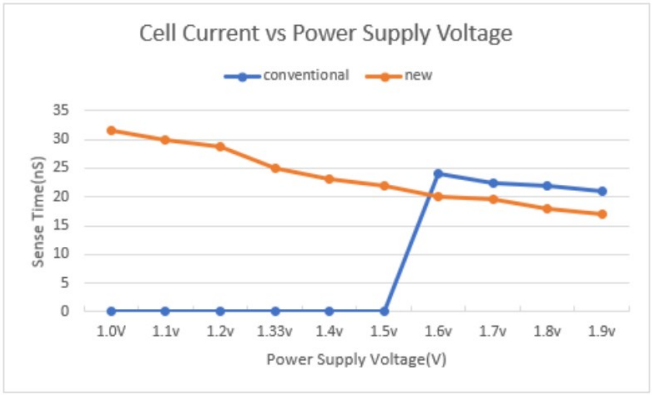

Fig 5. Sense time with respect to power supply voltage

CONCLUSION

This paper presents a new low-voltage sense amplifier for low-power-supply-voltage flash memories application. By taking use of trimmable resistor instead of reference cell to generate reference current in reference current generating circuit, the proposed sense can work at low power supply voltage at 1v. The capability of the sense amplifier presented in above paper is illustrated by simulation results.

BIOGRAPHICAL NOTES

Jiarong Guo is Lecturer of Internet of Things Engineering in the Department of Network Engineering in the School of Electronic Information Engineering at Shanghai Dian Ji University. She received her PhD from Shanghai University. Dr. Jiarong' current research interests are in areas related to the design of Flash Memory and MCU.

References

[1] Roy, K & Prasad, S. (2000). "Low Power CMOS VLSI Circuit Design," New York, NY, USA: Wiley Inter Science.

[2] Atsumi,S., Umezawa, A., et al. (2000). "A channel erasing 1.8-V-only 32 Mb NOR flash EEPROM with bit-line direct sensing scheme," Solid-State Circuits, 35(11), 1648-1653.

[3] Tanzawa, T., Takano, Y., Taura, T., & Nakamura, H. (2002). "Circuit State Circuits," vol. 37, no. 1, pp. 84–89.

[4] Tanzawa, T., Takano, Y., Taura, T. & Atsumi, S. (2000) "Design of a sense," 35(10), 1415–1421.

[5] Papaix, C. & Daga, J. M. (2002). "A new single ended sense amplifier for low voltage embedded

EEPROM nonvolatile memories," Proc Int Workshop on MTDT, 149-152.

[6] Soung-Hoon Sim, In-Wook Cho, Sang-Won Kim. et al. (2005) "A 130-nm 0.9 V 66-MHz 8-Mb (256Kx32) local SONOS embedded flash EEPROM," Solid-State Circuits, 40(4), 877–883.

[7] Conte, A., Giudice G. L., Palumbo, G., et al. (2005). "A high-performance very low-voltage current sense amplifier for nonvolatile memories," Solid-State Circuits, 40(2), 507-513.

[8] Liu Jiang, Wang Xueqiang, Wang Qin, et al. (2010). "A low-voltage sense amplifier for high-performance embedded flash memory." Journal of Semiconductors, l31(10), 105001-1~105001-5.

[9] Meng-Fan Chang, Che-Wei Wu, Chia-Chen Kuo, et al. (2012). "A 0.5V 4Mb logic-process compatible embedded resistive RAM (ReRAM) in 65nm CMOS using low-voltage current-mode sensing scheme with 45ns random read time", in Proc. IEEE ISSCC, 434-436

[10] Hua Zhang, Ling Lu. (2015). "A Low-Voltage Sense Amplifier for Embedded Flash Memories." Solid-State Circuits, 62(10), 236-240.