I J C T A, 9(20), 2016, pp. 357-367

Design of Low Power SISO & SIPO Shift Registers Using Lector Technique in 50 nm Technology

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ABSTRACT

In designing CMOS circuits, Power dissipation is considered to be a vital issue. In battery-powered applications, high power consumption causes reduction in the battery life and affects reliability, cooling costs and packaging. The development of digital integrated circuits is challenged by higher power consumption as we decrease the geometries of voltages scale, threshold voltages must also decrease to gain the performance advantages of the new technology, but leakage current increases exponentially increases leakage power. Now leakage power is increasingly important issue in processor hardware and software design. With the important component of leakage, the sub-threshold current, increasing exponentially as the device dimension decrease, leakage commands an ever increasing share in the processor power consumption. When Leakage current flows the circuit is idle and hence the power is wasted. For the deep submicron and nanometre circuit, efficient leakage power reduction techniques have become critical. In this paper, a 4-bit SISO and SIPO Shift registers are designed using LECTOR technique and is analysed with different types of sleep techniques. For designing, digital schematic editor (DSCH) is used. For simulation and layout generation Micro Wind Layout Editor is used.

Keywords: CMOS, Scaling, Leakage power, D flip-flop, Johnson Counter, Dual sleep, Dual stack, Stacked sleep, LECTOR

1. INTRODUCTION

Power consumption is one among many critical issues of VLSI circuit design, for which CMOS is the chief technology. The power consumption of CMOS consists of static and dynamic components. Dynamic power is consumed when transistors are switching while static power is consumed regardless the switching of transistors. Dynamic power consumption is considered to be the single largest concern for low-power chip designers as dynamic power is accounted for more than 90% of the total chip power. Nonetheless, as the feature size shrinks, e.g., to less than 90nm, static power has become a tough challenge for present and upcoming technologies.

The scaling of process technologies to nanometer has increased leakage power dissipation to a very large scale. Hence during inactivity periods, static power dissipation must be decreased to a great extent. The power reduction must be achieved without trading-off performance which makes it tougher to decrease leakage during normal operation. There are more VLSI methods to reduce leakage power [1]. One such technique is scaling which improves transistor density and functionality on a chip. It also increases speed and frequency of operation which results in higher performance. As the geometries of voltages scale is reduced, threshold voltages must also be reduced to achieve high performance advantages but leakage current will exponentially increase [2]. Power gating is one common technique where a sleep transistor is

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added in between actual ground rail and circuit ground (called virtual ground).In sleep mode, this device will be turned-off to cut-off the leakage path. In this paper, for designing 4-bit SISO and SIPO Shift registers we designed a new technique for reducing leakage power called LECTOR (LEakage Control TransisOR) using CMOS technology. Previous techniques are summarized and compared with our new approach in this paper.

2. SHIFT REGISTERS

Shift registers are one among the sequential logic circuits, mostly used for the storage of digital data. Here a set of flip-flops are connected in series so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers do not have specific internal sequence of states. All flip-flops are driven by same clock, and can be set or reset at the same time. Because the shift register stores data it is implemented using flip-flops. D flip-flop operation is used here.

Types of shift registers:

2.1. Serial In - Serial Out Shift Register

The serial in/serial out shift register accepts data in serial fashion i.e, one bit on a single line at one time. It produces the stored information on its output in serial form [6].

In order to get the data out of the register, they must be shifted out serially. When the control line is HIGH (ie WRITE) the data is loaded into the register and when the control line is LOW (i.e. READ) the data can be shifted out of the register.

When data is retrieved one bit at a time, it takes N clocks to retrieve N bits of data stored in N bit SISO shift register. So, the 4-bit shift register takes 4 clock pulses to retrieve the 4 bits stored in it. The important drawback in the operation of SISO shift register is that it is slow when compared to other shift registers but is very easye to implement and operate[10,11].

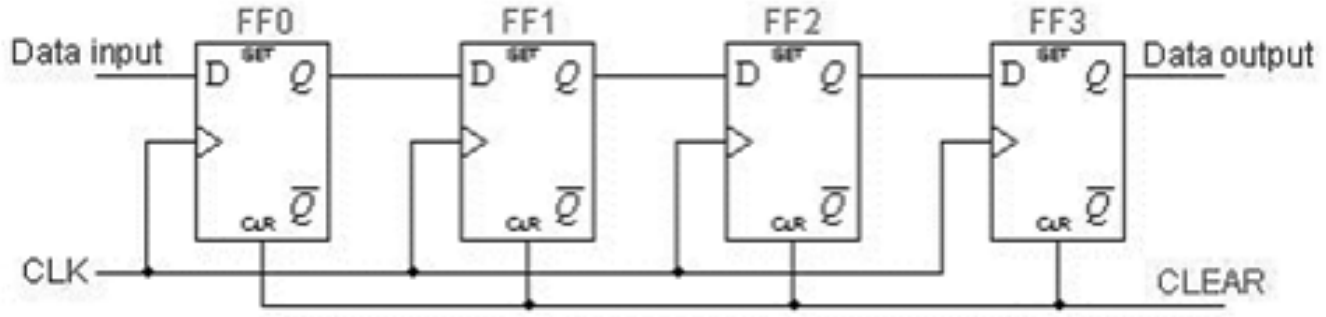

Figure 1: Four-Bit SISO Shift Register

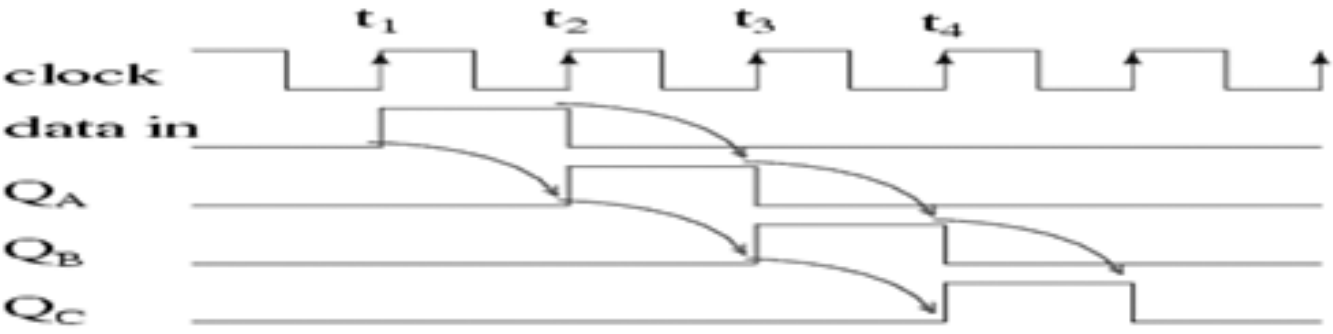

Figure 2 : Waveform of SISO Shift Register.

2.2. Serial In - Parallel Out Shift Registers

In this configuration it allows the conversion from serial to parallel form. Data is given in serial form and once the data has been clocked in, it can be either read at each output at the same time, or can be shifted out In this configuration, each flip-flop is edge triggered. The first flip-flop operates at the given clock frequency and every subsequent flip-flop operates at half the frequency of its predecessor and doubles its duty cycle. Hence, to trigger each subsequent flip-flop it takes twice the rising/falling edge period and this staggers the serial input in the time domain, leading to parallel output. In case if we do not require the parallel outputs to change during the serial loading process, it is desirable to use a buffered or latched output. In latched shift register (such as the 74595) the serial data is first loaded into an internal buffer register, then on the receipt of a load signal, the state of the buffer register is then copied into a set of output registers. In general, serial-in/parallel-out shift registers are used to convert data from serial form on a single wire to parallel form on multiple wires [8, 9].

A construction of a four-bit serial in - parallel out register is shown below

In the waveform below, the four-bit binary number 1001 is shifted to the Q outputs of the register.

3. SLEEP TECHNIQUES

3.1. Dual Sleep Transistor Approach

There are different methods of leakage power reduction. One of such method is dual sleep transistor approach. It uses two extra pull- up and two extra pull-down transistors in sleep mode either in On state or OFF state. The dual sleep portion is common to all logic circuitry.

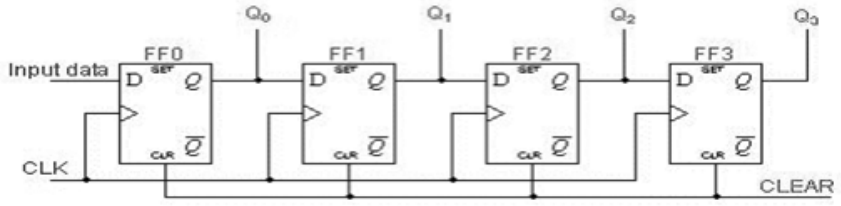

Figure 3: Four-Bit SIPO Shift Register.

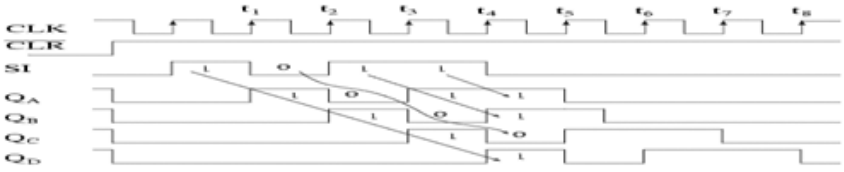

Figure 4: Waveform of SIPO shift register.

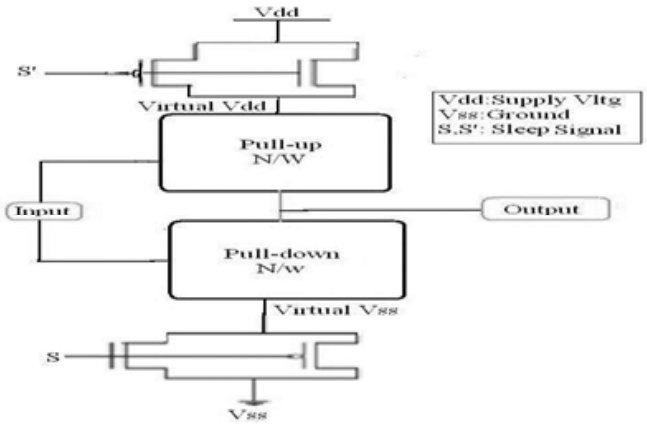

Figure 5: Dual Sleep Transistor Approach

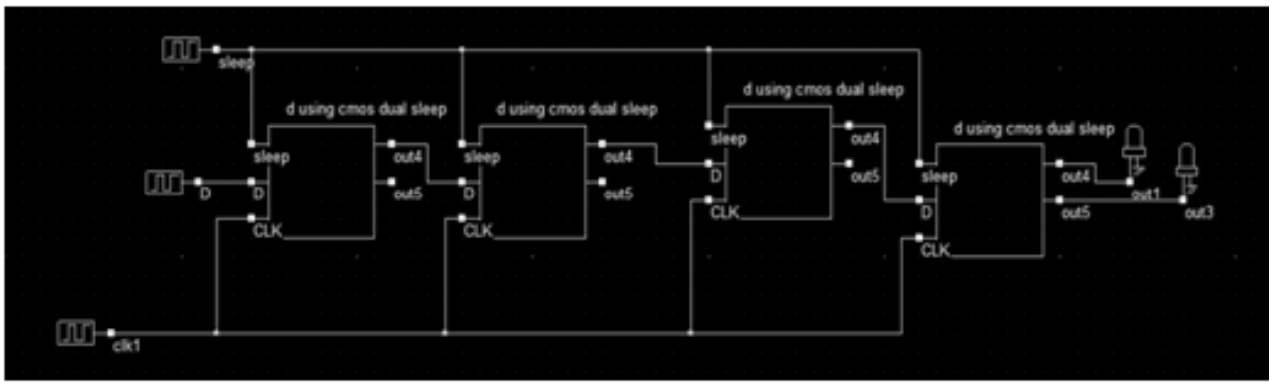

Figure 6: Block Diagram of SISO using dual sleep

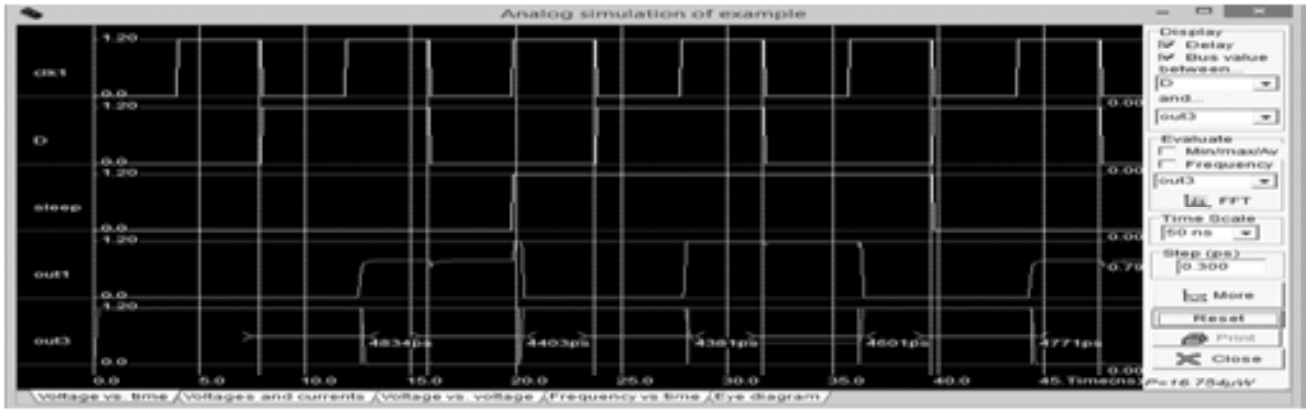

Figure 7: Simulation result of SISO using dual sleep

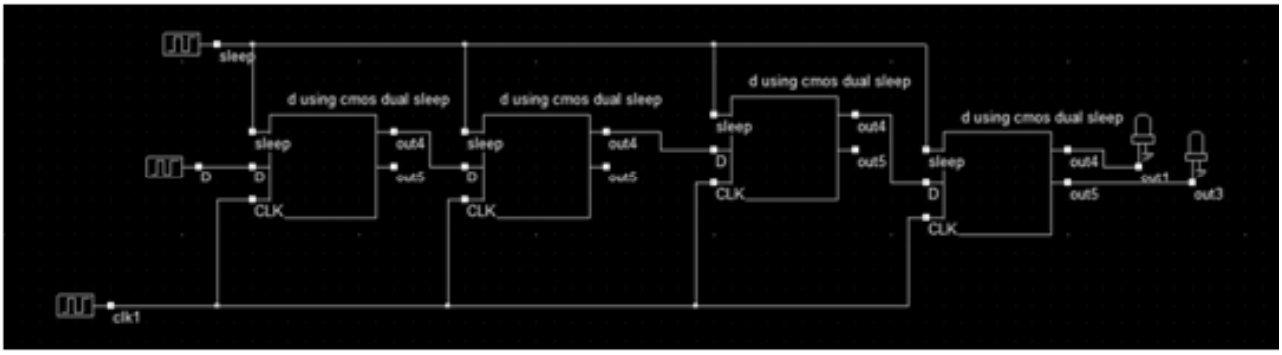

Figure 8: Block Diagram of SIPO using dual sleep

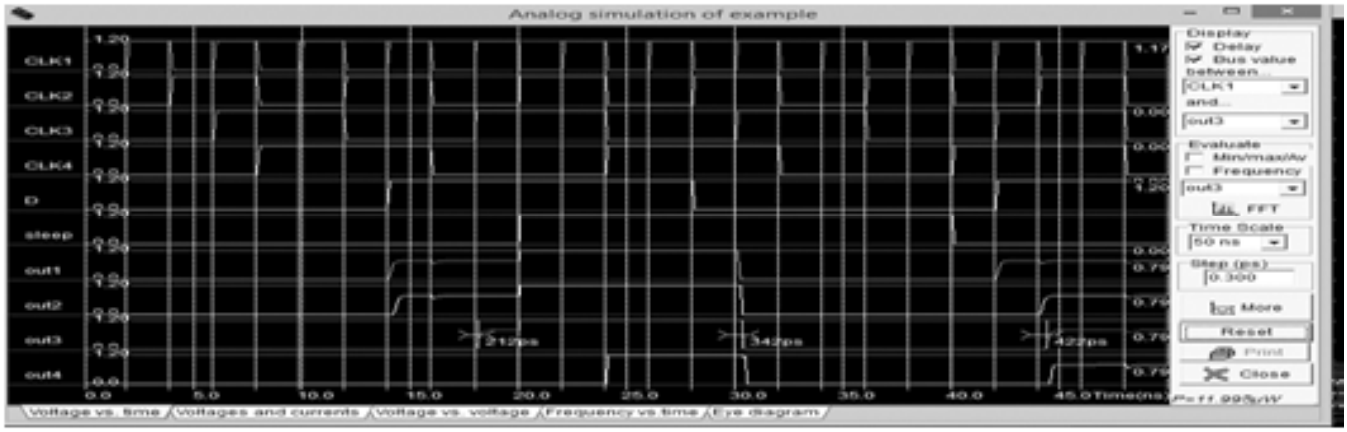

Figure 9: Simulation result of SIPO using dual sleep

3.2. Dual Stack Approach

In this approach, 2 NMOS in the pull-up network and 2 PMOS in the pull-down network are used in addition to the sleep transistors. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level.

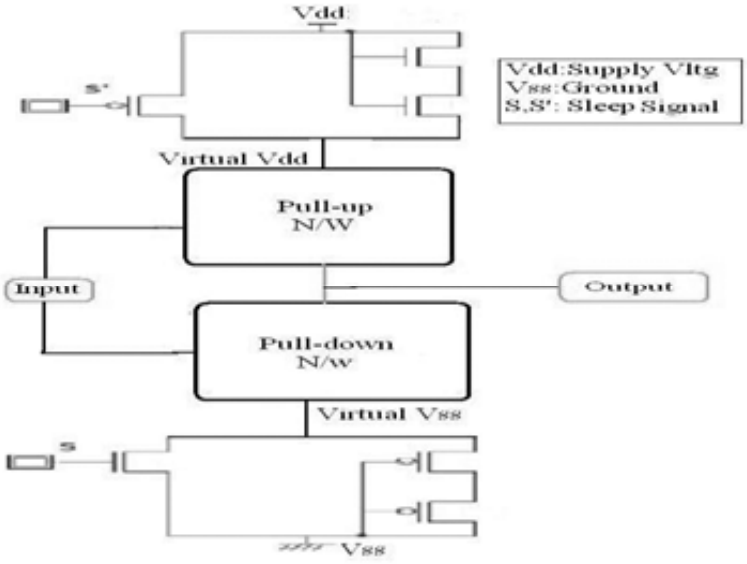

Figure 10: Dual Stack Approach

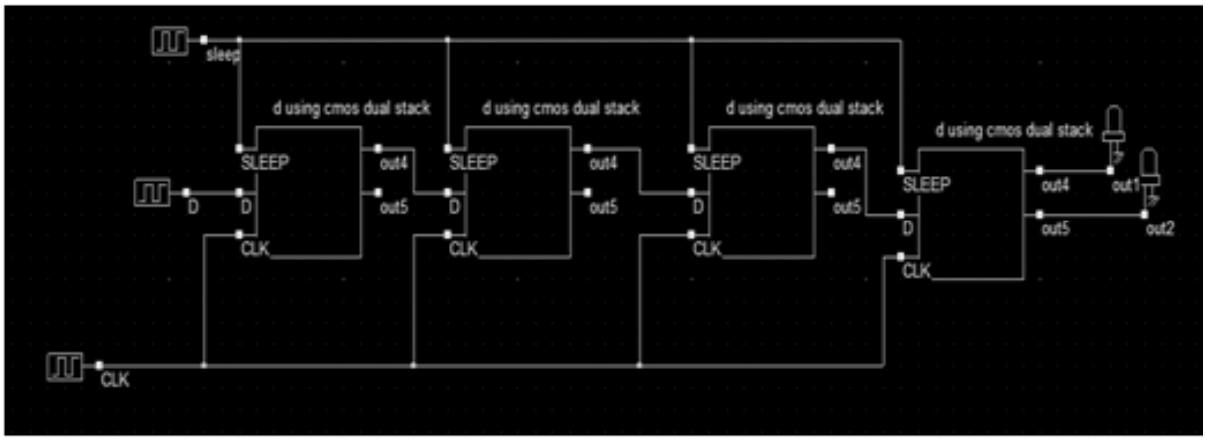

Figure 11: Block Diagram of SISO using dual stack

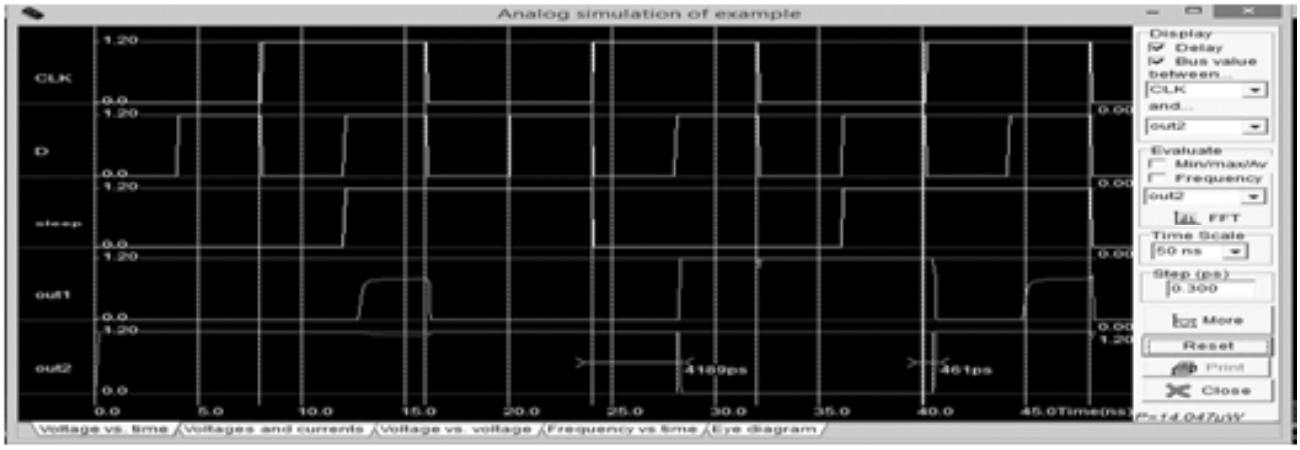

Figure 12: Simulation result of SISO using dual stack

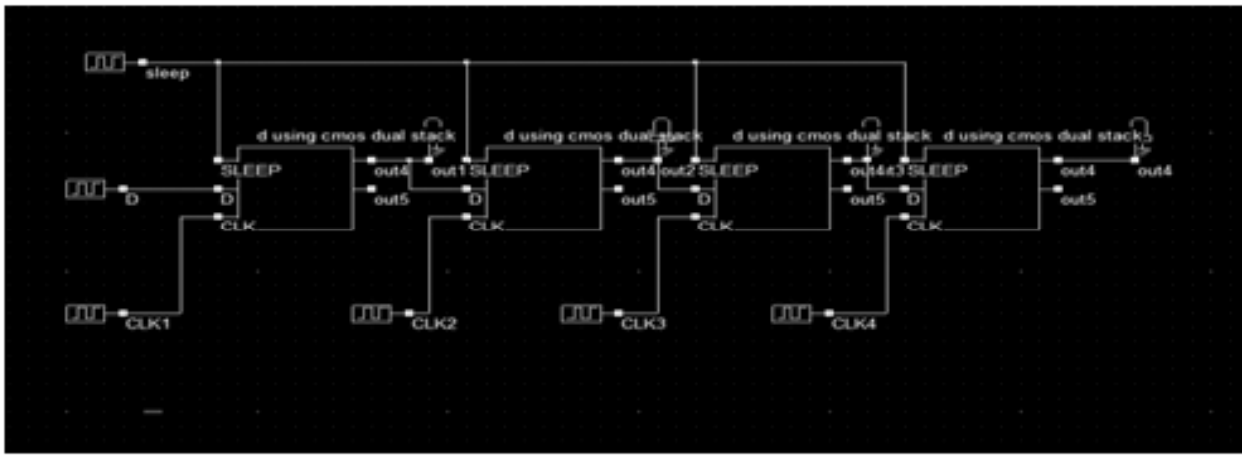

Figure 13: Block Diagram of SIPO using dual stack

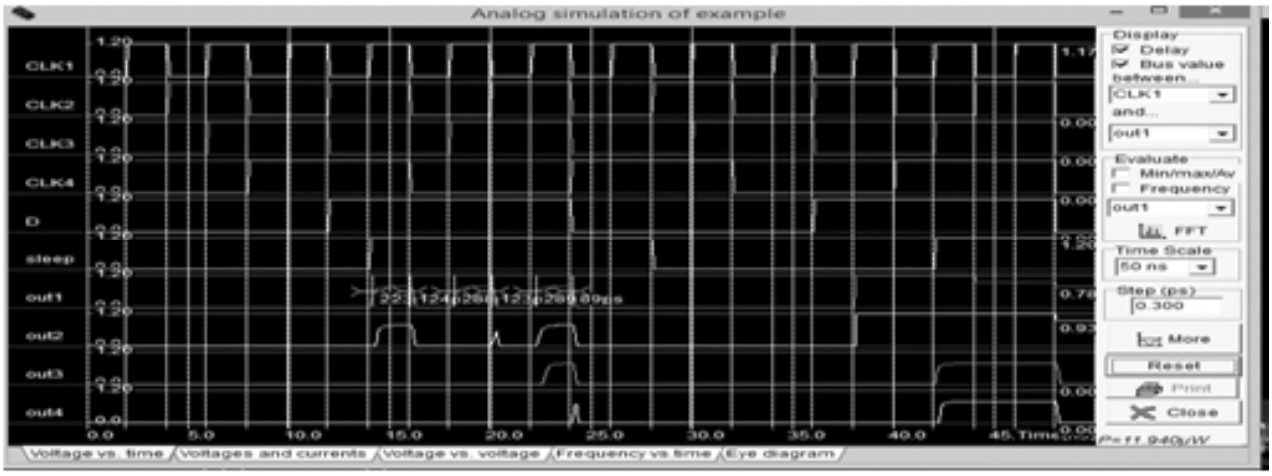

Figure 14: Simulation result of SIPO using dual stack

3.3. Stacked Sleep Transistor Approach

In Stacked Sleep Transistor Approach, sleep transistor is stacked, which decreases the leakage current to maximum extent. In this technique, two stacked sleep transistors near power supply rails and two more stacked sleep transistor near ground is used. Thus leakage reduction takes place in two steps, first due to stack effect of sleep transistor and then due to sleep transistor itself. It is well known that NMOS are not efficient in passing the power supply. So in this approach, stacked sleep transistor uses PMOS in the power supply and NMOS in the ground for maintaining the exact logic state of the circuit.

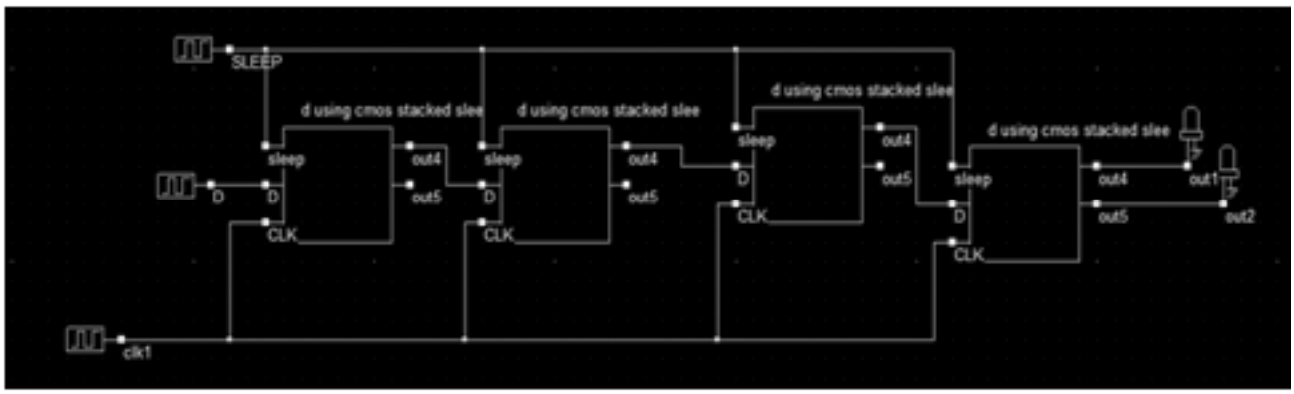

Figure 15: Block Diagram of SISO using stacked sleep

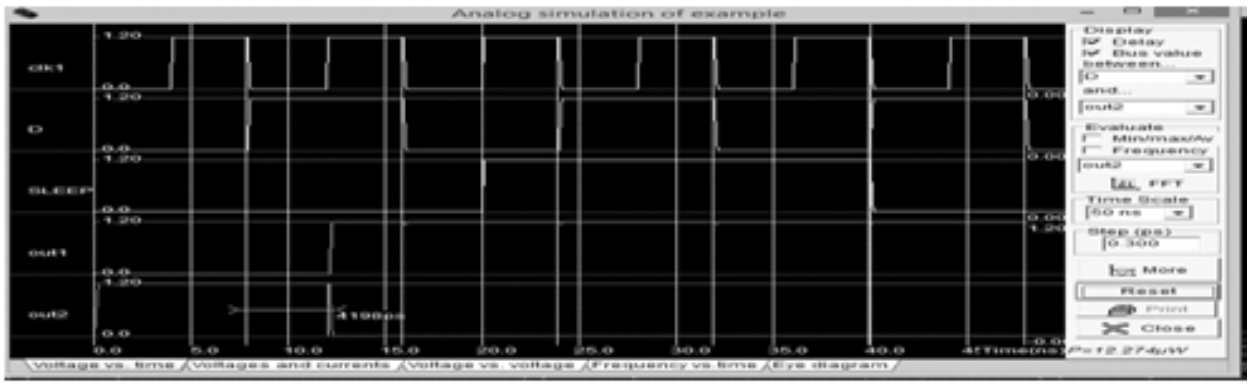

Figure 16: Simulation result of SISO using stacked sleep

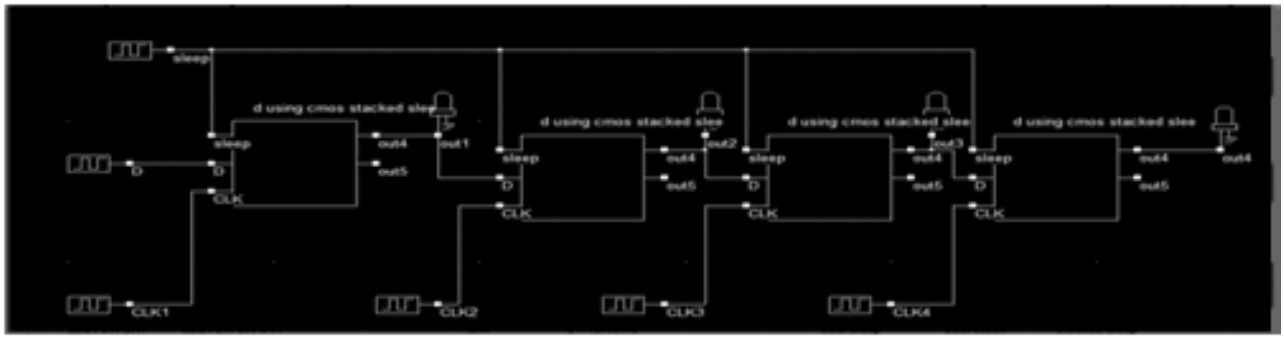

Figure 17: Block Diagram of SIPO using stacked sleep

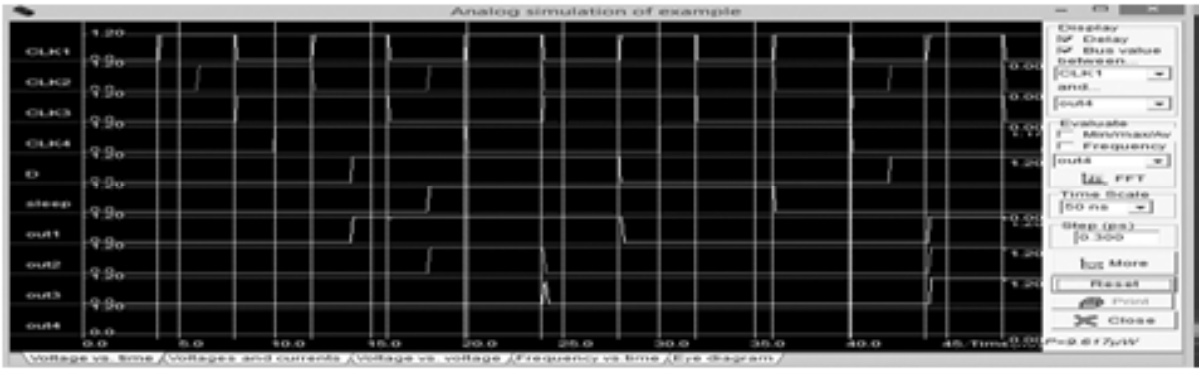

Figure 18: Simulation result of SIPO using stacked sleep

4. PROPOSED TECHNIQUE

The proposed technique for leakage reduction in CMOS circuit is called LECTOR. It provides two Leakage Control Transistors (LCT's), a p- type and a n-type within the logic gate in which the source terminal of one LCT controls the gate terminal of the other. LECTOR is effective in both active and idle states of the circuit so it has better leakage reduction. Either one of the two LCT's will always be "near its cut- off voltage" for every input combination, thus increasing the stacking effect without any additional control signal.

It works on the fact that a state with more than one transistor off in a path from supply voltage to ground is very less leaky than a state with only one transistor off in any supply to ground path. The LCT's are self-controlled and do not require any control logic unlike in the mostly used sleep transistor method. [12]

5. COMPARISON TABLE

We compare the LECTOR technique with different sleep techniques in terms of power consumption and the results are tabulated.

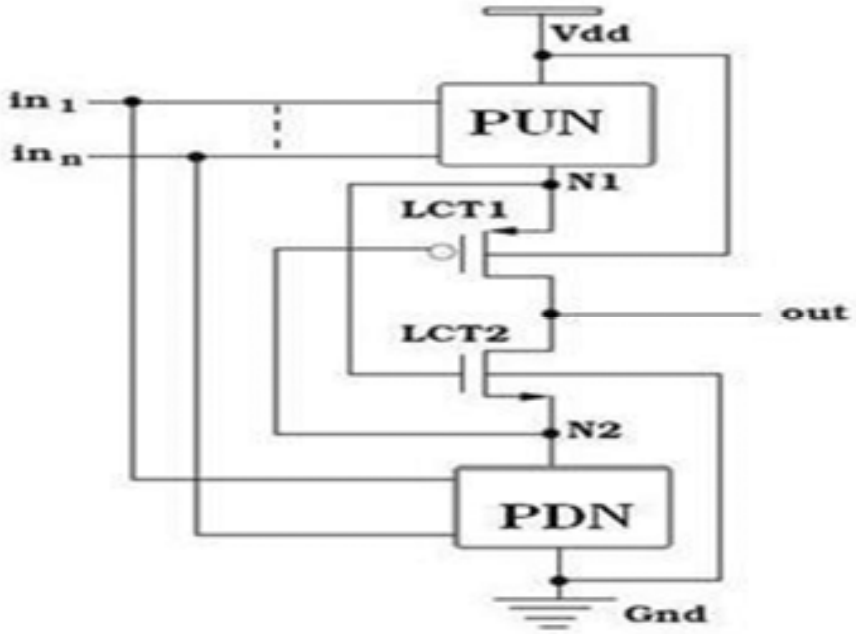

Figure 19: Lector technique

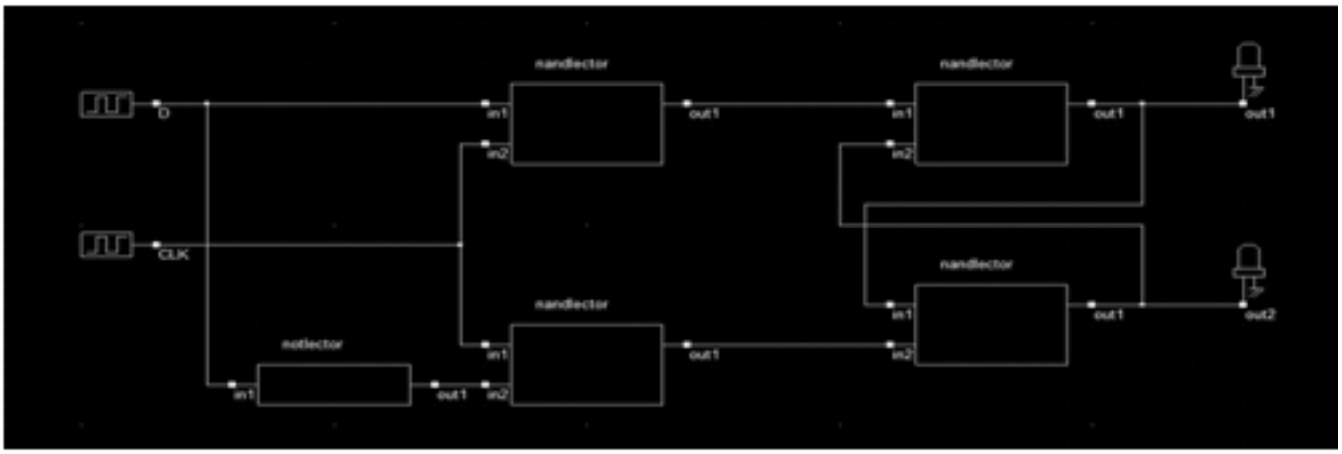

Figure 20: Block Diagram of D Flip Flop using Lector technique

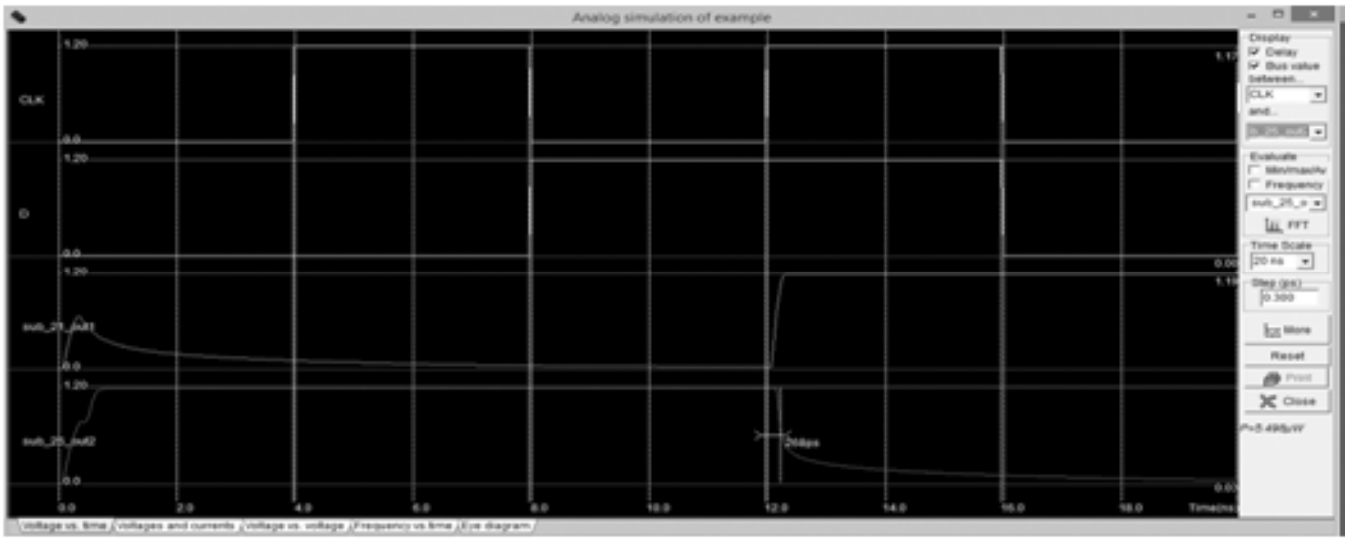

Figure 21: Simulation Result of D Flip Flop using Lector technique

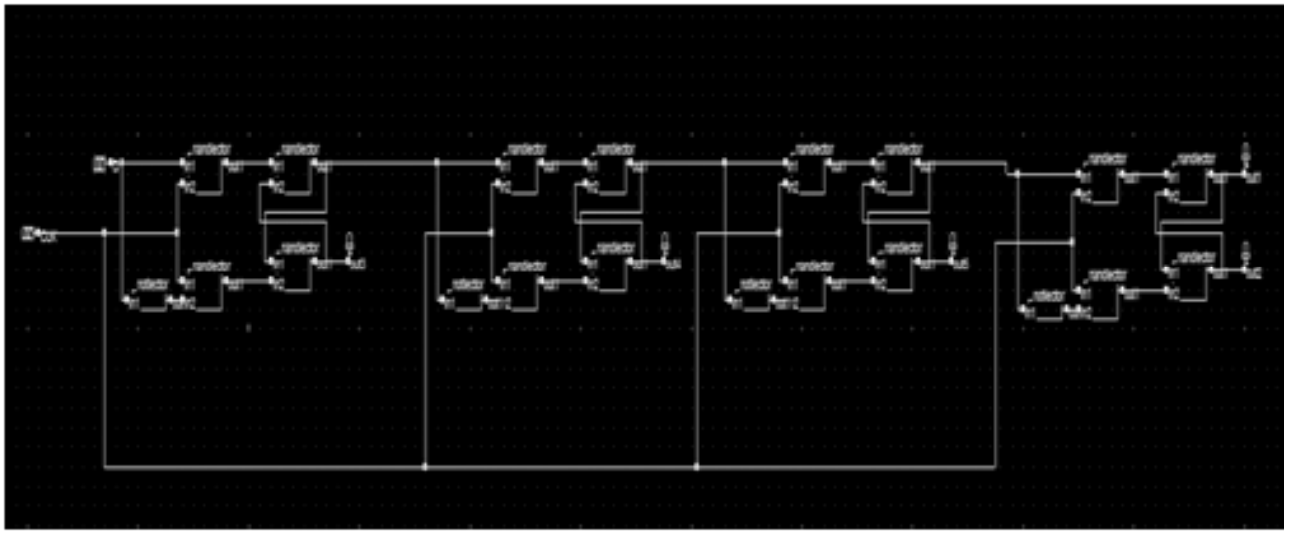

Figure 22: Block Diagram of SISO using Lector technique

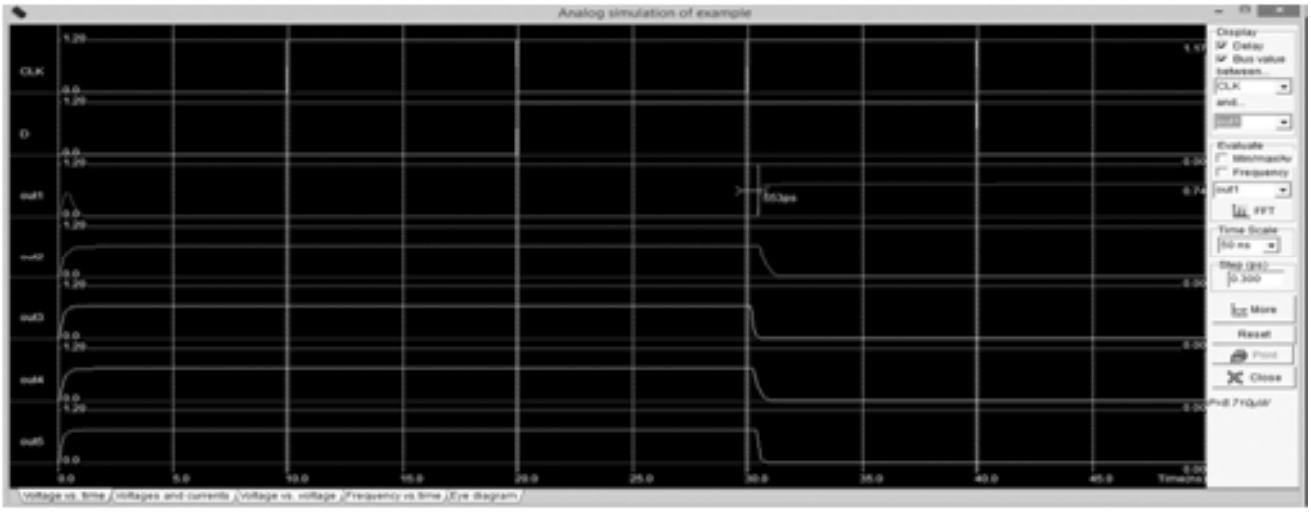

Figure 23: Simulation Result of SISO using Lector technique

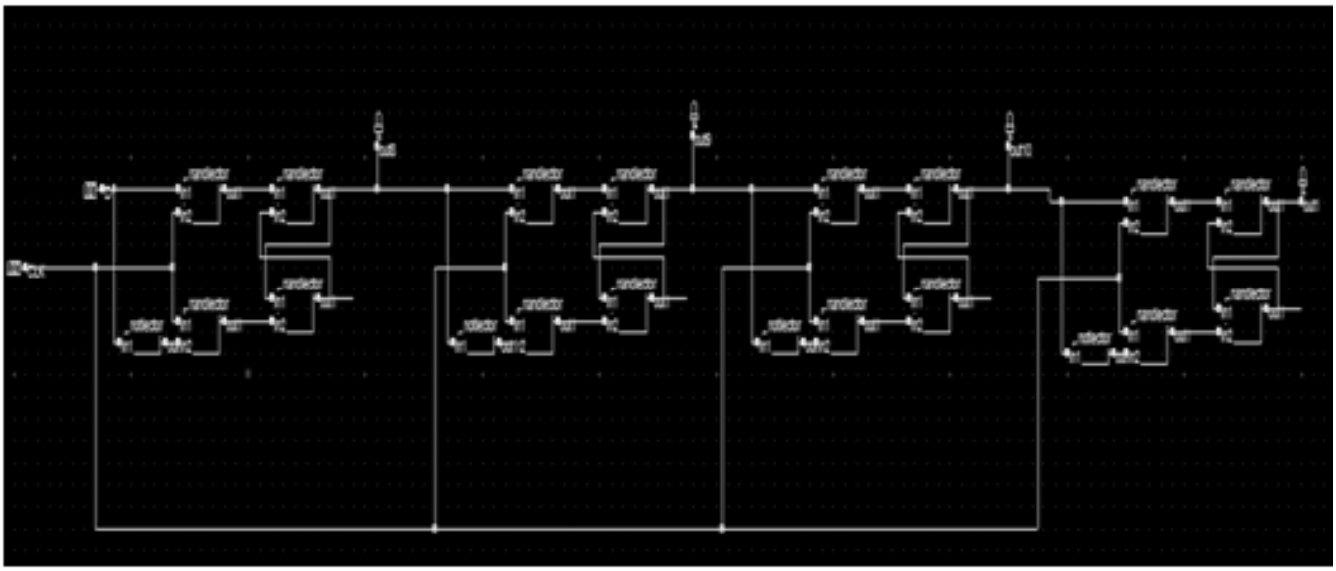

Figure 24: Block Diagram of SIPO using Lector technique

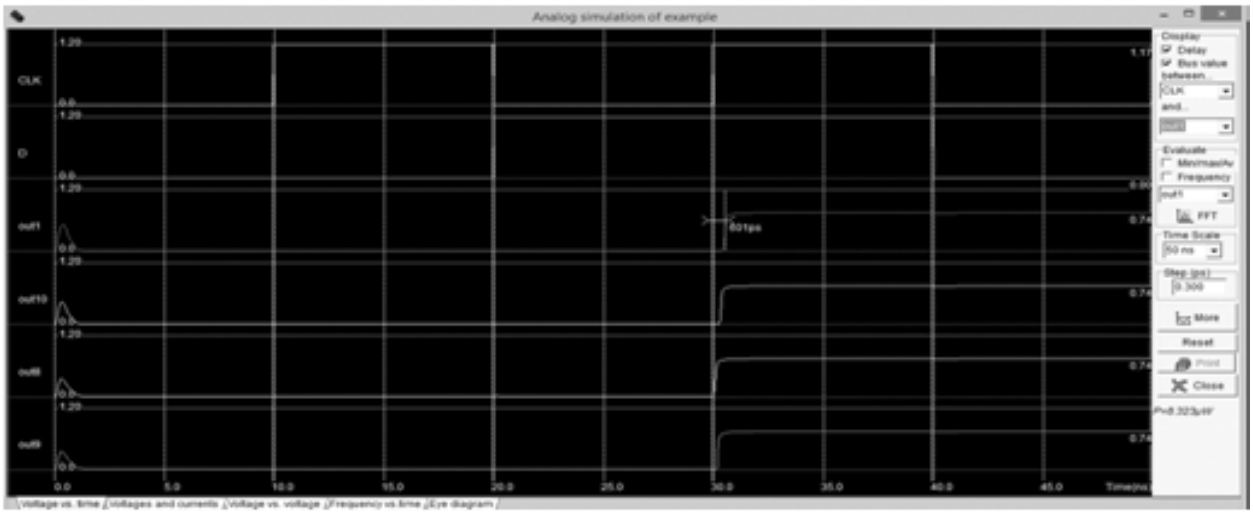

Figure 25: Simulation result of SIPO using LECTOR technique

Table 1
Comparison table of power dissipation of d- flip flop and shift register types in all sleep techniques and proposed technique.

APPROACH(μm)	D-FLIP FLOP(μm)	SISO(μm)	SIPO (μm)
LOGIC GATES	7.542	27.855	4.752
CMOS	12.579	27.263	12.399
DUAL SLEEP	7.512	16.754	11.995
DUAL STACK	6.699	14.047	11.940
STACKED SLEEP	6.713	12.279	9.617
LECTOR	5.492	8.710	8.323

6. CONCLUSION

Sub threshold leakage power consumption in nano scale technology is great challenge to VLSI designers. Though there are several techniques to reduce leakage power, based upon the technology and design criteria the designer can choose the techniques. In this paper, Power consumption of 4-bit PISO and PIPO Shift Register is reduced using different sleep methods and LECTOR technique. Compared with other leakage control techniques, LECTOR does not require any additional control circuitry to monitor the states of the circuit. Also the power consumption is greatly reduced using LECTOR technique with minimum possible area and this method can be used in several integrated circuits for power efficiency.

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