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# An Efficient Bridge-Less Power Factor Correction Tapped Inductor based SEPIC converter For BLDC Motor Application

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**ABSTRACT**

Due to the intensified BLDC motor applications in recent decades, Power factor correction (PFC) converters have attracted several researchers. In previous research works, SEPIC converter with the Tapped Inductor model operating in Discontinuous Conduction Mode (TI-SEPIC-DCM) to produce significant results. This work proposes a novel idea of bridgeless rectifier for PFC to enhance rectifier power density for the BLDC Motor applications. Moreover, due to the introduction of the bridgeless rectifier in TI-SEPIC Converter which operates in DCM, noise emissions are eliminated significantly. A third order harmonic reduction control loop has been proposed for better harmonic mitigation. The proposed work has been simulated in MATLAB and the results are validated for dynamic speed varyng conditions of the BLDC motor. The proposed BL-TI-SEPIC-DCM approach provides significant results with almost unity power factor and minimal THD.

***Keywords:*** Tapped Inductor (TI) converter, high gain converter, Bridgeless Power Factor Correction (BL-PFC) converter, voltage source inverter (VSI), BLDC motor drive.

## 1. INTRODUCTION

Power supplies having active power factor correction (PFC) methods are necessary for an extensive range of applications for the purpose of communication, automotive, computer and biomedical industries. All these applications are expected to satisfy the industry standards like the IEC 61000-3-2. Furthermore, it is greatly recommended to adhere to new Industry standards like the 80 PLUS initiative. Several papers have been written in the literature for providing a solution for the case of single-stage power factor correction (PFC) integrated topologies [1-7]. These solutions have been resourceful in providing cost-efficient approach for attaining both the functionality of high PFC and fast output voltage control.

Many of the PFC rectifiers make use of boost converter at their front end. Boost converter yield several benefits like natural power factor correction capacity and simple control [8]. Nonetheless, low voltage applications like telecommunication or computer industry need an extra converter or an isolation transformer for stepping down the voltage. But, the traditional arrangement of boost has lesser efficiency because of considerable losses in the diode bridge [1]. Additionally, boost converters are affected by high inrush current that also increases the cost incurred in the safety required disconnection devices present between the load and the line voltage. In order to reduce the losses of the full bridge, several bridgeless PFC rectifiers have been proposed for improving the rectifier power density and/or minimized emissions of noise [2]-[5] through the soft switching methods or coupled magnetic topologies.

Many non-boost bridgeless rectifiers have been presented in the literature in the recent times [9]-[10]. A bridgeless PFC rectifier on the basis of the Sepic topology is introduced in [11]. Nevertheless, the topology

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consists of only a step up capability just as a boost transformer; but, an isolation transformer can be utilized for stepping down the voltage, thereby leading to an increase in the cost and also size of the rectifier.Although Cuk converter topology is generally a converter with lesser efficiency, but it has various benefits, like isolation capability, step up/step down output voltage, constant output current and lesser electromagnetic emissions.

In contrary, a Single-Ended-Primary-Inductor (SEPIC) Converter is a type of dc-dc converter that permits the electrical potential(voltage) at its output to be presented greater than, less than, or even equal to that of its input. SEPIC is regulated by the duty cycle corresponding to the control switch. It has inherited the merits of possessing a true shutdown and non inverted output. There are significant chances to accomplish a high voltage gain using this converter. SEPIC converters are chiefly employed in industrial applications. This converter functions at a pre-determined switching frequency and duty ratio. This converter demonstrates a good response speed also. SEPIC converters are appropriate for those applications which need high voltage step-up. Because of its huge range of applications it would be advantageous in case the voltage gain of the converter has raised to some high value in an effective manner.

In a quest for higher voltage gain and efficiency, several innovative schemes have been formulated in recent literature. These comprise application of multipliers, switched capacitor/ inductor hybrid structures, voltage-lift, and cascaded boost converters. In general, these schemes bring about increased component count and cost in addition to control complexity. Tapped Inductor (TI) kind of converters are an option, which provides simple circuit and low part count. The TI boost (TI-boost) converter [11] can accomplish much more gain than its fundamental counterpart simply by adjusting the turn's ratio. TI can be introduced to other conventional dc–dc converters also. TI-flyback [12], TI-cascaded boost [12]; TI-SEPIC [13], [14] and TI-ZETA [15] topologies have been reported. The conventional DBR based PFC TI-SEPIC model is shown in Figure 1.

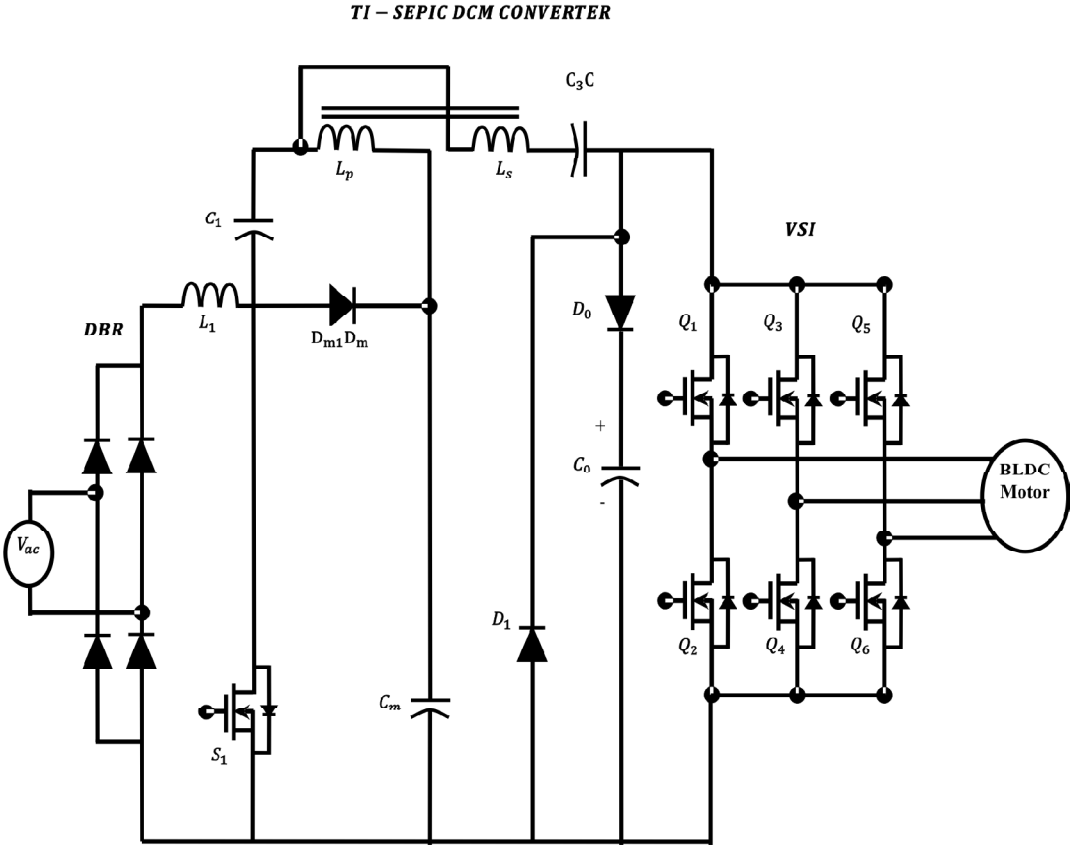
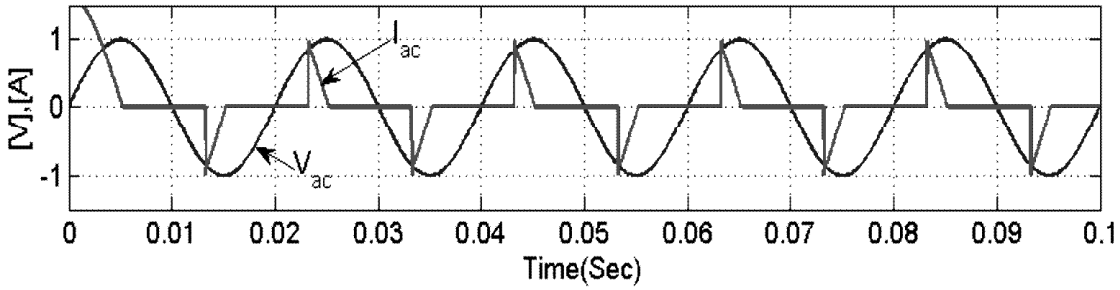
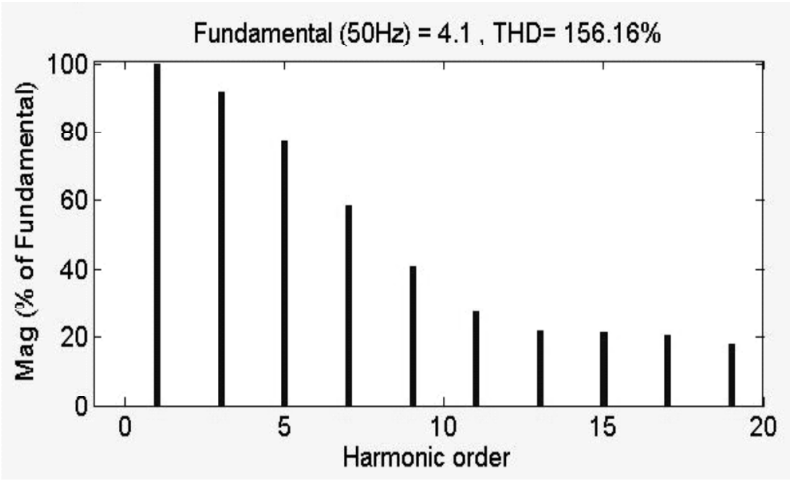



**Figure 1: Conventional DBR based TI-SEPIC Converter**

As shown from the Figure 1, a diode bridge rectifier (DBR), followed by a high value of the dc link capacitor feeding a voltage source inverter (VSI) - based BLDC motor, draws peaky current from supply and injects a high amount of harmonics in the supply system [16]. This results in a poor power factor (as low as 0.7) and high total harmonic distortion (THD) of supply current (as high as 65%) at the ac mains is shown in Figure 2(a) and 2(b). Such power quality indices are not acceptable by international power quality standard IEC 61000-3-2 [9].




(a)




(b)

**Figure 2: Waveforms of (a) Supply Voltage and Supply Current (b) Harmonic Spectra of Supply Current**

In order to increase the power supply efficiency, significant research efforts have been aimed towards the design of bridgeless PFC converter circuits with extended gain range, where the number of semiconductors producing losses is minimized by essentially removing the full bridge input diode rectifier. In the recent times, multiple bridgeless PFC rectifiers have been proposed for the purpose of improving the rectifier power density and/or minimize noise emissions through soft-switching techniques.

## 2. PROPOSED METHODOLOGY

This research work introduces a novel bridgeless SEPIC converter along with the TI model functioning in Discontinuous Conduction Mode (BL TI-SEPIC DCM) having an extended gain range for the case of BLDC motor drive applications. The sschematic diagram of the BL TI-SEPIC DCM converter proposed and the convention of the circuit variables that are adopted is illustrated in Figure 3.

This converter circuit consists of an input inductors $L_1$ and $L_2$; the main switches $S_1$ and $S_2$; intermediate capacitors $C_1$ and $C_2$; A voltage multiplier cell is then included in the circuit, which comprises of $C_m$, $D_{m1}$ and $D_{m2}$; a Tapped Inductor (TI) of $L_p$, $L_s$; and a charge pump also finds its inclusion in the circuit that

incorporates $C_3$, $D_1$ and $D_0$, powering an output filter capacitor, $C_0$, and at last a VSI fed BLDC motor drive.

In the topology proposed the usage of bridgeless configuration will minimize the losses associated with conduction and the voltage multiplier cell will maximize the gain and limit the switch voltage stress. Therefore, this new topology improves the efficiency on the whole. The circuit proposed has two symmetrical configurations. Every configuration will function in a half-line cycle. Through the implementation of two slow diodes $D_p$ and $D_n$, the output ground is connected at all times to the ac mains terminals directly over the entire ac line cycle. Consequently, this helps in the stabilization of the voltage potential of the output ground and limits the generation of common mode EMI.

The converter proposed makes use of two nonfloating switches ($S_1$ and $S_2$). Switch $S_1$ is turned ON/OFF at the time of the positive half-line cycle with the current flowing back to the source by means of diode $D_p$. During the duration of the negative half-line cycle, switch $S_2$ is switched ON/OFF and the current flows back through the diode $D_n$. Furthermore, the two power switches $S_1$ and $S_2$ can be powered by the same control signal that considerably helps in the simplification of the control circuitry.

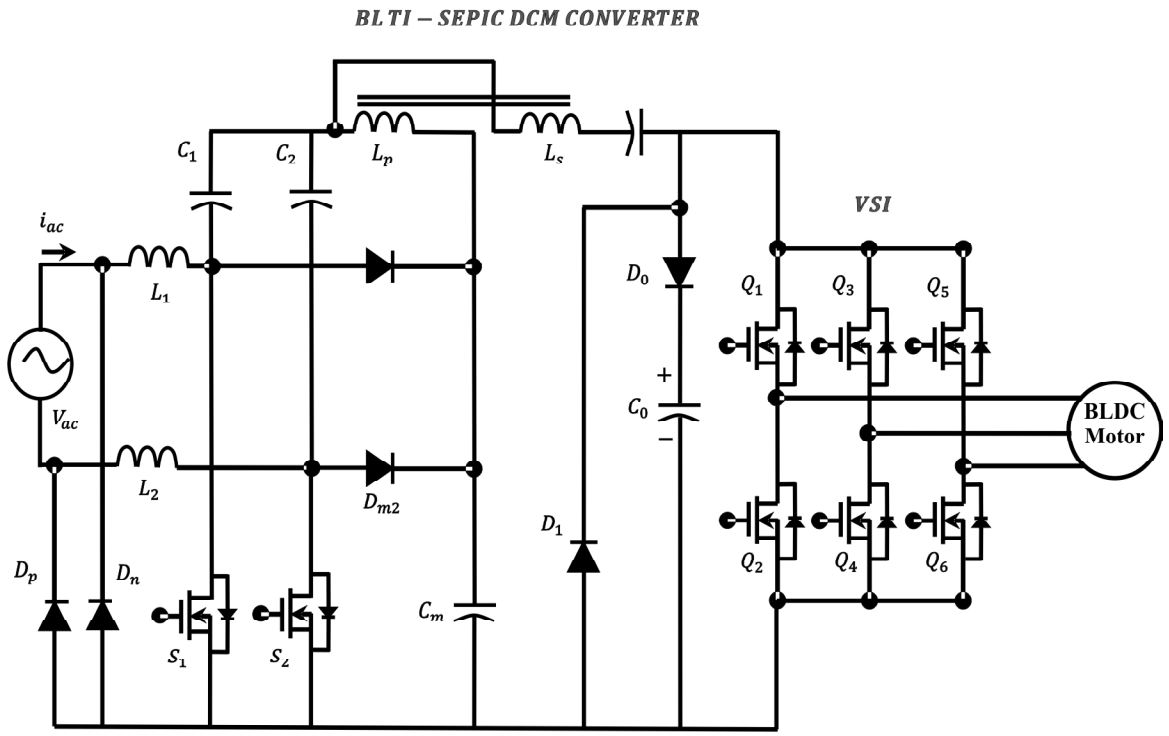



**Figure 3: Schematic Diagram**

Figure 3 schematic diagram of proposed BL TI-SEPIC DCM converter fed BLDC motor drive

This converter is designed from the basic SEPIC topology [17]. It is seen evidently from the Figure 3, the inductor is exchanged with TI for accomplishing higher voltage gain. More addition to the increase in voltage gain is accomplished by means of the process of application of a voltage multiplier cell. Furthermore, the integrated "voltage multiplier cell" helps in the proposed converter gaining Zero-Voltage (ZV) and Zero-Current (ZC) switching that improves the efficiency, and, possibly, allows a greater switching frequency and reduction in size.

This converter topology has an additional benefit. If the switch, $S_1$ or $S_2$, is turned on, the charge pump capacitor, $C_3$, ties the anode voltage corresponding to the output diode, $D_0$, to ground. This way, the voltage stress of $D_0$ is devoid of the TI turns ratio and similar to the output voltage. This reduces the switching

losses associated with $D_0$ and is termed an extra advantage of this converter. Additionally, this converter is developed in order to operate in DCM for achieving nearly a unity power factor and a less Total Harmonic Distortion (THD) of the input current. The operation of DCM yields extra merits such as control circuitry that is simple i.e. only one voltage sensor is required for controlling this converter.

## 3. PRINCIPLE OF OPERATION

The BL TI-SEPIC DCM converter proposed which is functioning in DCM has three stages of operation. This circuit contains three inductors; in accordance, various combination of inductor values can be employed for the operation of DCM. For the purpose of reducing the input current ripple corresponding to the preregulator, a relatively high value for the inductor $L_1$ and $L_2$ is used. A considerable low value of the Tapped Inductor (TI) is exploited for the operation of the converter in DCM in the form of a voltage follower, in which the input current follows the input voltage waveform. Based on this, the preregulator input current does follow the input voltage waveform having lesser current ripple, with no input filter and no current-control loop.

In lieu of the fact that the circuit proposed is assessed for the entire switching period is indicated in Figure 4. Considering that the three inductors are working in DCM, and thereafter the circuit operation during the period of one switching can be split into three different operating modes, as illustrated in Figure. 4(a)–(c), and it can be explained as below.

### Mode 0

When the switch $S_1$ is turned on by means of the control signal, and both the diodes $D_p$ and $D_1$ are forward biased, As a result, the input voltage, $V_{ac}$, is applied across the inductor, $L_1$, and the input current, $i_{L1}$, begins shooting up, while the multiplier cell capacitor $C_m$ begins to discharge through the switch $S_1$, hence the voltage that is applied across TI(Lp) is equivalent to the voltage of capacitor $C_m$ subtracted by the voltage of capacitor $C_1$, and the diodes $D_{m1}$ and $D_{m2}$ gets blocked at this stage of operation. Moreover, capacitor $C_3$ starts to charge from TI (Ls) through switch $S_1$, as illustrated in Figure 4(a).

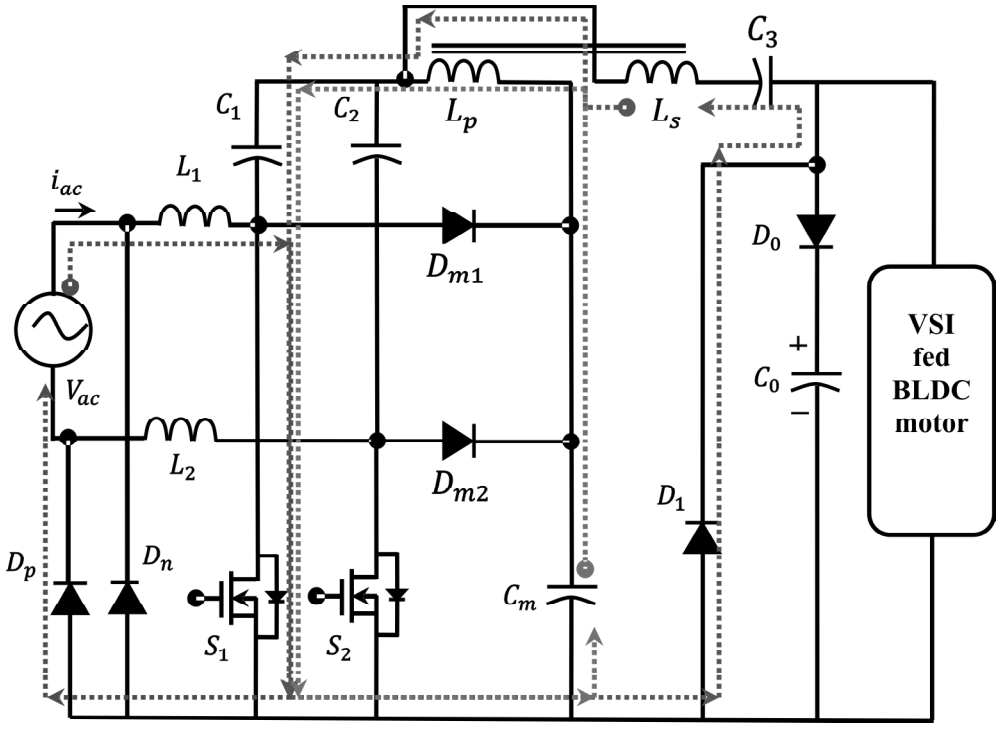



**Figure 4(a): Mode 0 Operation**

**Mode 1**

If the power switch $S_1$ is turned off, the supply current and the energy which is stored in the input inductor $L_1$ is carried over to the multiplier cell capacitor $C_m$ by capacitor C1 and TI(Lp), and both the diodes $D_{m1}$ and $D_p$ are forward biased at this stage of operation. There also exists transference of energy to $C_m$ capacitor via diode $D_{m1}$ and the maximum switch voltage equals the $C_m$ capacitor voltage. Next, the secondary side of tapped inductor TI (Ls) maintains to discharge the secondary current, via the diode $D_0$ to the output capacitor $C_0$. At this stage the capacitor $C_0$ voltage was raised in a steep manner, as the energy stored in the TI(Ls), capacitor $C_3$, energy in main supply $V_{ac}$, input inductor $L_1$ and capacitor $C_1$ is then transmitted to the capacitor $C_0$ (i.e. high gain is received at this stage of operation) as illustrated in Figure 4(b).

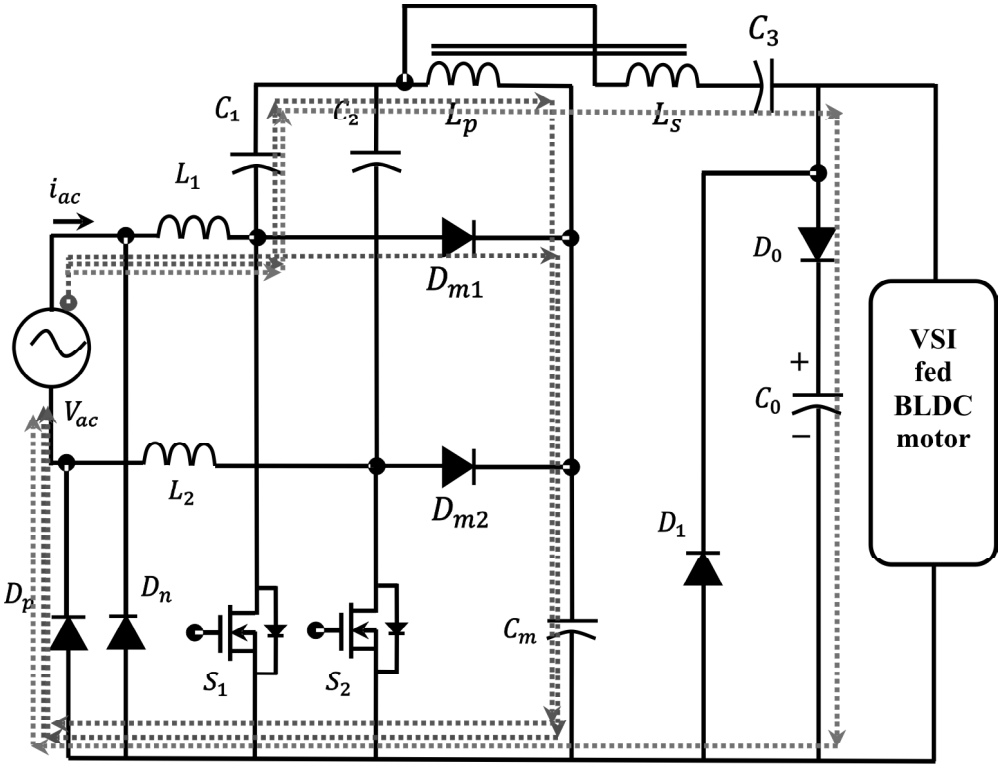



**Figure 4(b): Mode 1 Operation**

**Mode 2**

If the diodes $D_0$ and $D_{m1}$ are blocked at that instant, the voltage which is applied across the input inductor $L_1$ and Tapped Inductor (TI) are zero, thus keeping the inductors currents at a constant value as shown in the equations (1) and (2).

$$V_{L1} = V_{L2} = 0(1) \quad (1)$$

$$\Delta i_{L1} = \Delta i_{L2} = 0 \quad (2)$$

The currents passing via the input inductor and Tapped Inductor (TI) also are of the same value, thereby functioning as a freewheeling stage as illustrated in Figure 4(c).

**Control of Proposed BL TI-SEPIC DCM Converter**

**(A) Front End Converter Control**

If the converter proposed which is working in DCM indicates a third-harmonic distortion in the input current, this current distortion is actually a function of the voltage difference existing between the input and

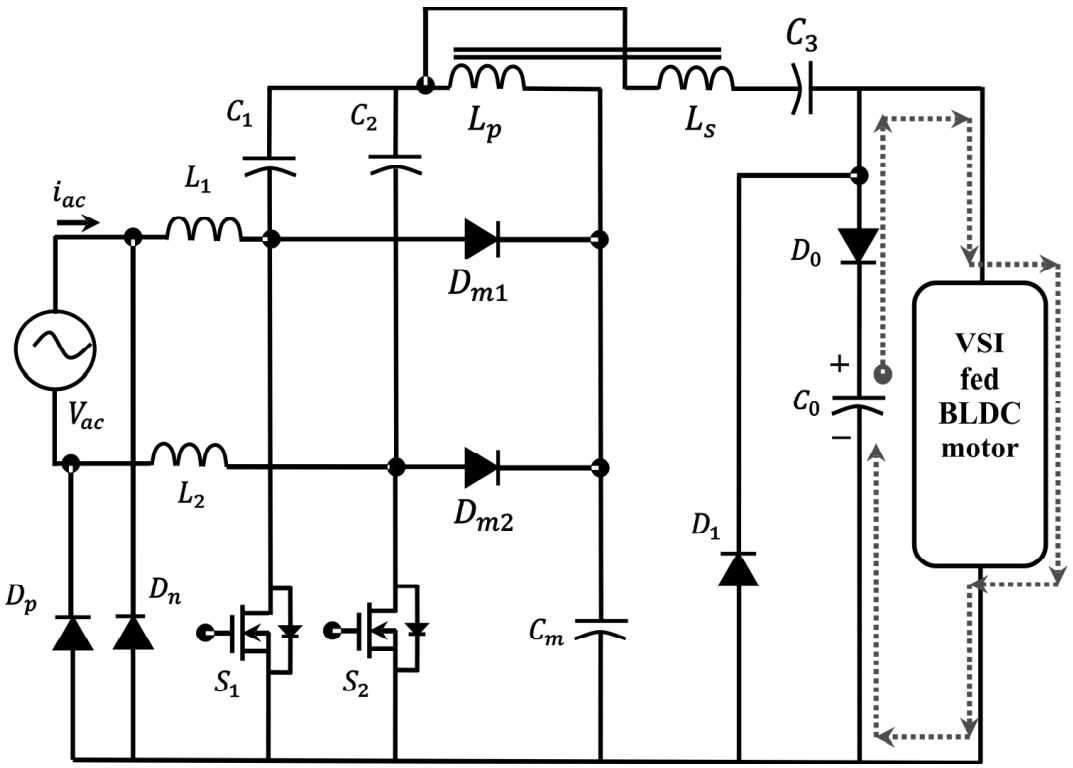



**Figure 4(c): Mode 2 Operation**

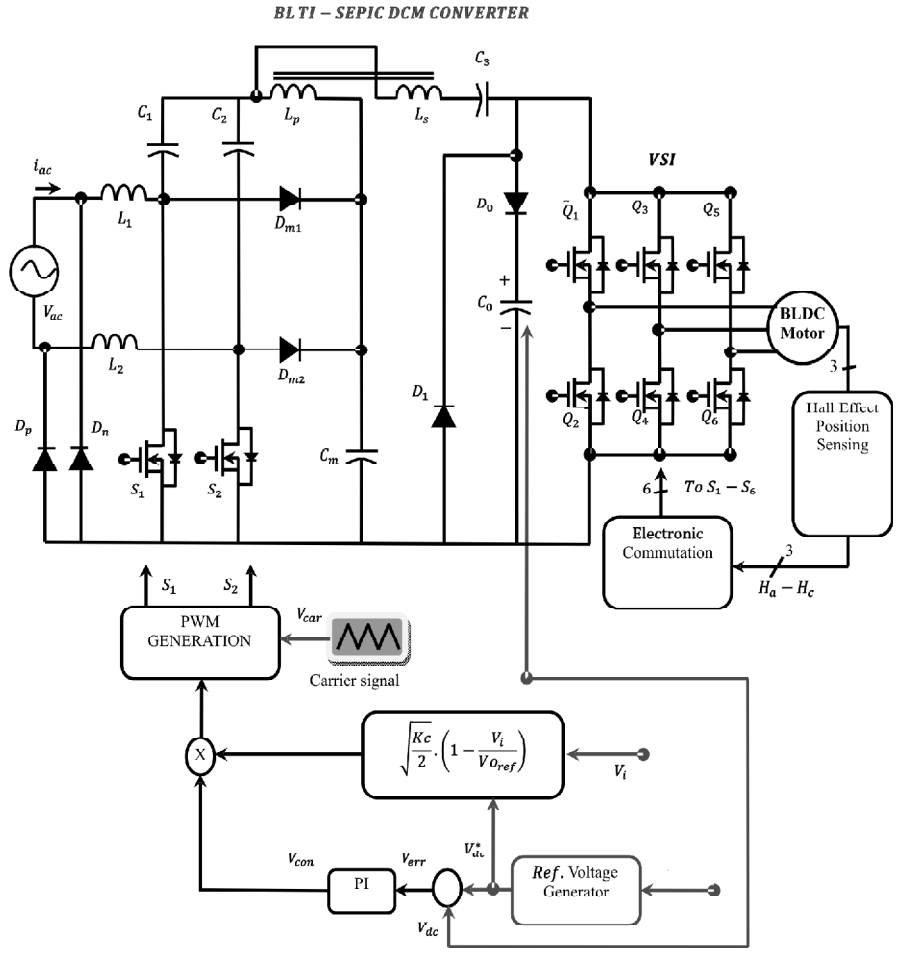



**Figure 5: Control Loop Diagram of the Proposed Converter**

the output voltage. Generally, the output voltage is raised for the purpose of reducing the third-harmonic distortion and for maintaining high power factor, though there is an increase in the semiconductors losses. The goal of minimizing the third-harmonic distortion without any increase on the output voltage has led to the introduction of an open-loop control action.

A single voltage control loop (voltage follower approach) is used for the BL-TI SEPIC converter which functions in DCM. A reference dc link voltage ($V^*_{dc}$) is produced as

$$V^*_{dc} = k_{volt} \times \omega^* \tag{3}$$

In which $k_{volt}$ and $\omega^*$ refer to the corresponding motor's voltage constant and the reference speed.

The voltage error signal ($V_{err}$) is generated by having a comparison of the reference output voltage ($V^*_{dc}$) with the output voltage sensed ($V_{dc}$) as

$$V_{err}(k) = V^*_{dc}(k) - V_{dc}(k) \tag{4}$$

Where $k$ represents the kth sampling instant. This error voltage signal ($V_{err}$) is provided as input to the voltage proportional–integral (PI) controller for the generation of a controlled output voltage ($V_{con}$) as

$$V_{con}(k) = V_{con}(k-1) + k_p\{V_{err}(k) - V_{err}(K-1)\} + k_i V_{err}(k) \tag{5}$$

Where $k_p$ and $k_i$ refer to the respective proportional and integral gains of the voltage PI controller.

$$D(\omega t) = \sqrt{\frac{K_c}{2}} . \sqrt{1 - \frac{V_{pk} . \sin(\omega t)}{V_0}} \tag{6}$$

Where, $K_c = \dfrac{8.P_0.L_{eq}.f}{V^2_{pk}}$

Only the output and input voltages are required for controlling the converter. In the same time, the rectified input voltage that is sensed ($V_i$) and the output voltage reference are applied to (4) for calculating the variation of duty-cycle for the third-harmonic reduction. The result from the PI output voltage controller and also the result from the third-harmonic reduction are multiplied thus getting the converter duty cycle and then having the PWM signal generated which regulates the main switch $S_1$ and $S_2$.

### (B) Control of BLDC Motor Drive

An electronic commutation of the BLDC motor contains the proper switching of VSI in such a manner that a symmetrical dc current is obtained from the dc link capacitor for 120° and then placed in a symmetrical

**Table 1**
**Switching States based on Hall Effect Position Signals**

| $\theta^0$ | *HALL SIGNALS* | | | *SWITCHING STATES* | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $H_a$ | $H_b$ | $H_c$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
| NA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0-60 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 60-120 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 120-180 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 180-240 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 240-300 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 300-360 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| NA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

manner at the centre of every phase. A Hall-effect position sensor is employed for sensing the rotor position with a span of 60° that is necessary for the electronic commutation of the BLDC motor.

A line current is obtained from the dc link capacitor whose magnitude is dependent on the dc link voltage that is applied, back electromotive forces, resistances, and self-inductance and mutual inductance with respect to the stator windings. Table 1 illustrates the various switching states of the VSI powering a BLDC motor on the basis of the Hall-effect position signals (*Ha – Hc*).

## 4. RESULTS AND DISCUSSION

The performance of the proposed BL TI-SEPIC- DCM converter is simulated in a MATLAB / Simulink environment using the SimPower-System Toolbox. The performance of the proposed converter is evaluated for both rated and dynamic conditions and the achieved power quality indices obtained at ac mains.

Parameters such as supply voltage ($V_s$), supply current ($i_{ac}$), Switch $S_1$ current ($i_{sw1}$) Switch $S_2$ current ($i_{sw2}$), Dc link voltage ($V_{dc}$), Speed of the BLDC motor (N), Motor Torque ($T_e$), Stator Current ($I_a$), converter output voltage, output current and output power ($V_{OUT}$), ($I_{OUT}$) and ($P_{OUT}$) respectively. Moreover, power quality indices such as power factor (PF), Total Harmonic Distortion (THD) of supply current are analysed for determining power quality at ac mains. The converter specifications used for the simulations are given in Table 2.

**Table 2**
**Specification**

| | |
|---|---|
| $V_{ac\_peak}$ | 28.28 V |
| $V_{ac\_RMS}$ | 20 V |
| $I_{ac\_peak}$ | 20 A |
| $I_{ac\text{-}RMS}$ | 14.14 A |
| *Rated Power* | 250W |
| *Rated dc link voltage* | 200 V |
| Rated torque | 1.2 Nm |
| Rated speed | 1500 Rpm |

### (A) Steady-State Performance

Figure 6(a)-(g) shows the proposed converter operates at rated Vac of (20 Vrms), rated speed of 1500 rpm and rated Torque of Te (1.2 Nm). Based on the above mentioned rated conditions, the corresponding response of the proposed converted is evaluated in the following waveforms. The stator current, Switch current and Switch current are maintained at the desired reference value as shown in Figures 6(e-g).

The dynamic performance of the proposed converter is analysed during a step change in BLDC motor speed from 1200 rpm to 1500 rpm at a specific time period, i.e. the Vac is maintained constant at 20 Vrms under varying speed, which shows a satisfactory closed-loop performance of the proposed BL TI-SEPIC-DCM converter.

Figure 7 (a) shows the supply voltage Vac maintained at 20 Vrms. The dynamic response of the proposed converter during closed loop control corresponding to the variation of the BLDC motor speed suddenly from 1200 rpm to 1500 rpm at instant of 0.5 sec as shown in Figure 7(b). Due to the speed variation from 1200 rpm to 1500 rpm, the dc link voltage suddenly responds to teh variation from 160 Vdc to 200 Vdc as shown in figure 7 (c). The reference voltage generator block functions and adapts to the speed variation. A smooth closed loop control is obtained which proves the proper functioning closed loop system. This is

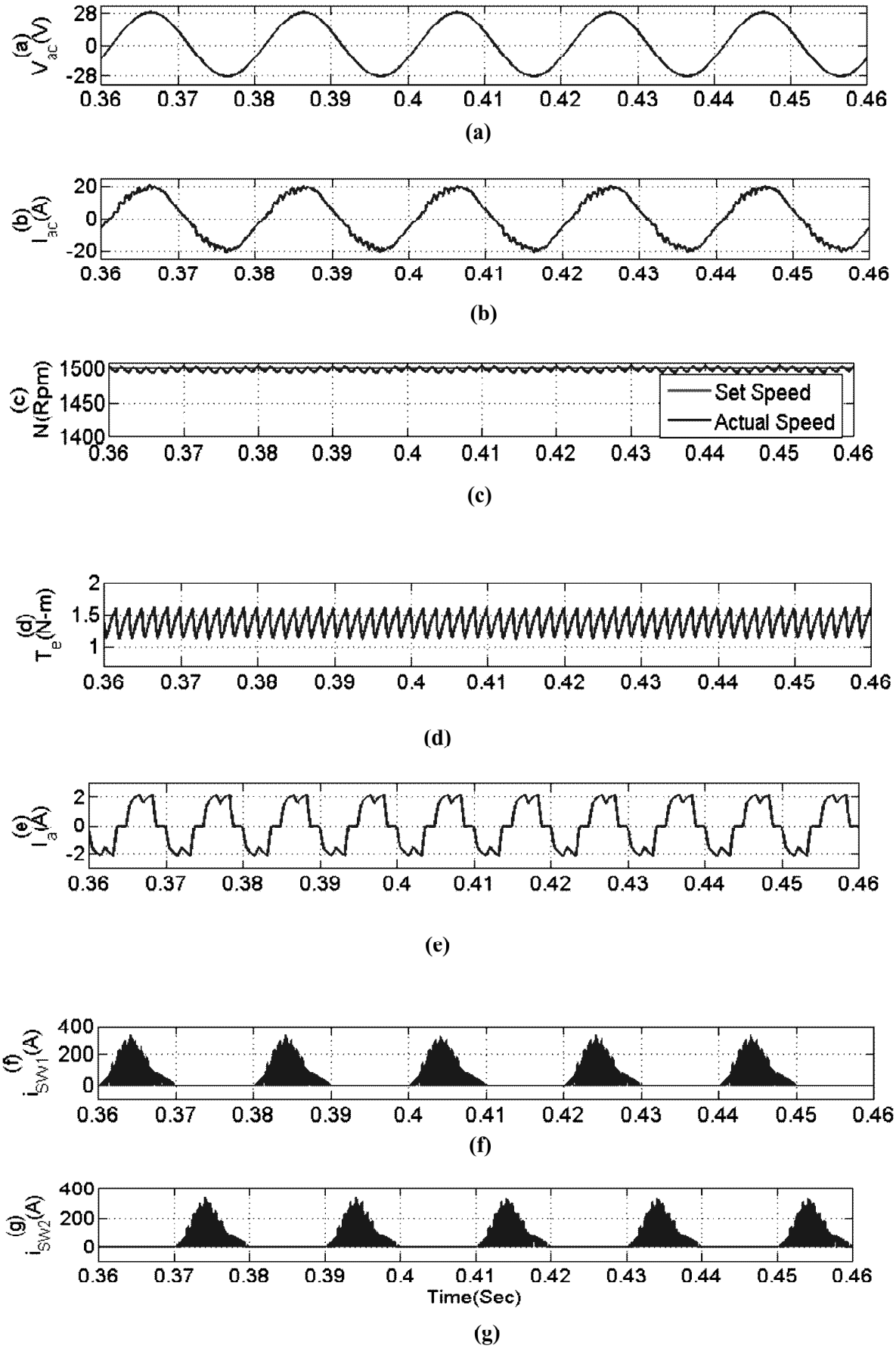



**Figure 6(a)-(g): The Proposed Converter Operates at rated Supply Voltage of (20 Vrms) Performance Evaluvation**

called as the Pulse Amplitude Modulation (PAM). Figure 7 (d) shows the corresponding stator current response of the proposed system. Figure 7 (e) shows the supply current response for the corresponding speed variation. The current amplitude increases at 0.5 sec due to the sudden change of speed as shown in figure 7 (e).

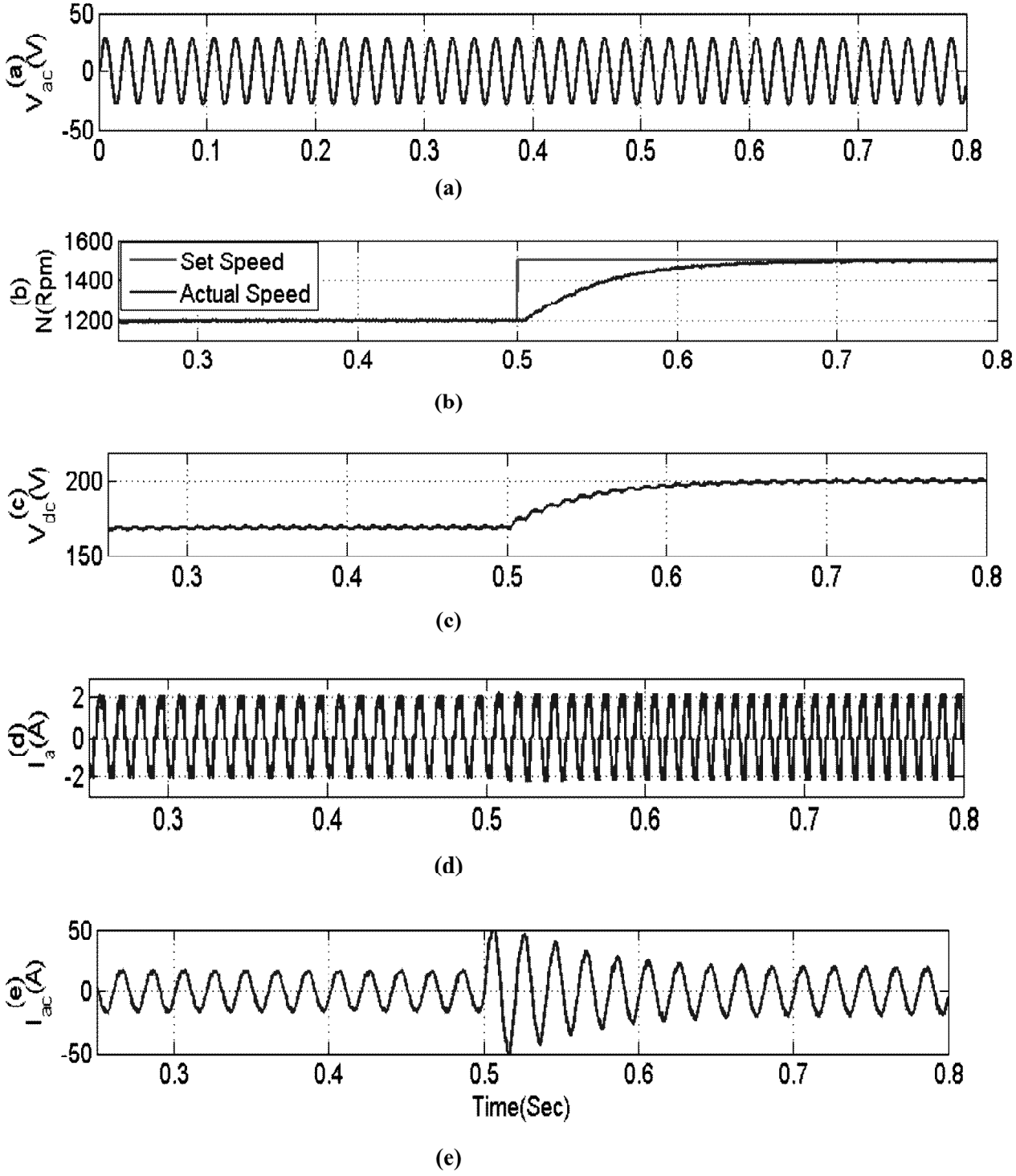



**Figure 7 (a)-(e): Dynamic Converter Response for Varied Speed Condition**

**Table 3**
**THD and PF Evaluation for the Varied Speed Conditions**

| *SPEED (N) in Rpm* | *THD%* | $I_{ac}$ *(A)* | *PF* |
|---|---|---|---|
| 1500 | 4.71 | 12.86 | 0.9982 |
| 1450 | 4.74 | 12.32 | 0.9981 |
| 1400 | 4.83 | 12.01 | 0.9979 |
| 1350 | 4.88 | 11.78 | 0.9978 |
| 1300 | 4.96 | 11.52 | 0.9976 |
| 1250 | 5.03 | 11.26 | 0.9974 |
| 1200 | 5.08 | 11.04 | 0.9972 |

Table 3 shows the performance of the proposed BL TI-SEPIC- DCM converter in terms of THD and PF for varying speed from 1200 rpm to 1500 rpm. It is clearly observed that the proposed BL TI-SEPIC DCM converter results in optimal and acceptable THD range. Moreover, the PF of the proposed converter is almost unity.

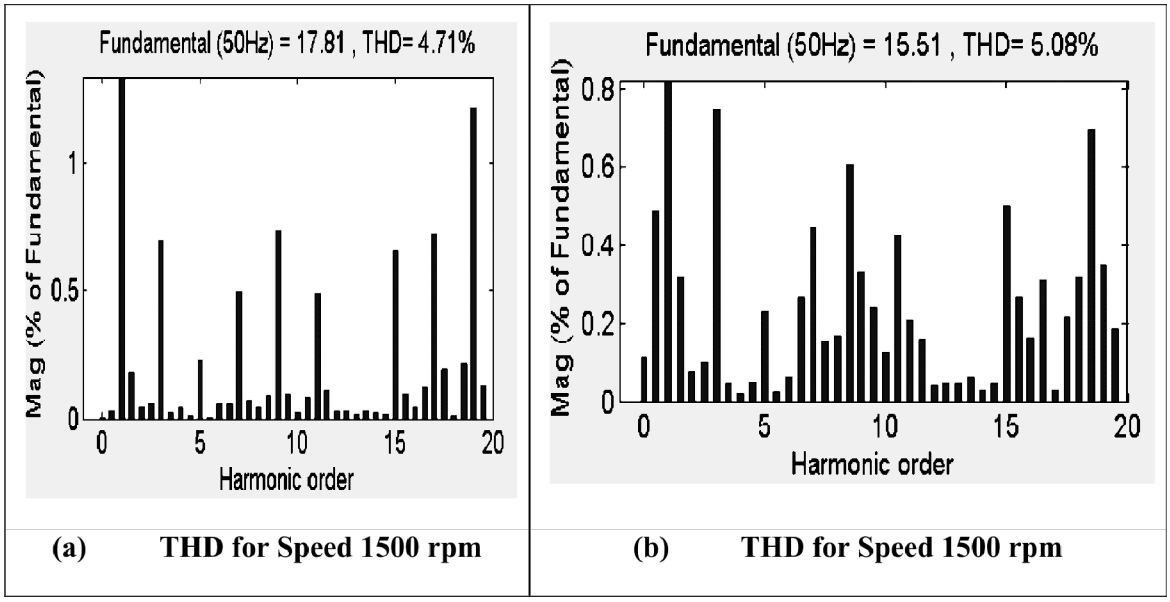



**Figure 8: THD Comparison for Dynamic Speed Variation**

## Performance Comparison

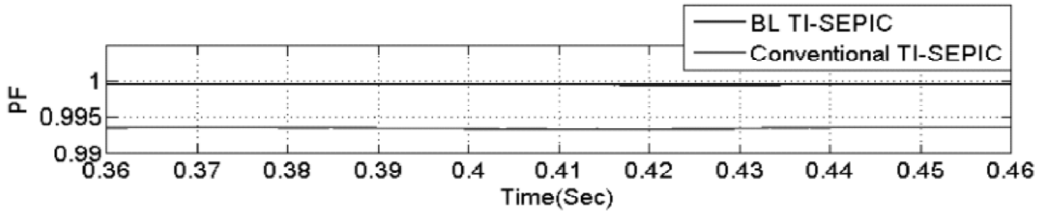



**Figure 9: PF Performance Comparison**

Figure 9 shows the PF based performance comparison between proposed BL TI SEPIC and the conventional TI SEPIC converters. It is clearly observed from the figure that the proposed BL TI SEPIC converter attains almost unity PF. This is mainly due to the fact that, the proposed system operates in BL converter type.

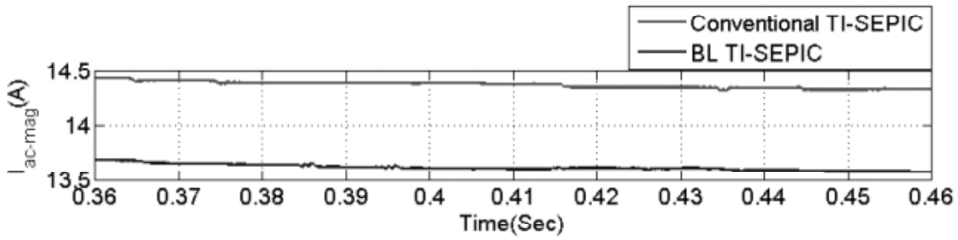



**Figure 10: Supply Current Performance Comparison**

The supply current performance comparison between proposed BL TI SEPIC and the conventional TI SEPIC converter is shown in figure 10. It is clearly observed from the figure that due to almost unity PF, the supply current consumption of the proposed BL TI SEPIC converter is minimized when compared with the conventional system. The Conventional TI SEPIC converter consumes nearly 14.3 A, where as the proposed system consumes only 13.6 A supply current.

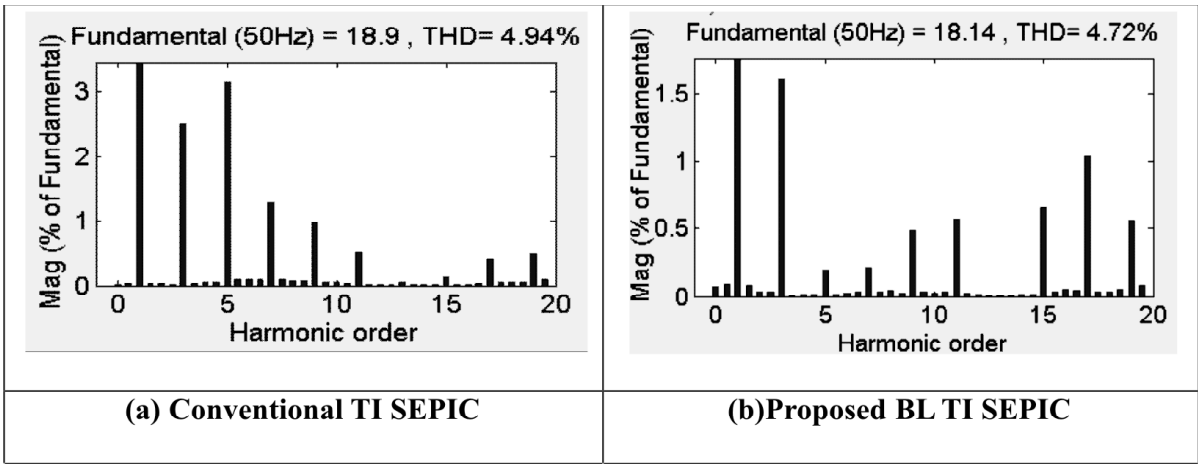



**Figure 11: THD Performance Comparison**

Figure 11 shows the THD comparison between the conventional TI SEPIC and the proposed BL TI SEPIC converter. Due to the introduction of BL PFC converter in the proposed system, the THD is minimized considerably when compared with the conventional TI SEPIC converter with bride rectifier.

## 5. CONCLUSION

This paper proposed an efficient Bridgeless PFC Converter for BLDC motor applications. The proposed BL-TI-SEPIC-DCM introduced the bridge less rectifier model for BLDC motor application. The results are simulated for dynamic varying conditions such as varying the speed of the BLDC motor. The converter results are obtained for the rated conditions. Moreover, the converter response for the varying BLDC motor speed is anlaysed. It is clear that THD results are obtained for third order harmonic reduction with minimal THD. Thus, the proposed converter results in near unity PF improvement through third order harmonic reduction for BLDC motor application. Due to the near unity PF, the supply current consumption of the proposed BL-TI-SEPIC-DCM converter is also less when compared with the conventional TI-SEPIC-DCM system.

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