I J C T A, 9(11) 2016, pp. 5427-5434

A LOW POWER LOW TRANSCONDUCTANCE OTA IN 180NM CMOS PROCESS FOR BIOMEDICAL APPLICATIONS

Rajeev Kumar[*], Sanjeev Sharma[**] and Amandeep Singh[***]

Abstract: The study presents the design and analysis of an operational transconductance amplifier with linear input range for portable electrocardiogram detection system. The proposed configuration uses the technique of current division and current cancellation with source degeneration in order to achieve linearity, small transconductance and to reduce the odd order harmonic distortion significantly. The linear transconductor is designed and simulated in 180 nm CMOS process technology on cadence virtuoso using spectre simulator with 0.85V power supply. Simulation results show the transconductance value is 2.5 nS for 100 mVpp input signal at 100 Hz. The input referred noise of the transconductor is 23 µV/sqrt(Hz) and output referred noise is 650 pV/sqrt(Hz) at 100 Hz. The power consumption is l.2 µW with biasing voltage Vb and Vfb of 0.2V and 0.18V respectively.

Key Words: Operational Transconductance Amplifier (OTA), Inversion coefficient (IC), Electrocardiogram (ECG), Electromyogram (EMG), Multiple Input Floating Gate MOS (MIFG MOS), Low Pass Filter (LPF)

1. INTRODUCTION

The world of biomedical electronics is changing rapidly with new designs and emerging new technologies. Nowadays biomedical devices are being made with more features, accuracy, preciseness, condensed in size and more comfort to use. In case of portable biomedical devices power consumption has become an important issue because of battery lifetime. The designs for biomedical portable devices must give better noise performance at low power depending upon biomedical signal characteristics.

With the rapid and numerous development of microelectronics in the recent past years, more applications require an ultra-low amplitude signal measurement module, such as implantable devices in biomedical application. Monitoring different biomedical signals of the human body is very interesting topic since it helps to know vital health information of the human body from the acquired data. These data are used by medical practitioners to diagnose diseases. Biomedical signals, such as electrocardiogram (ECG), Electromyogram (EMG), Electroencephalogram (EEG),

[*] Department of electronics and communication engineering, Lovely Professional University, Phagwara, Punjab, India
Email: email-rajeevecee2104@gmail.com

[**] Department of electronics and communication engineering, Lovely Professional University, Phagwara, Punjab, India
Email: sharmasanjeev89@yahoo.com

[***] Department of electronics and communication engineering, Lovely Professional University, Phagwara, Punjab, India
Email: amandeep.15982@lpu.co.in

are characterized by their voltage and frequency characteristics. The characteristics of these signals are presented in Table 1.

Table 1

Most Commonly used Biomedical Signals

Signal	*Frequency*	*Amplitude*
ECG	0.01 Hz – 300 Hz	50μV – 3mV
EEG	0.1 Hz – 100 Hz	1μV – 1mV
EMG	50 Hz – 3KHz	1μV – 100mV

A typical system is shown in Figure 1.1 to preprocessing the Electrocardiogram (ECG signal or cardiac signal) [3]. Since the ECG signals are weak amplitude signals, typically in the range of 50 μV–3 mV, a preamplifier is used to amplify the signal 10 to 100 times. After amplifier, a low cut-off frequency (below 250 Hz) low-pass filter (LPF) is used to eliminate the noise. This LPF is the key part in the whole ECG detection system since the accuracy of the overall system depends on the low pass filter. The major critical issues in designing such LPF are the low cut-off frequency, linearity, input referred noise, and power consumption. The need of high linearity is to achieve low THD and low input referred noise. Moreover, implementing this LPF with low frequency (f = 1/RC) on an integrated chip (IC) is tough task. In an IC, a typical capacitor value is 10 pF, and a typical resistance value is 10 K ohm is allowed to be integrated within the IC. While, to implement LPF with low frequency on an IC, a resistance with value of 100 M ohm is required, which means that a realization using active components is needed. In general, analog integrated low pass filters can be realized using different approaches such as switched capacitor (SC) and continuous time OTA-C implementations. The SC filters are limited to low frequency applications due to the sampling process and need high supply voltage for operation because of turning MOS switches on and off, and maintaining proper op-amp operation and it is having high switching noise. On the other hand, the continuous time OTA-C filters have a significant speed and low noise advantage over discrete time filters because no sampling is required. Therefore a technique is required to realize this filter using continuous time operational transconductance amplifier-C (OTA-C) filters in which the value of the transconductance (G_m) of the G_m cell and the capacitors determine the cut-off frequency. As a result, an OTA with typical value of G_m in the order of a few nA/V to 9 nA/V is needed. Obtaining OTA with low Gm leads to higher noise levels, so to achieve low Gm with low input referred noise requires an optimized design. As a result, techniques were proposed to reduce the noise such as spectral subtraction method.

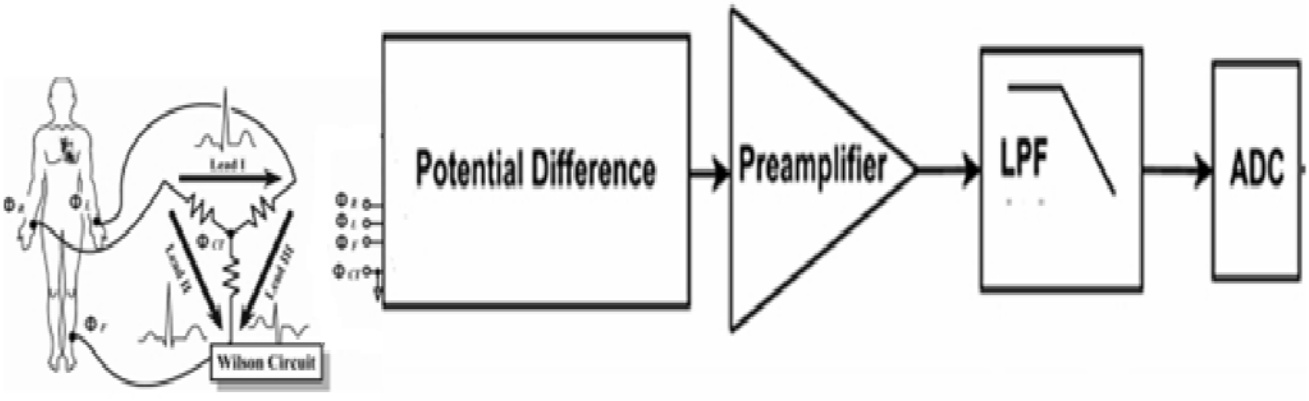

Figure 1.1 input stage of an ECG detection system

Several topologies are developed to implement low frequency low pass filter for biomedical applications. Among those g_m-C topology is most suitable one because of its leakage cancellation and better noise performance. A digitally programmable OTA using class AB buffer and linear NMOS transistor array is presented in [1]. A tunable OTA using subthreshold MIFG MOS with cubic term cancellation technique is given in [10]. The realization given in [11] is based upon obtaining a tunable OTA using four quadrant multiplier with current division technique. A comparative design approach to obtain small transconductance OTA using techniques like bulk driven OTA with current division, source degeneration with current division, MIFG MOS with current division is discussed in [12].

The primary objective of this study is to reduce the transconductance of G_m cell and to increase its linearity so that the input referred noise density is low. This paper is organized as follows: in section II OTA Design with applied techniques to reduce transconductance is discussed. Section III describes the simulation results of the proposed OTA. Finally, section IV concludes the paper.

2. CIRCUIT DESCRIPTION-

2.1 Techniques used to reduce Transconductance

There are various techniques to reduce the transconductance of OTA. A few of them are discussed in this paper.

Current Division Technique

Current division method is one of the mostly commonly used techniques to obtain the small transconductance OTA. In this method the transconductance is reduced by reducing the output current of the circuit by splitting the current unequally to flow in two transistors.

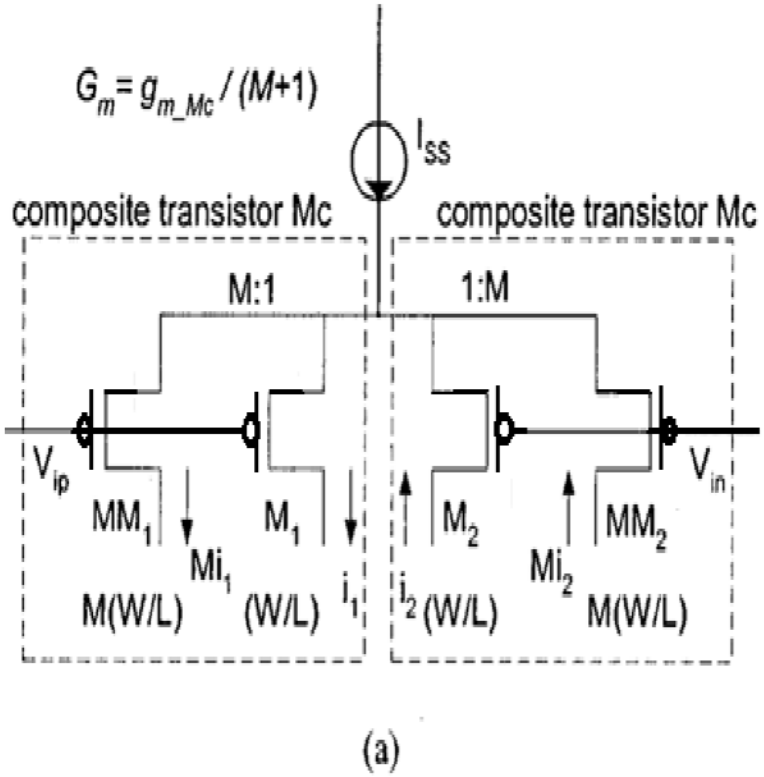

Figure 2.1 Current Division Technique

Current Cancellation Technique

Current cancellation method is another one of the mostly used technique to obtain the small transconductance OTA. In this method the transconductance is reduced by reducing the output current of the circuit by splitting the current unequally to flow in two transistors and cancelling currents using cross coupling of drain terminal of transistors.

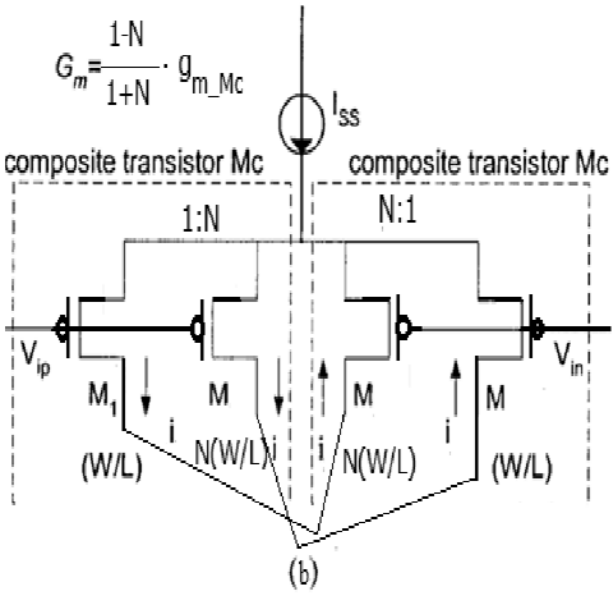

Figure 2.2 Current Cancellation Technique

Source Degeneration Technique

Source Degeneration method is another one of the mostly used technique to obtain the small transconductance OTA. . In this method the transconductance is reduced by a factor of $(1+g_m R)$. In this method we use resistor as source degenerator in the circuit and we put resistor in between current source and load. In the proposed circuit at the place of resistor a linear G_m cell is used as source degeneration element because of limitation of passive resistance value only up to hundred MΩ and more heat dissipation.

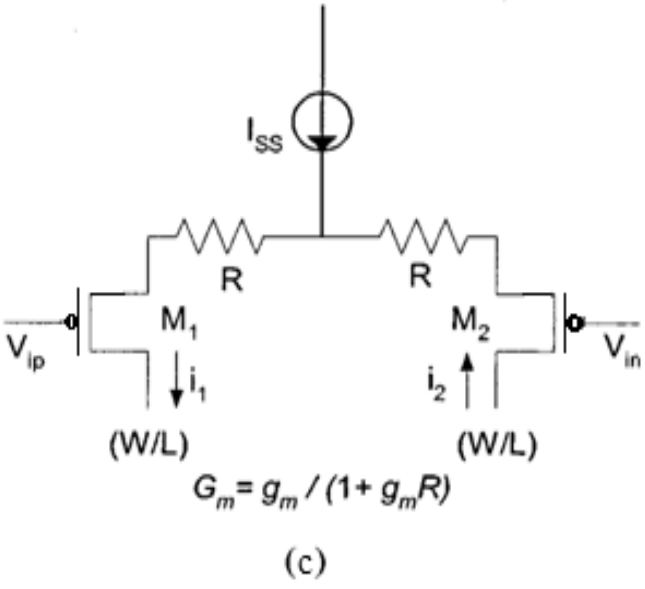

Figure 2.3 Source Degeneration Technique

2.2 Proposed OTA Structure

Figure 2.4 represents the proposed fully differential OTA which uses the concept of current division and current cancellation with extra source degeneration. The transistors M_M and M_N are current division and current cancellation transistors respectively. The transconductance ratio between transistors M_M, M_1 and M_N is M:1:N to reduce the overall transconductance. The internal G_m cell is used as source degeneration element to improve linearity as well as to reduce the overall transconductance. The internal G_m cell transistor M_B and $M'_{B'}$ are biased in moderate inversion and linear region to obtain linear transconductance. The transconductance of internal G_m cell can be approximated as [2]

$$G_{mi} = \frac{g_{mbB}}{1+\frac{r_{D+}r_L}{r_{OB}}+g_{mB}(r_D+r_L)+g_{mbB}r_L} \quad (1)$$

All NMOS transistors work in subthreshold region. PMOS transistors M_M, M_1, M_N, M_B, M_5, M_6, M_2 and M_3 work in subthreshold region, while PMOS transistors $M'_{M'}$, $M'_{1'}$, $M'_{N'}$, $M'_{B'}$ and M_4 work in linear region for low power operation. Transistor pairs M_D, M_8 and $M'_{D'}$, M_9 act as current mirror. The transconductance of internal G_m cell is kept low with acceptable linearity because the linearity of proposed OTA depends on it. For each transistor, the moderate inversion characteristic current I_S is given by [16]

$$IS=2\mu\ C_{ox}H\ V_T^2\frac{W}{L} \quad (2)$$

where μ is the carrier effective mobility in the channel, η is the subthreshold slope factor, and V_T is equal to kT/q, where q is the electron charge and T is the absolute temperature (at room temperature, V_T is about 25 mV). The inversion coefficient(I_C) is defined as the ratio of channel current I_D to the moderate inversion characteristic current I_S. If, $10 > I_C > 0.1$ the device operates in the moderate inversion region.

The overall transconductance of the complete cell can be approximated as [5]

$$Gm=\frac{1-N}{1+N+M}\cdot\frac{Gs}{1+Gs/G_{mi}} \quad (3)$$

Where G_m is overall transconductance, G_{mi} is internal G_m cell transconductance and G_S is the admittance looking into the source of input stage and equal to $(1+N+M)g_m$.

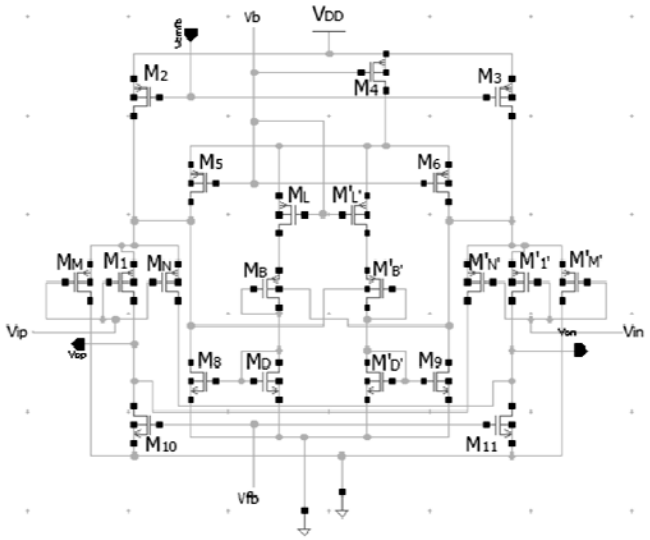

Figure 2.4 Proposed Fully Differential OTA

3. SIMULATION RESULTS

The proposed OTA is designed on Cadence Virtuoso in 180nm CMOS process. The simulator used is spectre simulator for simulations to obtain the results. Figure 3.1 shows the transconductance vs. input differential voltage plot. The nominal G_m value of our final transconductor is 2.5 nS. Figure 3.2 shows the power vs. input differential voltage plot. Figure 3.3 shows the AC voltage gain (dB) vs. frequency plot of proposed OTA. The AC voltage gain of OTA is 2 dB for 100mV at 100Hz differential input. Figure 3.4 and Figure 3.5 show output referred noise and input referred noise vs. frequency respectively. The input referred noise is 23 μV/sqrt(Hz) and output referred noise is 650 pV/sqrt(Hz) at 100 Hz.

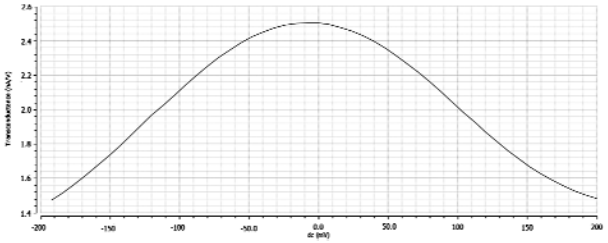

Figure 3.1 Transconductance vs. dc differential input voltage of Proposed OTA

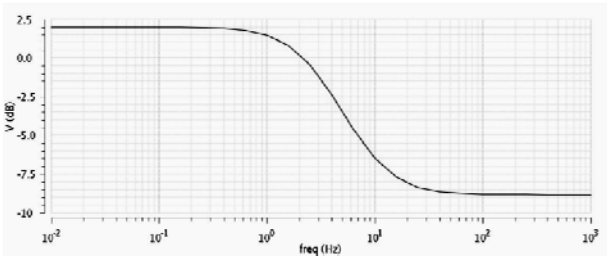

Figure 3.2 AC voltage gain of proposed OTA at 100mV and 100 Hz differential input

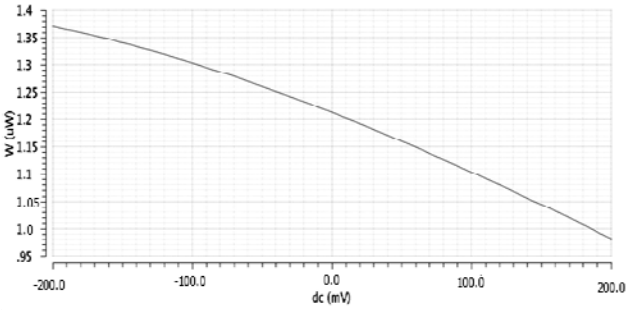

Figure 3.3 Power vs. input differential voltage of proposed OTA

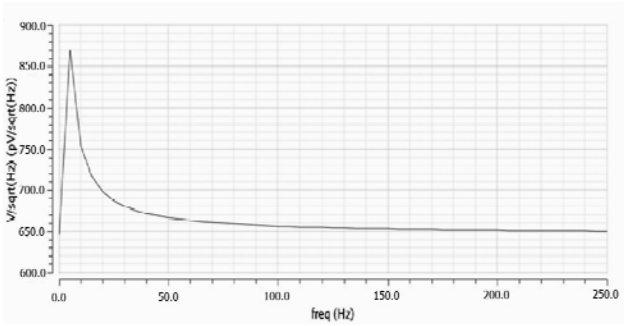

Figure 3.4 Output referred noise vs. frequency plot of proposed OTA

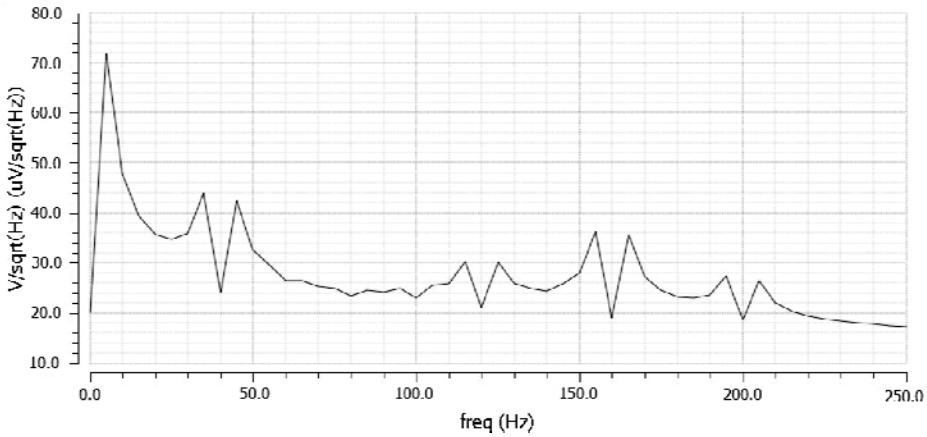

Figure 3.5 Input referred noise vs. frequency plot of proposed OTA

Table 2
Performance Parameter comparison of the Proposed OTA with previously designed OTA

	Technique	*G_m*	*Power (µW)*	*Power Supply(V)*	*CMOS process (µm)*	*Input referred Noise(µV/sqrt(Hz))*
This Work	Current division+ current cancellation+ extra source degeneration	2.5 nS	1.2	0.85	0. 18	23
Soliman A. Mahmoud [1]	Programmable OTA using class AB buffers+ linearized NMOS transistor array	3 nS - 9 nS	2.78	±0.8	0. 25	20
Aimad El Mourabit [10]	Subthreshold MIFG MOS+ cubic distortion term cancellation technique	0.4 nS - 80 nS	<1	1.5	0.8	90
Anand Veeravalli [12]	Four quadrant multiplier+ current division	50 pS - 5 nS	_	±1.5	1.2	_
Anand Veeravalli [13]	MIFG MOS+ current division	11.51 nS	1.62	2.7	1.2	26.03
	Bulk driven MOS+ current division	11.24 nS	4.05	2.7	1.2	70.3
	Source degeneration+ current division	11.55 nS	1.35	2.7	1.2	17.29

4. CONCLUSION

The paper presents a low power low voltage linear small transconductance design in 180nm CMOS process using current division and current cancellation technique with extra source degeneration technique. The internal G_m cell is used as linear source degeneration resistor which helps to decrease the transconductance. A small overview of applied techniques on the circuit to reduce the transconductance is presented. Comparison is also done with previous existing work on the presented topic. The simulation result shows improved transconductance at low power with acceptable input referred noise 23 µV/sqrt(Hz) and output referred noise 650 pV/sqrt(Hz) for at 100mV input @ 100 Hz, which is more adequate in designing low pass filter using small transconductance OTA for cardiac signal detection in biomedical application.

References

[1] Soliman A. Mahmoud, Ahmed Bamakhramah, and Saeed A. Al-Tunaiji, "Low-Noise Low-Pass Filter for ECG Portable Detection Systems with Digitally Programmable Range" Circuits Syst Signal Process, pp-2029–2045, vol.-32, 13 Feb 2013.

[2] Yen-Ting Liu, Donald Y.C. Lie, Weibo Hu and Tam Nguyen, "An Ultralow-Power CMOS Transconductor Design with Wide Input Linear Range for Biomedical Applications" IEEE *Circuits and Systems, pp-20*11-2014, Dec 2012.

[3] A. Bharadwaj, U. Kamath, Accurate ECG signal processing. Technical report. Cypress Semiconductor Corporation (2011)

[4] Esther Rodriguez Villegas, Alexander J. Casson and Phil Corbishley, "A Subhertz Nanopower Low-Pass Filter, " IEEE *Circuits And Systems,* vol .58, no.6, June 2011.

[5] Shuenn-Yuh Lee, Chih-Jen Cheng "Systematic Design and Modeling of a OTA-C Filter for Portable ECG Detection, " IEEE trans., vol .3, no.1, Feb 2009.

[6] Andras Timar and Marta Rencz,"Design issues of a low frequency low-pass filter for medical applications using CMOS technology," IEEE, *Design and Diagnostics of Electronic Circuits and Systems*, pp.1-4, April 2007.

[7] Chun-Lung Hsu, Mean-Hom Ho, Yu-Kuan Wu and Ting-Hsuan Chen, "Design of Low-Frequency Low-Pass Filters for Biomedical Applications," IEEE, *Circuits and Systems*, pp. 690-695 ,Dec 2006.

[8] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, "Nanowatt, sub-nS OTAs, with sub-10-mV input offset, using series-parallel current mirrors," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2009–2018, Sep. 2006.

[9] Gozzini. F., Ferrari.G., and Sampietro. M., "Linear transconductor with rail-to-rail input swing for very large time constant applications" Electronic Letters,vol. 42 no. 19, 2006.

[10] A. El Mourabit, G.-N. Lu, and P. Pittet, "Wide-linear-range subthreshold OTA for low-power, low-voltage, and low-frequency Applications," IEEE Trans., pp. 1481–1488, vol.-52, Aug. 2005.

[11] A. El Mourabit, G.-N. Lu, and P. Pittet, "A low-frequency, sub 1.5-V micropower Gm-C filter based on subthreshold MIFG MOS transistors," in Proc. IEEE ESSCIRC, Grenoble, France, , pp. 331–334. Sep. 2005.

[12] A. Veeravalli, E. Sánchez-Sinencio, and J. Silva-Martínez, "A CMOS transconductance amplifier architecture with wide tuning range for low frequency applications," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 776–781, Jun. 2002.

[13] A. Veeravalli, E. Sanchez-Sinencio, and J. Silva-Martinez, "Transconductance amplifier structures with very small transconductances: A comparative design approach," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 770–775, Jun. 2002.

[14] S-S Bustos, J S Martinez , F Maloberti and E Sanchez-Sinencio, "A 60-dB Dynamic-Range CMOS Sixth-Order 2.4-Hz Low-Pass Filter for Medical Applications", IEEE Transactions On *Circuits And Systems,* vol. 47, pp. 1391-1398, no.12, December 2000.

[15] E.S.Sinencio and J.S.Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial", IEEE *Proc.-Circuits Devices System*, vol. 147, no. 1, February 2000.

[16] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York: McGraw-Hill, 1998.

[17] Prasant K. Mahapatra, Manjeet Singh , Neelesh Kumar , "Realization of active filters using operational transconductance amplifier (OTA)", *Journal of the Instrument Society of India*, pp 1-9 1995.

[18] Randall L. Geiger, Edgar Sánchez-Sinencio "Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial," IEEE *Circuits and Devices Magazine*, vol. 1, pp.20-32, March 1985.