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Modified Hybrid PWM Technique For Neutral Point Stabilization of Five Level Diode Clamped Inverter

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ABSTRACT

An intrinsic problem with diode clamped multi-level inverter is fluctuations or simply called unbalance of voltage at neutral point. This voltage fluctuations can cause uneven voltage sharing among the switching devices. Sometimes may cause failure and increases harmonic component in the output waveform. This problem is normally mitigated by closed loop control of neutral point voltage. There are many mitigation methods well established in literature to balance the neutral point voltage using conventional SPWM and space vector PWM techniques. But these techniques has drawbacks like low frequency ripples at the neutral point and high switching losses. So This project deals with the new control technique for balancing the neutral point voltage i.e. With the combination of both SPWM and SVPWM techniques to the fullest for achieving efficient voltage balance at the neutral point by providing quality output for 5 level diode-clamped multi level inverter for any type of load. MATLAB-SIMULINK will be used to develop this technique.

Keywords: Diode clamped multi level inverter (dcmli), sinusoidal pulse width modulation (spwm), space vector pulse width modulation(svpwm), near vector(NV)

1. INTRODUCTION

For the most part, diode-clamped multi level inverters (DCMLI) are using for the high power/ voltage applications. As compared with a two-level inverter, it has the accompanying preferences: 1) gives higher quality output; 2) it works at higher ac-voltage levels and minimize or even dispose the need of interface transformer; 3) decrease switching losses. In spite of its merits for high-voltage applications, [1] it has a drawback that neutral point voltage unbalance at its dc-side capacitors. The voltage-drift occurrence will decays the output waveform, ineffective operation DCMLI and also cause failure of the switches in DCMLI. Thus, there is requirement of equal voltage division between dc capacitors. The occurrence of voltage-drift across dc capacitors of a three level DCMLI has been greatly researched and categorized as SPWM,SHE and SVPWM. In all these modulating techniques linear controlling, direct torque controlling and predictive controlled methods were used. Recently some hybrid techniques were developed.

These hybrid techniques uses the combination of near vector and non-near vector techniques, which is going to nullify the drawback of both nearest vector techniques and non near-vector techniques. NV techniques eliminate neutral point voltage ripple for a certain range of load power angle $\varnothing$ and converter modulation index m. Non-near vector strategies can eliminate neutral point voltage ripple but at the cost of high switching steps it causes high switching frequency when compared to nearest vector strategies. So for the effective control the neutral point unbalance and to decreases the switching losses of DCMLI, all this strategies were investigated extensively.

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Despite a wide range of applications that have been reported in the technical literature for a five-level diode clamped multi level inverter [5], but its capacitor-voltage-unbalance phenomenon has not been comprehensively analyzed. For five level DCI, it include more number of components and complexity of control circuit [6], [7] increases. A detailed study of five-level DCI will be projected in this project and focused on different approach called modified hybrid PWM technique, in order to balance the voltage unbalance phenomenon of five level DCI.

To overcome the neutral point voltage drift phenomena, this proposed technique gives efficient result at different power factors compared to normal sinusoidal pulse width modulation.

The rest of paper follows as: Section 2, Deals with literature review. Section 3 demonstrates the proposed system model and proposed techniques. Section 4 Discuses experimental results. Section 5 presents the conclusions and future enhancement.

2. LITERATURE REVIEW

Selective harmonic elimination technique [1] was used and it is able to eliminate lower order harmonics which is below thirteenth order at 25 hz of load frequency. But practically it is complex to solve equations. Carrier based pulse width modulation technique is very popular. It is developed by comparing reference wave with 4 carrier waves but this technique is good at low modulation index. Space vector modulation technique has redundant states which is used to balance the neutral point voltage [2][3]. But the modulation technique is quite complex and also switching losses increases. To reduce the complexity of space vector modulation some more work was done in papers [4][5][6].

3. 5 LEVEL DIODE CLAMPED INVERTER

Figure 1 shows that the simplified circuit diagram of a five level diode clamped inverter. A diode clamped multi level inverter consist of (m-1) capacitors on the dc side and 2(m-1)switches for each leg. The table 1 describes the voltage level and their respective switching states. State condition 1 means the switch is on

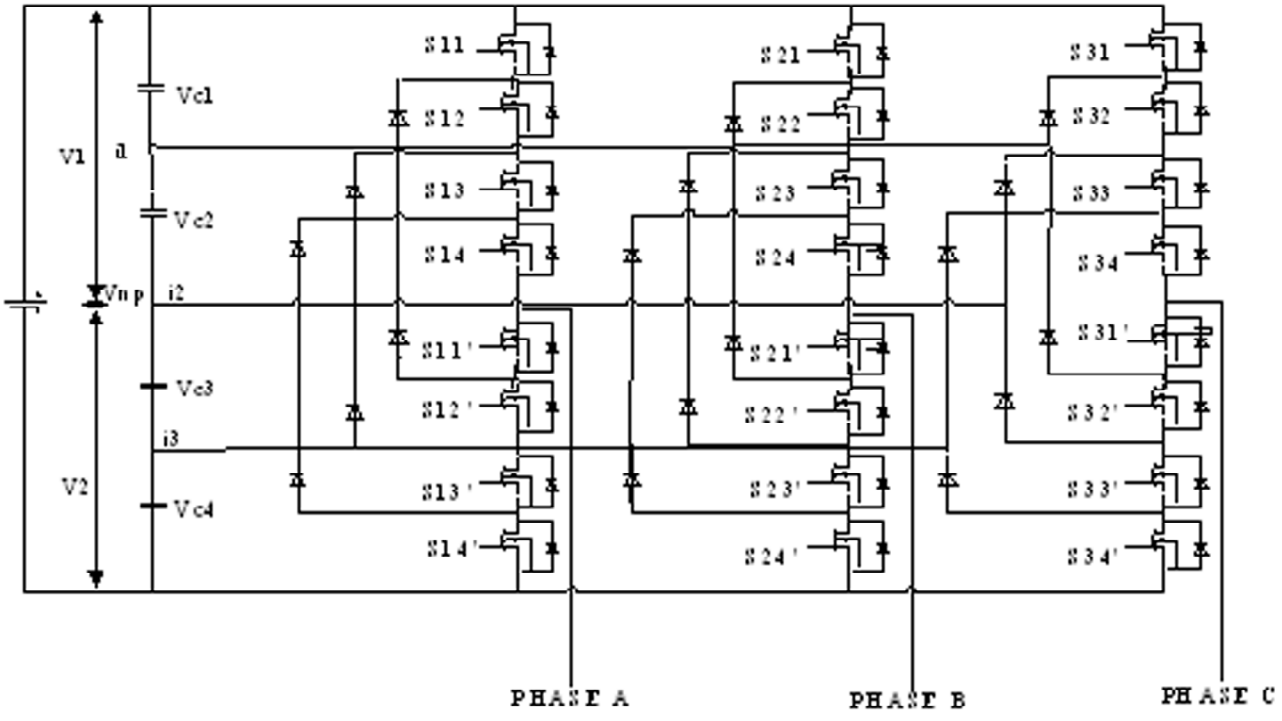

Figure1: 5 level diode clamped inverter

Table 1
5 level switching states, Switches(S), Mode(M)

S / M	S11	S12	S13	S14	S11'	S12'	S13'	S14'	Voltage magnitude
4	1	1	1	1	0	0	0	0	$+V_{dc}/2$
3	0	1	1	*1*	1	0	0	0	$+V_{dc}/4$
2	0	0	1	1	1	1	0	0	0
1	0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	0	1	1	1	1	$-V_{dc}/2$

and 0 means the switch is off. It should be noticed that each switch is turned on only once per cycle and there are four complementary switch pairs in each phase.

These pairs of one leg of inverter are(s11, s11'), (s12, s12'), (s13, s13'), (s14, s14').If one of the complementary switch pair is on and the other of same pair must be off. The operating states of the switches and voltage magnitudes of the diode clamped inverter is shown in Table 1. Switching state “4” denotes that the upper four switches in leg *A* are on and the inverter terminal voltagev_{Anp}, which is the voltage at terminal *A* with respect to the neutral point *np*, is $+V_{dc}/2$, whereas “3” indicates that upper four switches but not first switch conduct, leading to $v_{Anp}=+V_{dc}/4$. Switching state “2” signifies that the inner four switches are on and v_{AZ} is clamped to zero through the clamping diodes. Depending on the direction of load Switching state “1” signifies that the inner four switches but not last switch is on and $v_{Anp}=-V_{dc}/4$ and Switching state “0” signifies that the inner four switches are on and $v_{Anp}=-V_{dc}/2$.

3.1. 5-Level Space Vector

There are 125 switching states for the 5 level SVPWM as shown in Figure 2, for the 5 level there are more redundancy states which is defining as more switching states gives the same output voltage, and these

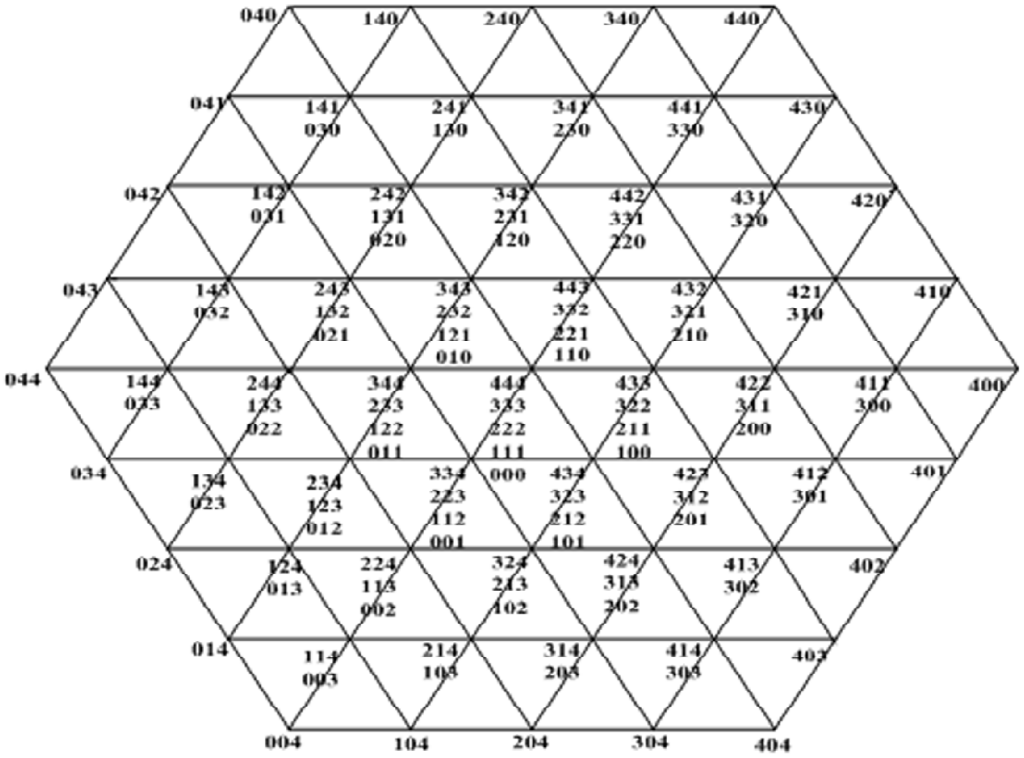

Figure 2: 5 level space vector diagram

redundant states are using for stabilization of the neutral point voltage unbalance. Inner hexagon states named as small vectors which is shown below figure has four redundancy states for each sector.

3.2. Proposed Technique

Combination of sinusoidal pulse width modulation and space vector modulation will be used, specifically SPWM will be used to operate the diode camped converter and SVPWM will be used at zero crossings of every phase voltage waves to stabilize the neutral point voltage at the same time to effect less distortion on output as shown in Figure 3.

Considering the direction of phase currents how these states effecting the neutral point and also considering less switching losses in view, two switching states per sector is taken into operation those which are effecting neutral point by phase current per sector is shown in Table 2.

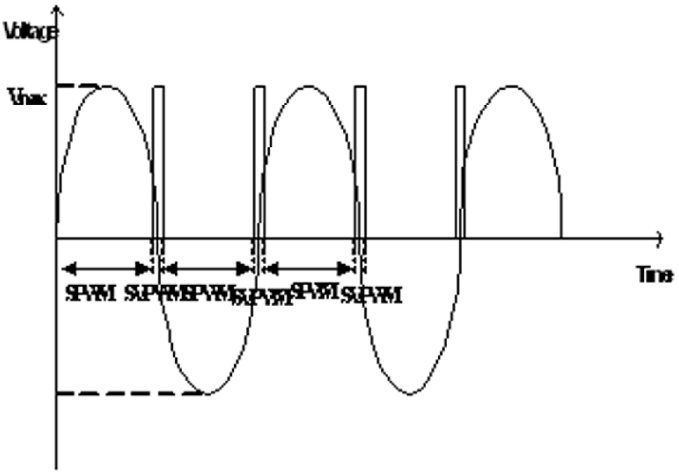

Figure3: Proposed technique

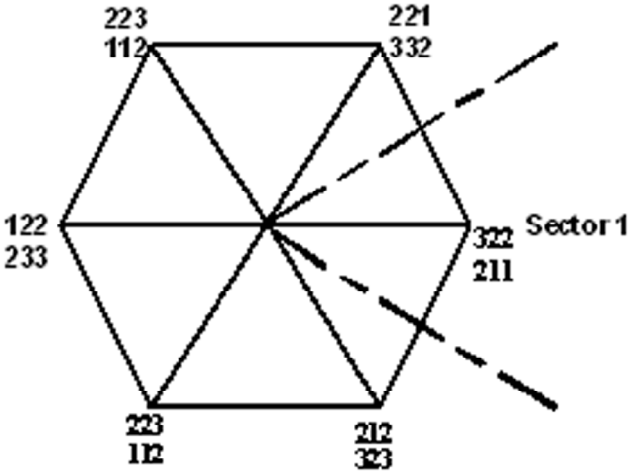

Figure 4: Inner hexagon of 5 level space vector

Table 2
Voltage, Current and Power states being considered

sector	V_1-V_2	*Neutral point current* (i_{np})	*Power*(V_1-V_2)* (i_{np})
1	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve
2	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve
3	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve
4	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve
5	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve
6	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve	+ve or –ve+ve or -ve

3.3. Algorithm

1. When the phase voltage wave crosses zero the space vector technique gets activated
2. First the sector is determined in which the reference voltage is.
3. The difference of the capacitor voltages used in the inverter and the neutral current measurements are taken.
4. Then the neutral power is calculated.
5. The direction of the neutral power is taken into consideration.

6. Then according to the direction of the neutral power direction, the vectors are taken into consideration as shown in the table 2.

3.4. Block Diagram

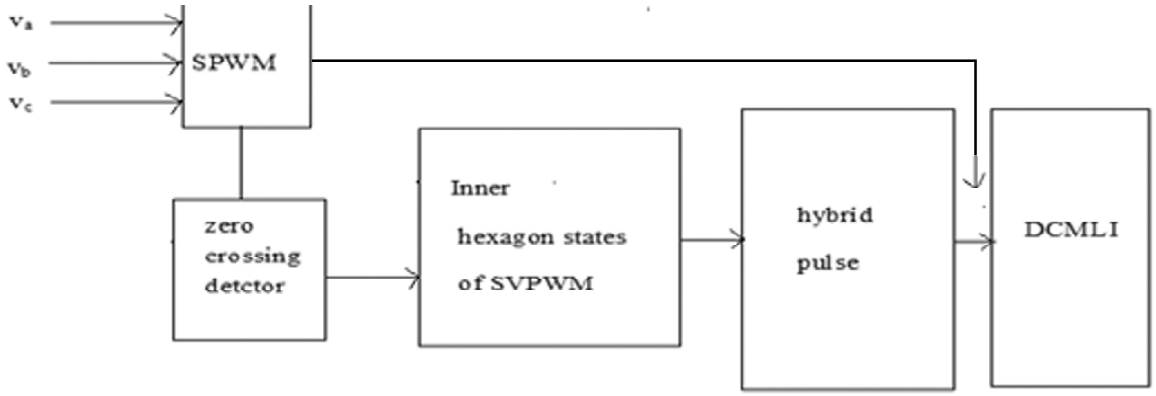

Figure 5:Implementation of proposed technique

4. RESULTANDDISCUSSION

4.1. ExperimentalSetup

The proposed technique has been implemented using MATLAB/Simulink.Heresimulink models of conventional and proposed technique were developed using power system tool box and commonly used tool boxes.

4.2. Result

In this paper the neutral point voltage oscillations of five level inverter controlled by conventional sinusoidal PWM technique and the proposed modified hybrid PWM technique are compared for different power

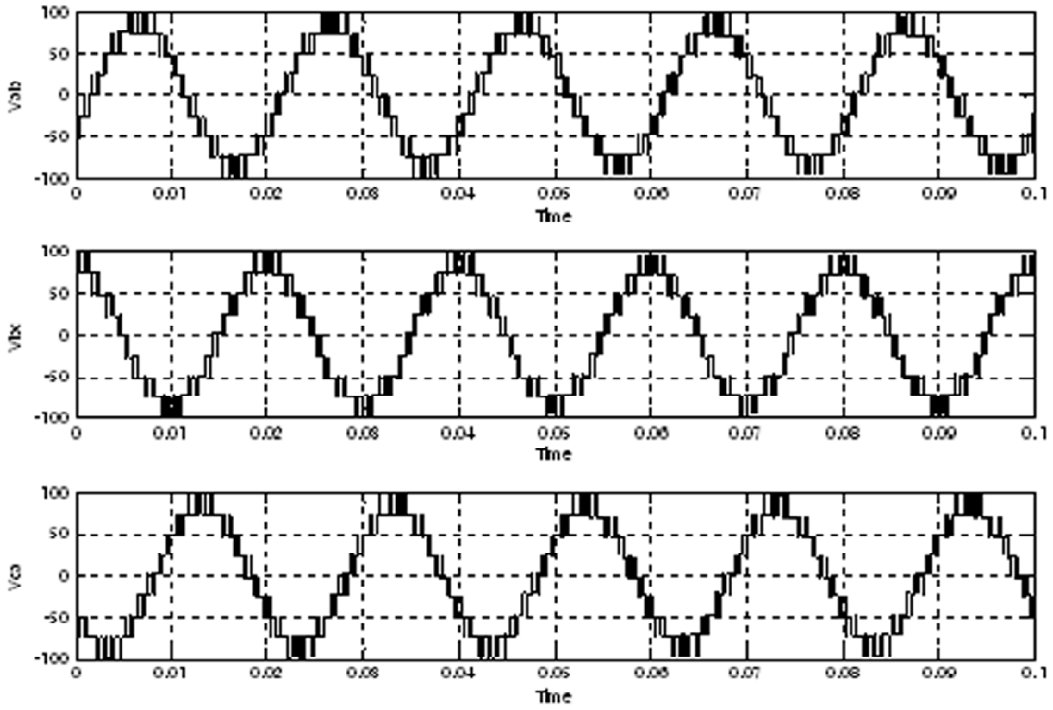

Figure 6: Output voltage of 5 level diode clamped inverter with proposed technique

factors.The supply voltage is considered to be 1000V and the capacitor values taken are 4mf. Figure 6 shows the output voltage of the five level inverter for the proposed technique, It can be observed that multilevels are equally spaced which demonstrates the equality of capacitor voltages.

The figures 7-10 witness the reduction in the neutral point voltage for the proposed technique compared with the conventional sinePWM technique with a magnitude of about 50.8V It can be observed from Table 3.

When p.f. = 0.2

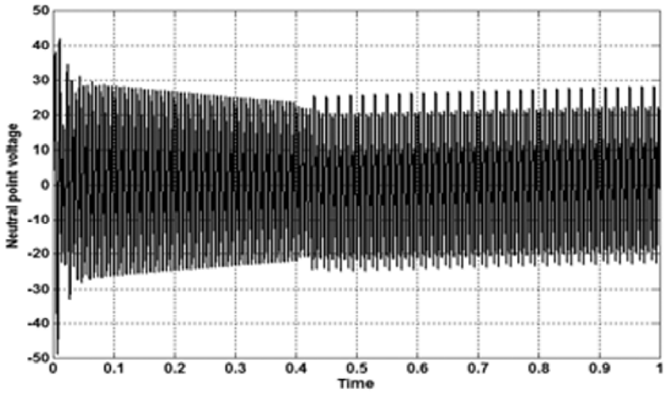

Figure 7: Neutral point voltage of SPWM when power factor equal to 0.2

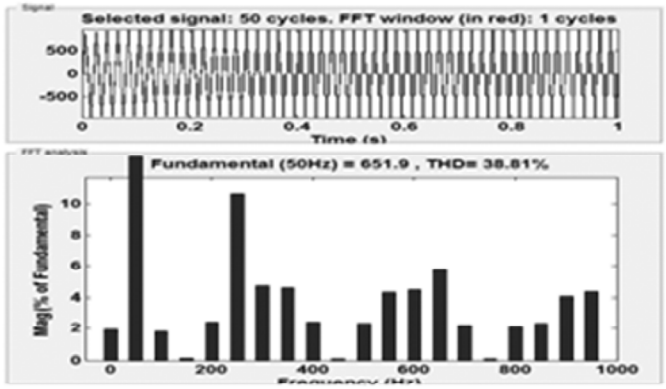

Figure 8: FFT analysis of SPWM when power factor equal to 0.2

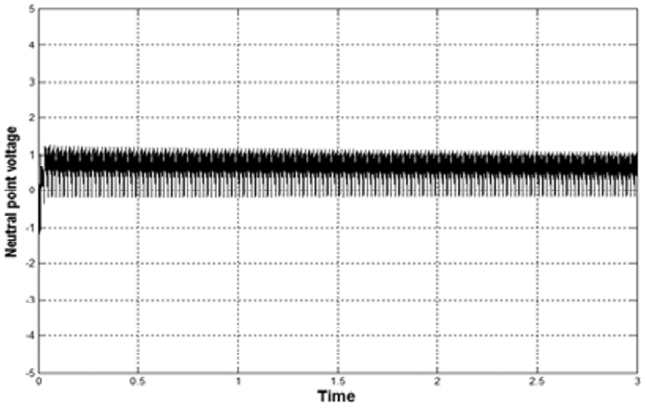

Figure 9: Neutral point voltage when power factor equal to 0.2

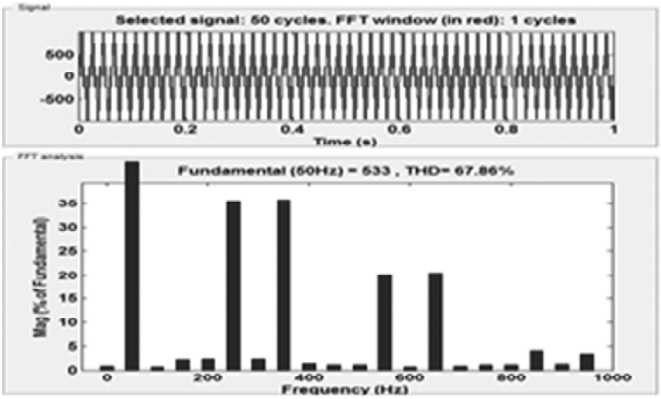

Figure 10: FFT analysis when power factor equal to 0.2

When p.f = 0.8

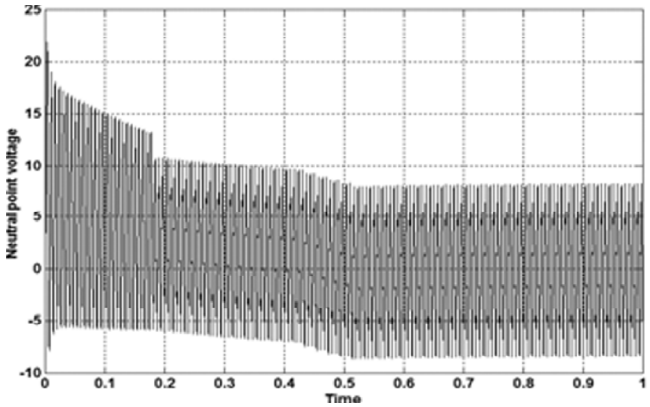

Figure 11: Neutral point voltage of SPWM when power factor equal to 0.8

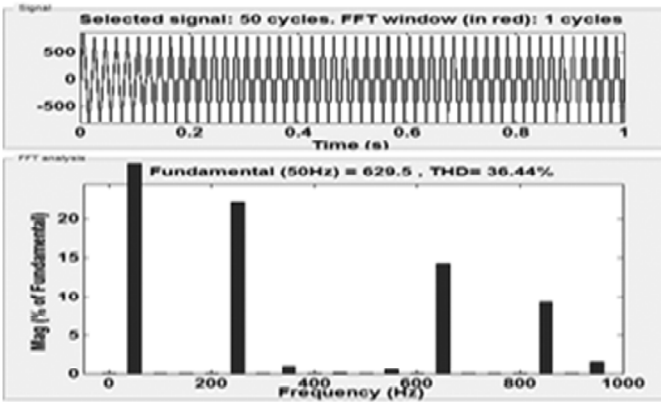

Figure 12: FFT analysis of SPWM when power factor equal to 0.8

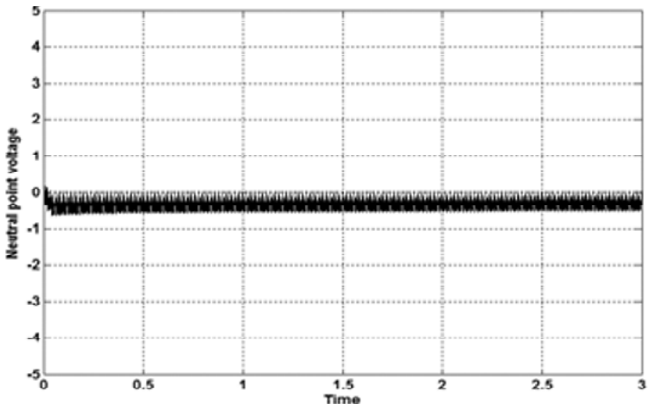

Figure 13: Neutral point voltage when power factor equal to 0.8.

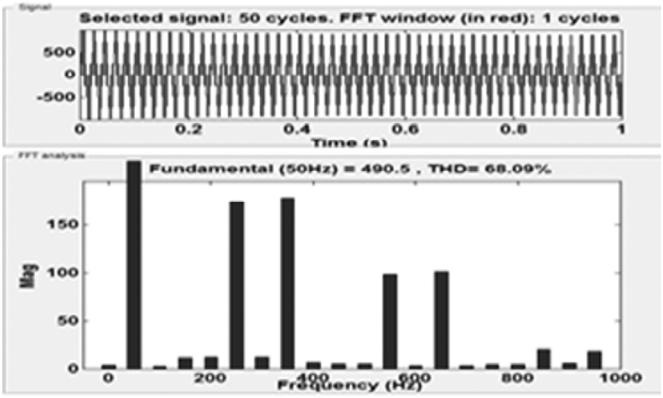

Figure 14: FFT analysis when power factor equal to 0.8

The figures 11-14 witness the reduction in the neutral point voltage for the proposed technique compared with the conventional sinePWM technique with a magnitude of about2.2V. It can be observed from Table 3.

When p.f. = 1

The figures 11-14 witness the reduction in the neutral point voltage for the proposed technique compared with the conventional sinePWM technique with a magnitude of about 16V. It can be observed from Table 3.

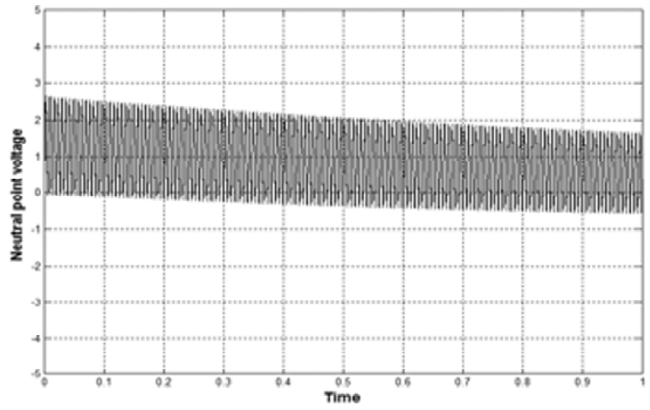

Figure 15: Neutral point voltage of SPWM when power factor equal to 1.

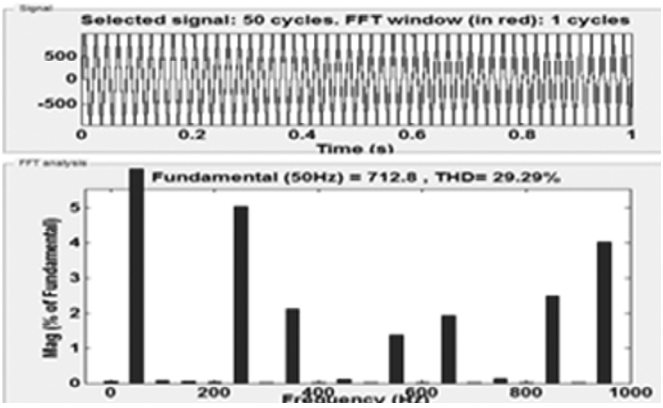

Figure 16: FFT analysis of SPWM when power factor equal to 1

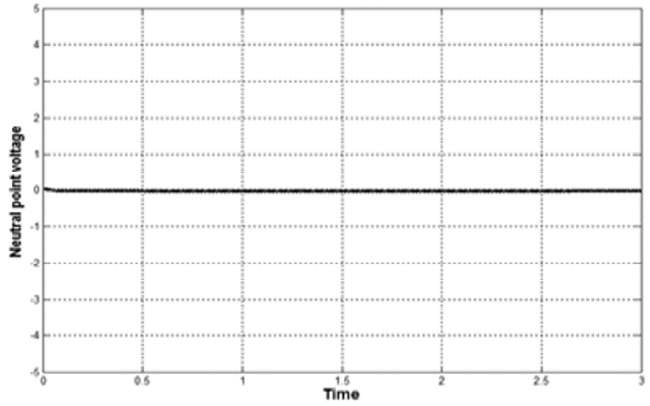

Figure 17: Neutral point voltage, when power factor equal to 1.

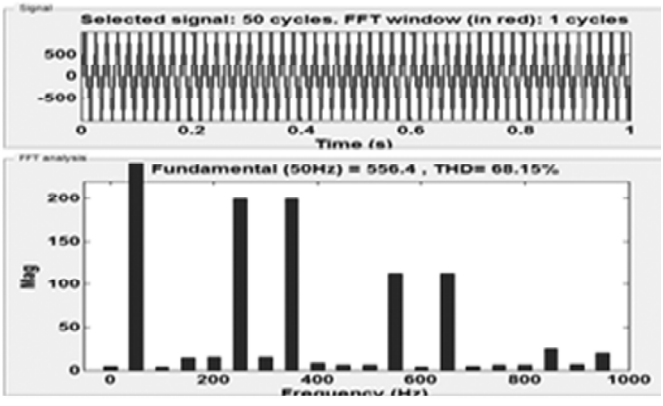

Figure 18: FFT analysis, when power factor equal to 1

The Table 3 shows the results obtained for p.f. = 0.2, 0.4, 0.6, 0.8 and 1. But the Figures are presented for p.f. = 0.2, 0.8 and 1.

Table 3
Variation of neutral point voltage and total harmonic distortion,Total harmonic distortion (THD)

S.NO	*Powerfactor*	*•/• THD in SPWM*	*•/• THD inhybrid*	*Neutral Point Voltage in SPWM*	*Neutral Point Voltage in hybrid*
1	0.2	38.81	67.38	52	1.2
2	0.4	38.42	68.11	45	1 to -1
3	0.6	38.8	68.03	35	-1
4	0.8	36.44	68.09	16	-0.5
5	1	29.29	68.12	2.5	0.3

5. CONCLUSION

The proposed technique is verified at different load power factors, it is observed that neutral point voltage balanced effectively but the total harmonic distortion increased. This technique makes use of redundant states in five level inverter thereby it simple mentation is quite easy when compared to other techniques.

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