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# Power Quality Enhancement Using Interline Dynamic Voltage Restorer with a Fuzzy Logic Controller

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**ABSTRACT**

Custom power devices like DVR, DSTATCOM, UPQC are used for mitigating power quality problems like voltage sag , voltage swell, interruptions etc. at the distribution side.DVR has been used in these system to performance its fast dynamic response and provide low harmonic of the voltage restorer.The Dynamic Voltage Restorer (DVR) is an effective series compensation device due to its fast response. However the amount of energy it requires as input for mitigating a power quality problem depends upon the problem duration. For longer durations greater energy is required. This limits the application of DVR. To overcome this situation an Interline Dynamic Voltage Restorer(IDVR)that contains two or more DVR's of different feeders is proposed. This paper presents a simulation model of the IDVR which utilizes a voltage fed switched coupled inductor inverter (VFSCII) instead of a conventional VSI. The phase advance angle of the load during fault condition is taken for generating the reference voltage. This voltage is compared with the load voltage using a fuzzy logic controller to generate pulses required for triggering the VFSCII.

***Keywords:*** Interline Dynamic Voltage Restorer, Voltage Fed-Switched Coupled Inductor Inverter, Fuzzy logic, Power devices

## 1. INTRODUCTION

Power quality is of important concern at both the transmission side and distribution side. To maintain the power quality,flexible ac transmission system (FACTS) devices are used at the transmission side. But the root cause of the power quality problems like voltage sag, voltage swell, interruptions etc. is due to the usage of ac drives, welding machines, electronic devices at etc. at the distribution side. Therefore installing devices that could maintain the quality of power at the distribution side itself would be more satisfactory[6].

Custom power devices are the modified form of FACTS devices that are used for maintain power quality at distribution side. DVR, DSTATCOM, UPQC are some of the commonly used custom power devices. Dynamic Voltage Regulator (DVR) is proven to the most efficient series compensation device because of its fast response nature[9]. It utilizes the energy from external sources like batteries or from DC link capacitors and converts into a three phase voltage which is injected in series to the distribution feeder lines [1],[6]. The mitigation percentage mainly depends upon the amount of energy available at its input. To mitigate a longer duration fault, more amount of energy is required. This limits the application of DVR. To overcome this limitation an interline dynamic voltage regulator (IDVR) is proposed. An IDVR consists of two or more DVRs of different feeders that are connected to a common DC link. When a fault occurs on one feeder, the DVRs of other feeders operate to replenish the DC link capacitors[3],[4]. The DVR of the faulted feeder utilizes the energy from the DC link for mitigating the fault on the feeder.

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This paper presents a simulation model of an IDVR consisting of only two feeders. It implements a voltage fed switched coupled inductor inverter strategy instead of a normal VSI [2]. The reference voltages are generated considering the phase advance angle that occurs during the fault. This voltage is compared with the load voltage using a fuzzy logic controller[5], [7]. The controller generates the pulses required for triggering the VFSCII.

## 2. INTERLINE DYANAMIC VOLTAGE RESTORER

An interline dynamic voltage restorer is similar to the interline power flow controller (IPFC) concept where the static synchronous series compensators (SSSC) of different transmission lines are commonly connected to a DC link. An IDVR consists of two or more DVRs connected to a DC link. Each DVR consists of an injection transformer, a filter and an inverter to which the DC link capacitor is connected. The filter is used to eliminate the unnecessary harmonic content present at the output of inverter. A schematic diagram of an IDVR with VFSCII and fuzzy control is given in Fig 1.where the two DVRs are connected across a common DC link. Here a fuzzy logic control strategy is implemented for triggering the inverter. The displacement angle or phase advance angle of the voltage input during fault is taken into consideration for giving the reference voltage input.During normal conditions each of the feeders operateindependently.

When a fault occurs at any of the feeders, the power flow between two DVRs through a DC link capacitor takes place. The DVR of the faulted feeder then operates in compensating mode to mitigate the problem [3][4]. The control logic for the triggering of inverters is done by considering the reference voltage across the DC link capacitor and the load voltage with its phase angle jump.

## 3. VOLTAGE FED SWITCHED COUPLED INDUCTOR INVERTER

The voltage fed switched coupled inductor inverter(VFSCII) is used instead of the conventional VSI's for its high voltage buck boost capability. It has the same principle of Z source inverter (ZSI) but requires only half the no of passive components used in ZSIand along with a greater shoot through capability for the same voltage gain [2]. It contains two modes of operation namely shoot through state and non-shoot through state. Shoot through means switching of the same leg thyristors during the voltage zero crossing instances leading to a short circuit condition and in turn can damage the inverter. To avoid this VFSCII consists of a diode and a mutual coupled inductor with a capacitor connected to one of the winding.

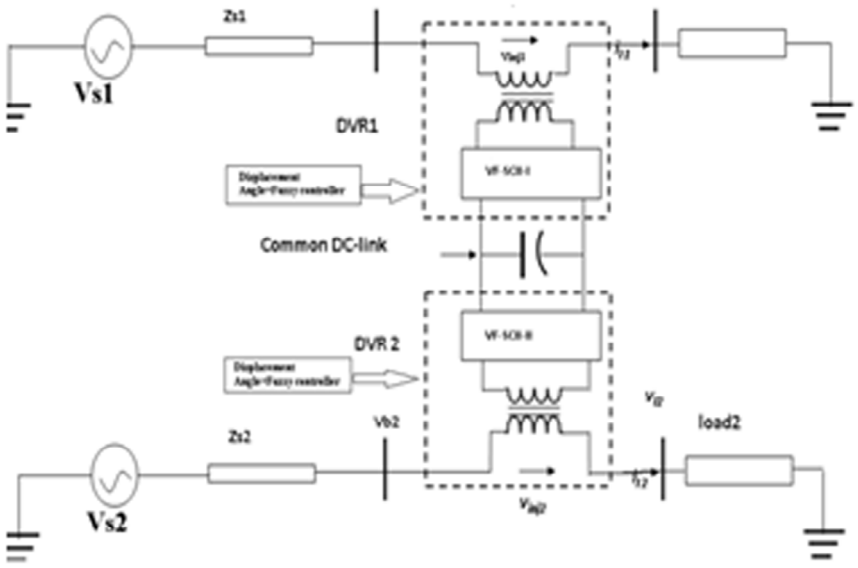


**Figure 1: Schematic Diagram of the proposed interline dynamic voltage restorer.**

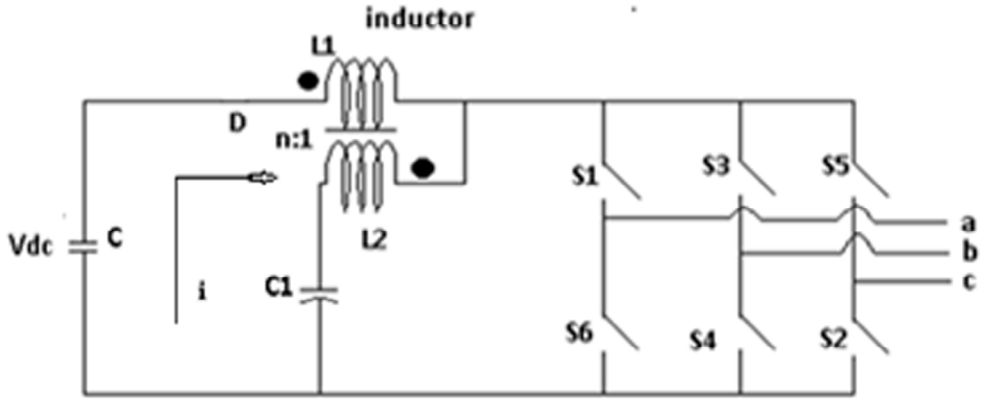


**Figure 2: VFSCII during normal state.**

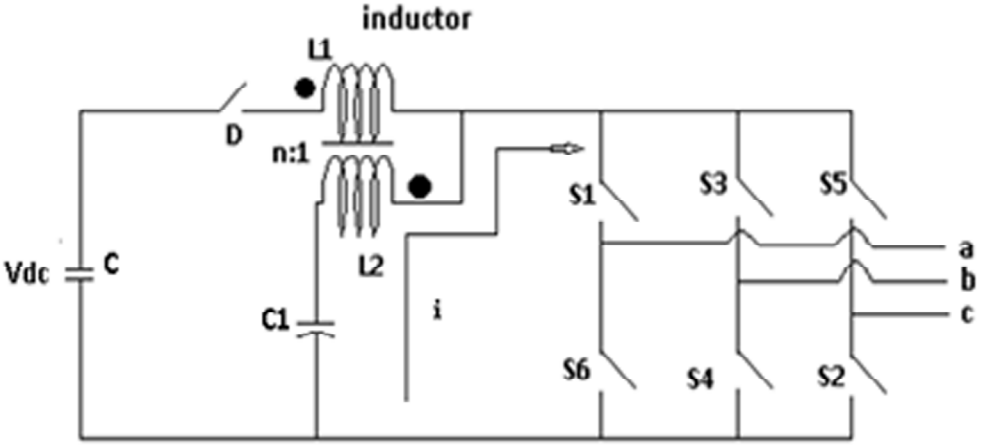


**Figure 3: VFSCII during shoot through state.**

Under normal conditions current flows from the source, charging the inductors and returns through the thyristors of the inverter. During this period the capacitor is also charged by the inductor winding L2. During the shoot through period the diode is switched off and no current flows from source. The charged capacitor discharges and makes the L2 winding to charge with the current flowing through the thyristors again. The total energy in the inductors during the switching period is to be maintained constant.

## 4. CONTROL STRATEGY FOR IDVR

### 4.1. Reference Voltage Generation

When the fault occurs at the second feeder, the converter of the first feeder is responsible for energizing the DC capacitor by transferring some amount of active power from the feeder 1 to the capacitor. The power exchange $P_{xg}$ is determined by the load voltage advanced angle β.

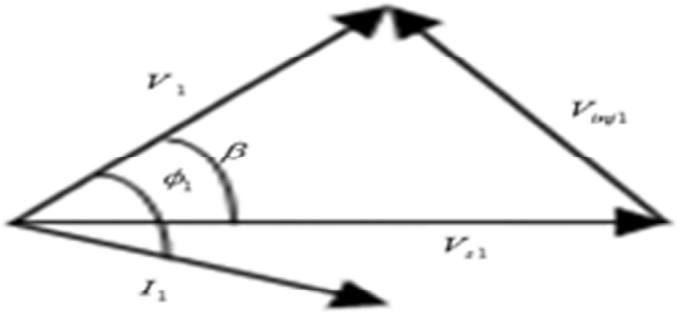


**Figure 4 : Phasor Diagram of Feeder-1**

$$P_{xg} = 3V_1 I_1 \cos(\phi_1 - \beta) - 3V_1 I_1 \cos\phi_1 \quad (1)$$

For the case of maximum power exchange $\phi_1 = \beta$, then $P_{xg}$ becomes

$$P_{xgref} = S_1(1 - \cos\phi_1) \quad (2)$$

This power is taken as the reference power exchange. Now the net reference voltage for the input of the fuzzy controller is obtained by considering the load advanced angle β which is calculated using the active current at the DC capacitor $i_{dact}$. This is calculated by considering the direct axis component that is in phase with the supply voltage $V_{1d}$. The net exchange power is divided with $V_{1d}$ to obtain $i_{dact}$. This is divided with the measured peak value of the load current $i_{p1}$.

$$P_{xg} = (V_{dcref} - V_{dc}) * (K_p + K_i / s) \quad (3)$$

$$P_{xgnet} = P_{xg} + P_{xgref} \quad (4)$$

$$i_{dact} = (2/3) * (P_{xgnet}) / V_{1d} \quad (5)$$

$$\beta = \phi_1 - \cos^{-1}(i_{dact} / i_{p1}) \quad (6)$$

Where $V_{dcref}$ and $V_{dc}$ are the reference and actual voltages of the DC link capacitor.

Now the *d* and *q* components of the reference voltage is obtained by,

$$V_{1dref} = V_{1m} * \cos\beta \quad (7)$$

$$V_{1qref} = V_{1m} * \sin\beta \quad (8)$$

The same equations are used for generating the reference voltage at faulted feeder except the power at the capacitor is also taken into consideration.

$$P_{xgnet2} = P_{xg2} + P_{xgref2} + 0.5CV_{dc}^{2} \quad (9)$$

Where *C* is the DC link capacitor value.

### 4.2. Fuzzy Logic Controlling Strategy

The *d* and *q* components from the load voltages are taken and are subtracted from their respective reference voltages generated considering the load advance angles [5]. This gives the error signal for each component. The

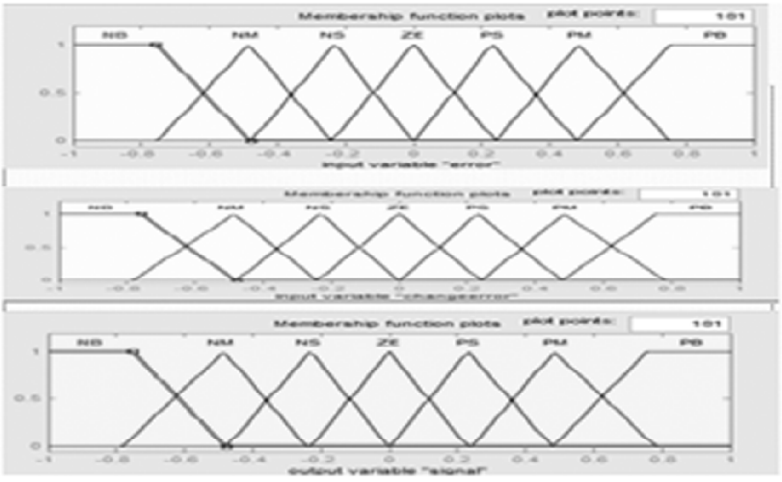


**Figure 5 : The membership functions for error, change in error and output signal.**

**Table 1**
**Rule base for fuzzy logic controller.**

| 'e' / 'ce' | NB | NM | NS | ZE | PS | PM | PB |
|---|---|---|---|---|---|---|---|
| NB | NB | NB | NB | NB | NM | NS | ZE |
| NM | NB | NB | NB | NM | NS | ZE | PS |
| NS | NB | NB | NM | NS | ZE | PS | PM |
| ZE | NB | NM | NS | ZE | PS | PM | PB |
| PS | NM | NS | ZE | PS | PM | PB | PB |
| PM | NS | ZE | PS | PM | PB | PB | PB |
| PB | ZE | PS | PM | PB | PB | PB | PB |

change in error signal is obtained by differentiating the error signal. The error and change in error is given as inputs to the fuzzy logic controller. Seven triangular membership functions are considered for each input and the output is also assigned with seven triangular membership functions. Centroid method is used for defuzzification.

## 5. SIMULATION RESULTS

The simulation for a three phase IDVR is carried out between two feeders each consisting of 11 KV in MATLAB-Simulink is shown in Fig 5. The corresponding DVRs are connected between the source bus and load bus. The DC link capacitor value is chosen as 750μF. Different fault conditions are considered and the output results are shown.

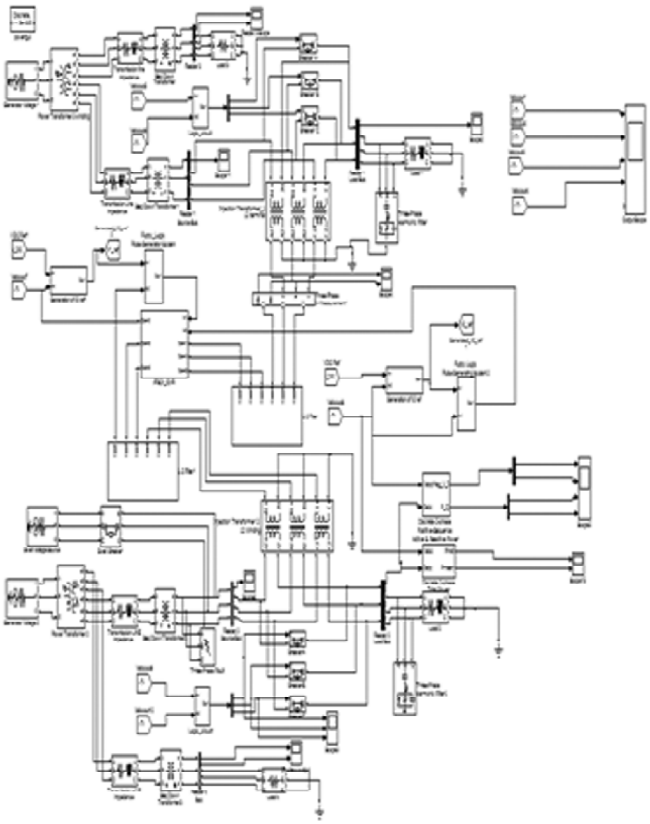

**Figure 6: Simulink Model of IDVR.**

**Table 2**
**Parameter details of the IDVR**

| *S. No* | *Parameters* | *Feeder 1* | *Feeder 2* |
|---|---|---|---|
| 1. | Source voltage | 11 KV | 11 KV |
| 2. | Load Resistance per phase | 1 ohms | 1 ohms |
| 3. | Load Inductance per phase | 0.01926 H | 0.01926 H |
| 4. | Injection Transformer (Line to Line) | HV Side-11 KV<br>LV Side-5 KV | HV Side-11 KV<br>LV Side- 5 KV |
| 5. | Filter inductance per phase | 10 mH | 10 mH |
| 6. | Filter Capacitance per phase | 750 μF | 750 μF |

### 5.1. During Voltage Interruption

A voltage interruption is created at the Feeder 2 by introducing a balanced 3 phase fault with fault and ground impedance values as 0.001Ω during the instant 0.4 sec to 0.6 sec. The waveforms for the output voltage of feeder 2 without and with compensation by IDVR are shown in the Fig 6 below.

### 5.2. During Voltage Sag

Voltagesag is created at the Feeder 2 by introducing a balanced 3 phase fault with fault and ground impedance values as 0.075Ω and 0.001Ω during the instant 0.4 sec to 0.6 sec. The waveform for the output voltage of feeder 2 without and with compensation by IDVR is shown in the Fig. 7 below.

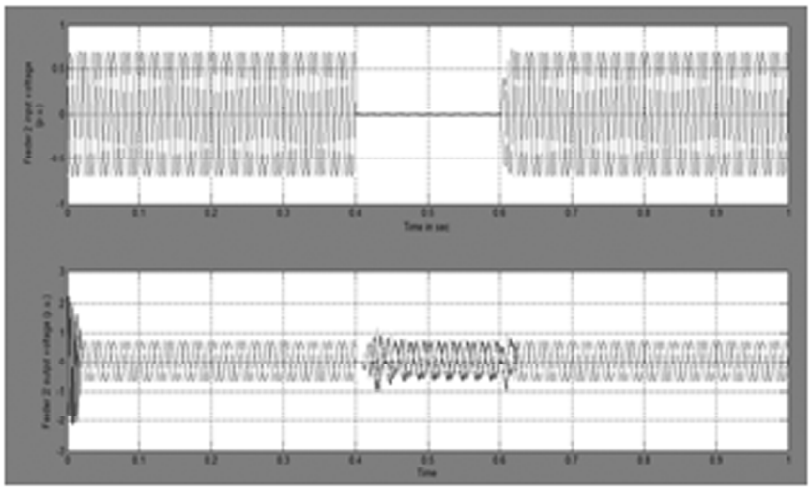

**Figure 7: Line voltages of Feeder 2 during an interruption without and with compensation.**

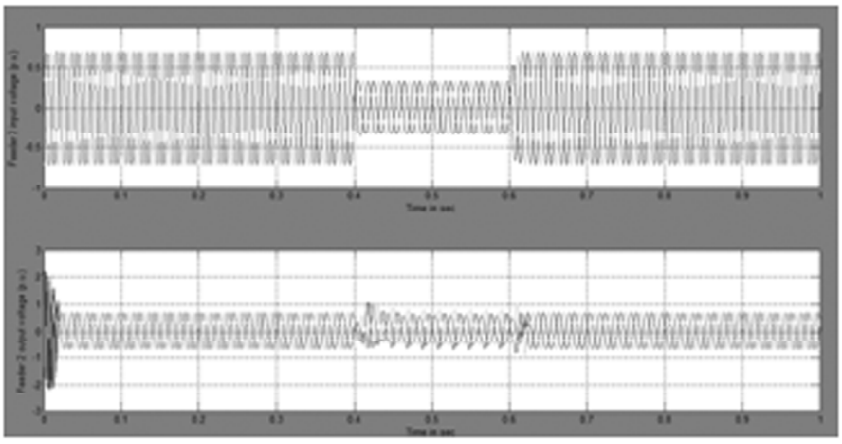

**Figure 8: Line voltages of Feeder 2 during a voltage sag without and with compensation.**

### 5.3. During Voltage Swell

A voltage swell is created at the Feeder 2 by introducing a an additional voltage of 7 KV during the instant 0.4 sec to 0.6 sec. The waveform for the output voltage of feeder 2 without and with compensation by IDVR is shown in the Fig. 8 below.

### 5.4. Un balanced Fault

The common unbalanced faults are single phase to ground fault, line to line faults and double line to ground fault. All these faults are analyzed separately during 0.4 to 0.6 sec and their waveforms are given in the Fig 10, 11, 12 respectively.

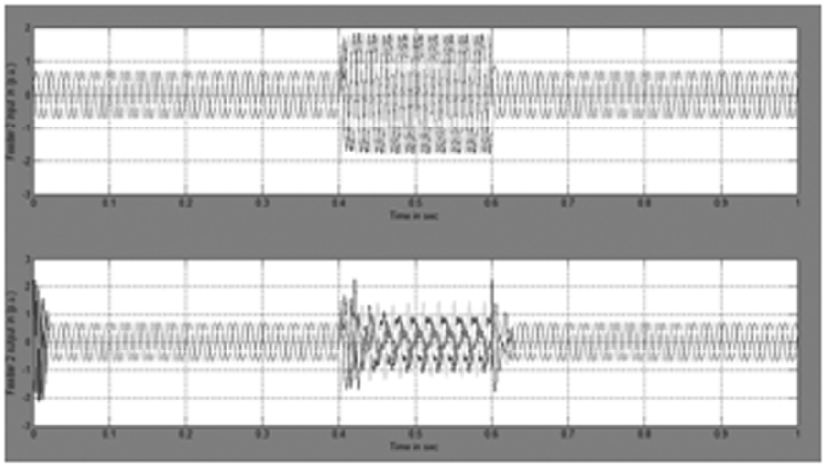

**Figure 9: Line Voltages of Feeder 2 during a voltage swell with and without compensation.**

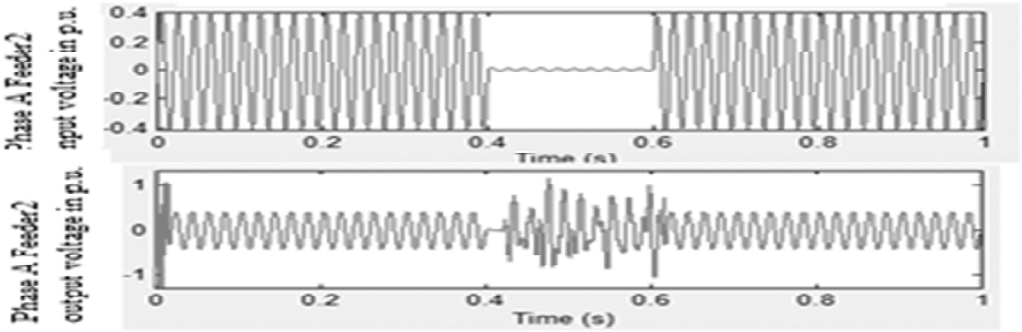


**Figure 10: Phase A voltage of feeder 2 during a L-G fault without and with compensation.**

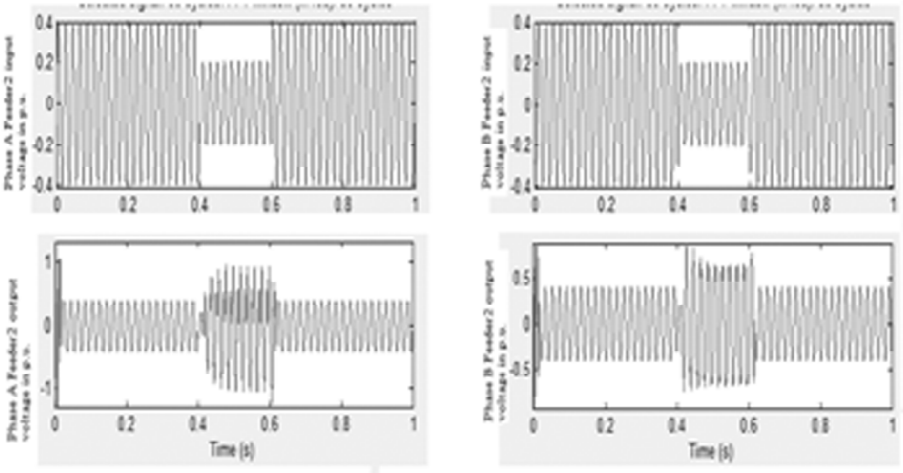


**Figure 11: Phase A and Phase B of Feeder 2 During L-L**

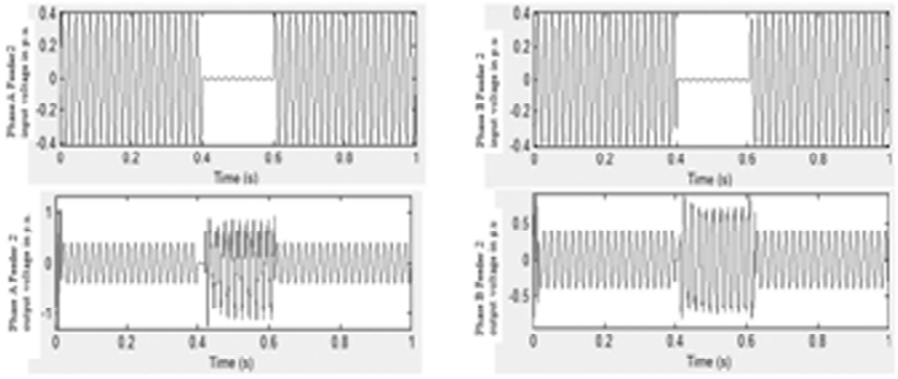

**Figure 12: Phase A and B of Feeder 2 during L-L-G fault.**

## 6. CONCLUSION

From the simulation outputs it can be seen that the IDVR is effective in mitigating the common power quality problems like voltage sag, voltage swell, interruption, unbalanced faults etc. Since these problems are mainly due to the nonlinear loads at the distribution side, using PQ compensators at the distribution side like IDVR would give an effective solution to these problems. Many heavy load centers are being supplied power from parallel feeders rather than single feeder for reliability and implementing IDVRs in between these parallel lines would improve the power quality at the load centers.

## REFERENCES


[1] Vilathgamuwa D.M , H. M. Wijekoon and S. S. Choi ,et al "Interline dynamic voltage restorer: A Noval and Economic Approach for Multiline Power Quality Compensation". IEEE Trans. Industrial Applications, Volume40, issue (6), pp.1678-1685, 2004.

[2] Qin Lei1, Fang. Z. Pengl and MiaosenShen2, et al "Switched-Coupled-Inductor Inverter". IEEE Trans. Industrial Electronics, pp.5280-5287, 2013.

[3] Usha Rani P, "Digital Simulation of Interline Dynamic Voltage Restorer for Voltage Compensation", JSIR, Vol. 1, issue 4, December 2014.

[4] Ramchandra Nittala, Alivelu M. Parimi, K. Uma Rao, "Comparing the Performance of IDVR for Mitigating Voltage Sag and Harmonics with VSI and CSI as Its BuildingBlocks," IEEE International Conference, SPICES, 2015.

[5] Md. RiyasatAzim, Md. AshrafulHoque, "A Fuzzy Logic based Dynamic Voltage Restorer for Voltage Sag and Swell Mitigation for IndustrialInduction Motor Loads", International Journal of Computer Applications (0975–8887)Volume 30– No. 8, September 2011.

[6] L. Gyugyi, K. K. Sen, and C. D. Schaude, "The interline power flow controller concept: A new approach to power flow management in transmission system," IEEE Trans. Power Del., vol. 14, no. 3, pp. 1115–1123, Jul. 1999

[7] Kinhal, V.G.; Agarwal, P.; Gupta, H.O., "Performance Investigation of Neural-Network-Based Unified Power-Quality Conditioner," Power Delivery, IEEE Transactions on , vol.26, no.1, pp.431,437, Jan. 2011.

[8] J. G. Niesen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," in Proc. 16thAnnu. IEEE APEC, 2001, vol. 2, pp. 1267–1273.

[9] Wijekoon, H.M. , Vilathgamuwa, D.M.; Choi, S.S. "Interline dynamic voltage restorer: an economical way to improve interline power quality" Generation, Transmission and Distribution, IEE Proceedings- Volume: 150 , Issue: 5, pp. 513–520, 2003.