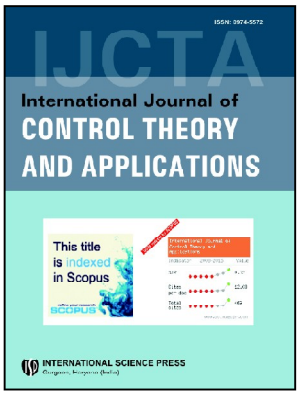

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Analyzing the Performance of Three Phase Five Level Inverter Fed BLDC Drive

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***Abstract*:** In high power medium voltage energy control the multilevel inverter technology placing major role. There are different topologies for multilevel converters. The CHB inverter is very popular among all the topologies which having the capability of using various dc voltages on each H-bridge units results in distributing the power conversion among higher voltage lower frequency and lower voltage higher frequency inverters. For a given number of semi-conductor devices available number of levels is high by considering the CHB as one unit. Different voltage levels for multilevel converters are taken and the output of simulation is represented in the form of THD. Based on switching and the no. of levels, the observed equation for highest order harmonic is obtained and applied to BLDC drive.

Keywords: Total Harmonic Distortion (THD), Cascaded H-Bridge (CHB) , Multilevel Inverters (MLI) , Pulse Width Modulation (PWM), Switching frequency

1. INTRODUCTION

In present days high power is required for many industrial applications. But sometimes medium and low power is required for operation in some applications in the industries. Using a high power source for all industrial loads may prove beneficial to some motors regarding high power, while it may damage the loads. Medium power is required for some motor drives and some applications. In 1975 MLI has been introduced as alternative in high power medium voltage situations. A group of power electronic devices and capacitor voltages are present in multilevel inverter, voltages with stepped waveform is generated as an output. Addition of high capacitor voltage is obtained at output is obtained due to the commutation of switches at the same time reduced voltage is withstand by the power semiconductors [1], [2], [3]. Figure 1 represents the different number of levels, of single leg phase of the inverter for several positions by using ideal switch the performance of devices can be observed. The two level output voltage, three level output voltage and so on is generated for the two level inverter, three level inverter and so on w.r.t the capacitor -ve terminal as shown in figure.

The output voltage have more steps which generates stepped output, by enhancing the inverter level, which has a reduced distortion [4],[5]. Due to the more number of levels the complexity increases and problem of voltage variations are introduced. For multilevel inverters three various topologies are introduced flying capacitor

clamped, diode-clamped and cascaded multi cell with isolated dc sources. For multilevel inverters control strategies and different modulation techniques have been adopted, which includes the following: sinusoidal PWM.

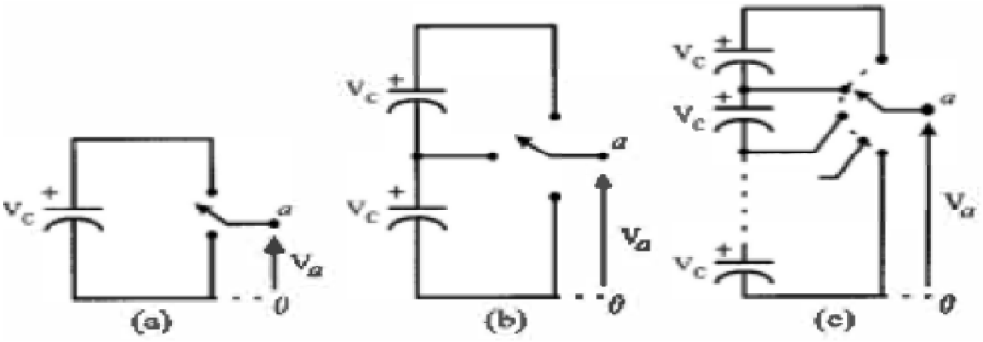

Figure 1: One Phase Leg on an Inverter with (A) Two Levels, (B) Three Levels, and (C) N-Levels

There are several advantages of multilevel converters when compared to two level conventional two level converter that uses high switching frequency pulse width modulation [6], [7]. Multilevel converter feature are as follows, (a) Staircase waveform quality: generating output voltages with very low distortion and also reduces dv/dt stresses by multilevel converters, so problems on electromagnetic compatibility (EMC) can be reduced. (b) Common-mode voltage (CM): smaller CM voltage is produced by the multilevel converters, so stress is reduced in the bearings of the motor connected to ML motor drive. (c) I_{input} : the less distortion of multilevel converter is drawn. (d) Switching frequency: The MLI will operate at greater switching frequency of higher value and also the switching fundamental frequency. Less switching frequency refers switching losses and also high efficiency. For multilevel inverters selection of switching techniques with different approaches are available. Finally in this paper simulation results for the 3-phase CHB inverter of five level which is applied to BLDC drive.

2. CASCADED H-BRIDGE MULTILEVEL INVERTER

The CHB with N number of levels MLI is having a connection of (N-1) 1-phase H bridges for each phase in series. Each of the H bridge comprises no. of separate dc source. The +Vs,-Vs and zero are the three output voltages which results 3*1/2(N-1) number of states. Where N-odd.

The single phase N-level cascaded multilevel inverter is observed in the figure-2. For each level and for each phase it requires separate power source this is the prescription. The dc supplies are replaced by the capacitors in the VA compensation and the losses are replaced by the inevitable energy of capacitor because of losses in inverter. The similar H-Bridges of modular structure is a +ve feature.

* The no. of levels K=2*N-1 in L-L voltage waveform
* In the line to neutral of star connected load the number of levels P=2K-1
* For each phase the required isolated sources or capacitors Ncap= ½(N-1)
* In each leg, the number of switches, Sn=(N-1)*2

Advantages

1. The number of dc sources are twice less than the possible output voltage levels present. (m= 2s+1)
2. The packaging and modularized output can made by the series of H-bridges. It will enhance the process of manufacturing and it can be done rapidly and with low cost.

Disadvantages

For each H bridges separate DC sources are required. This will limits its application to products that already have multiple SDCSs readily available.

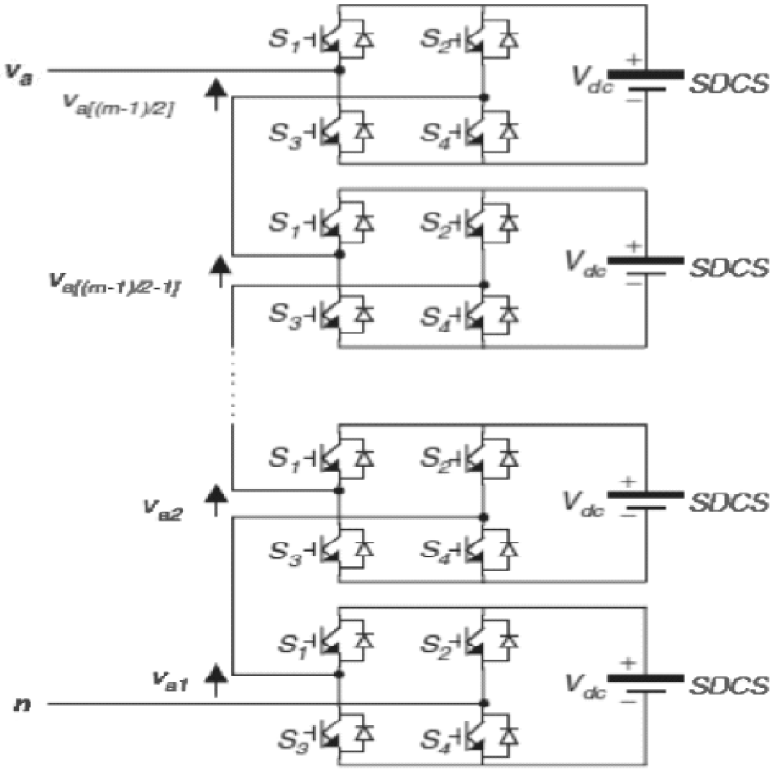

Figure 2: Three level Multilevel Inverter

(A) Full H-Bridge- 3 level Inverter

The configuration of full Hybrid-bridge is shown in figure. The 2 and 3 voltage levels are obtained from the 1-phase H-bridge. For full CHB inverter the no. of output voltage levels is 2n+1 and each level of voltage step is of Vdc/n. "n" means H bridges which are connected in cascaded manner. The switching sequence is represented in Table 1.

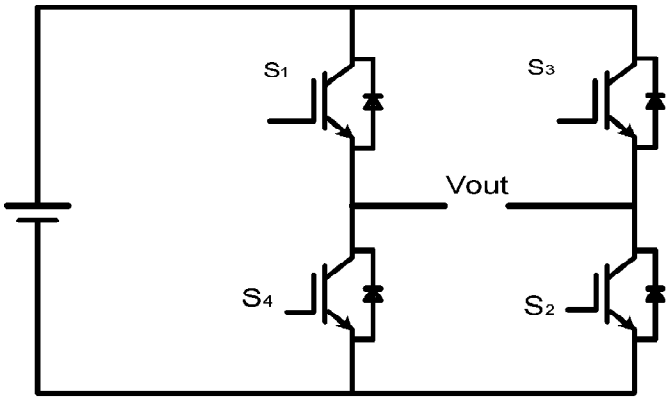

Figure 3 : Three level Full Bridge Inverter

Table 1
Full bridge inverter switching sequence

Switching state	*Output voltage*
S1, S2	0.5 Vdc
S3, S4	-05 Vdc

Table 2
Represents the three level inverter switching sequence

Switching states	*Output voltage*
S1, S2	0.5Vdc
S3, S4	-0.5Vdc
S2, S4	0

Table 2: switching sequence table for 3 level inverter full H-Bridge

(B) 5-level CHB-Inverter

The five level CHB is shown in figure and the switching states are given in the Table-3. In thesis CHB eight switches are present and for each state of switching a pair of switches are on/off and giving a Vdc/2 voltage level, so that we can observe the decrease in switching losses. The dv/dt for three level is Vdc but for the five level Vdc/2. The switching stress and the EMI will decrease as the dv/dt reduces**.**

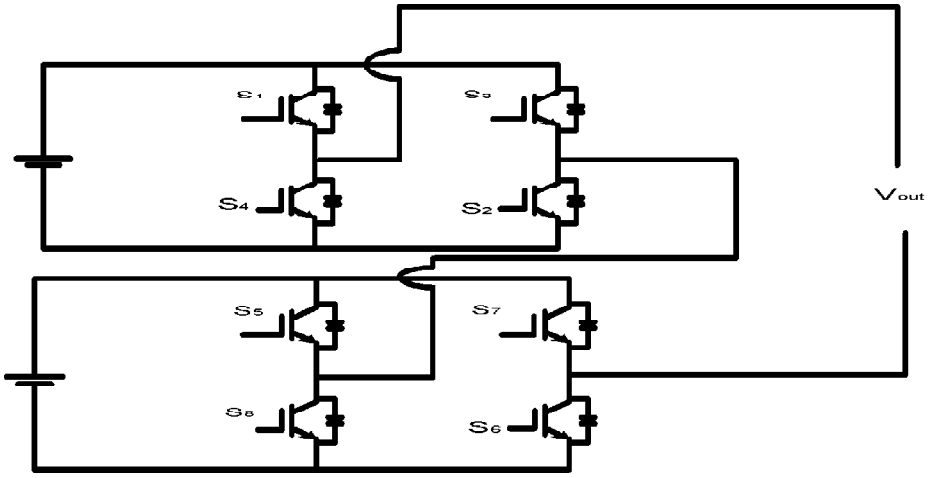

Figure 4 : CHB MLI of five level

Table 3
Five level inverter switching states

Switching states	*Output voltage*
S1,S2,S6,S8	0.5Vdc
S1,S2,S5,S6	Vdc
S2,S4,S6,S8	0
S3,S4,S6,S8	-0.5Vdc
S3,S4,S7,S8	-Vdc

3. PROPOSED SYSTEM

By using the Matlab/Simulink software the simulation is done and the results are shown. The arguments for the simulation are Vin dc =100v, the $f_{switching}$ is 3050 HZ

Level inverter with SPWM

Fig. 5 represents the simulink diagram of 3 level H bridge inverter with SPWM and figure 6 shows the output voltage level. From this we can observe the dv/dt value as 100V. Figure 7 represents the FFT analysis of the Voutput waveform. By observing this we can justify the frequency is 5950 to 6250 HZ and the dominant harmonic is shifted to high frequency zone.

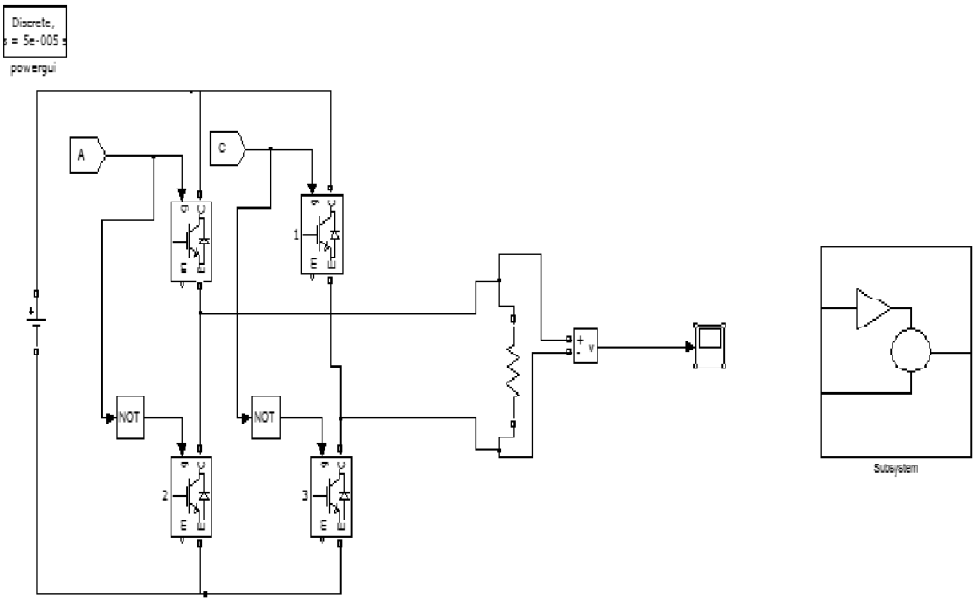

Figure 5: 3 level CHB MLI with PWM simulink model

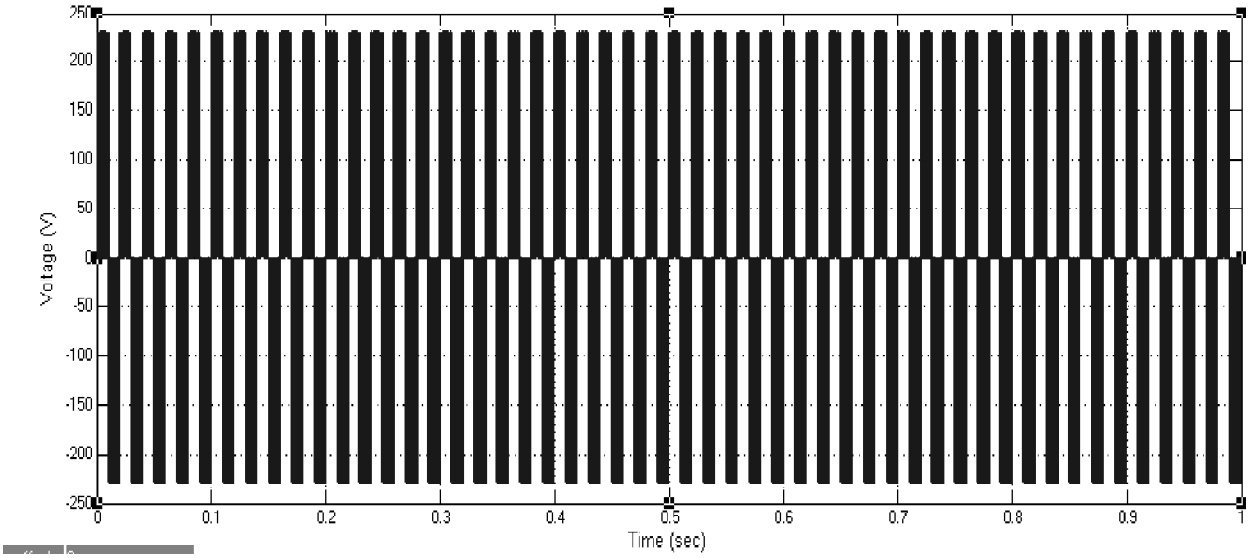

Figure 6 : 3 level CHB MLI Output voltage waveform

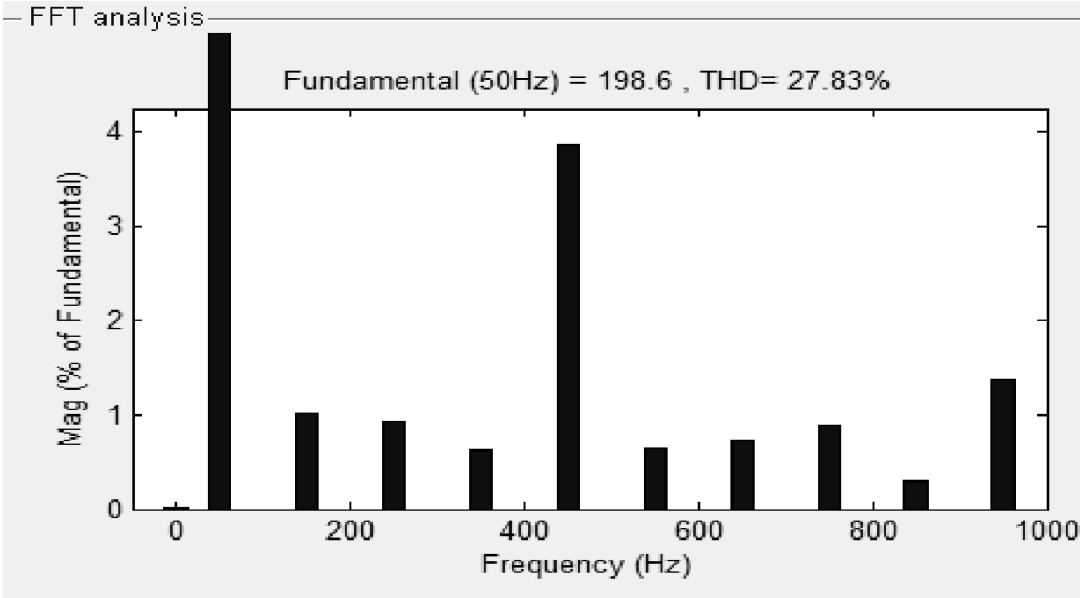

Figure 7: 3 level MLI CHB FFT analysis

(B) Five level CHB with sinusoidal PWM

The phase shifted carrier PWM of five level CHB inverter simulink model is observed in the Figure 8.

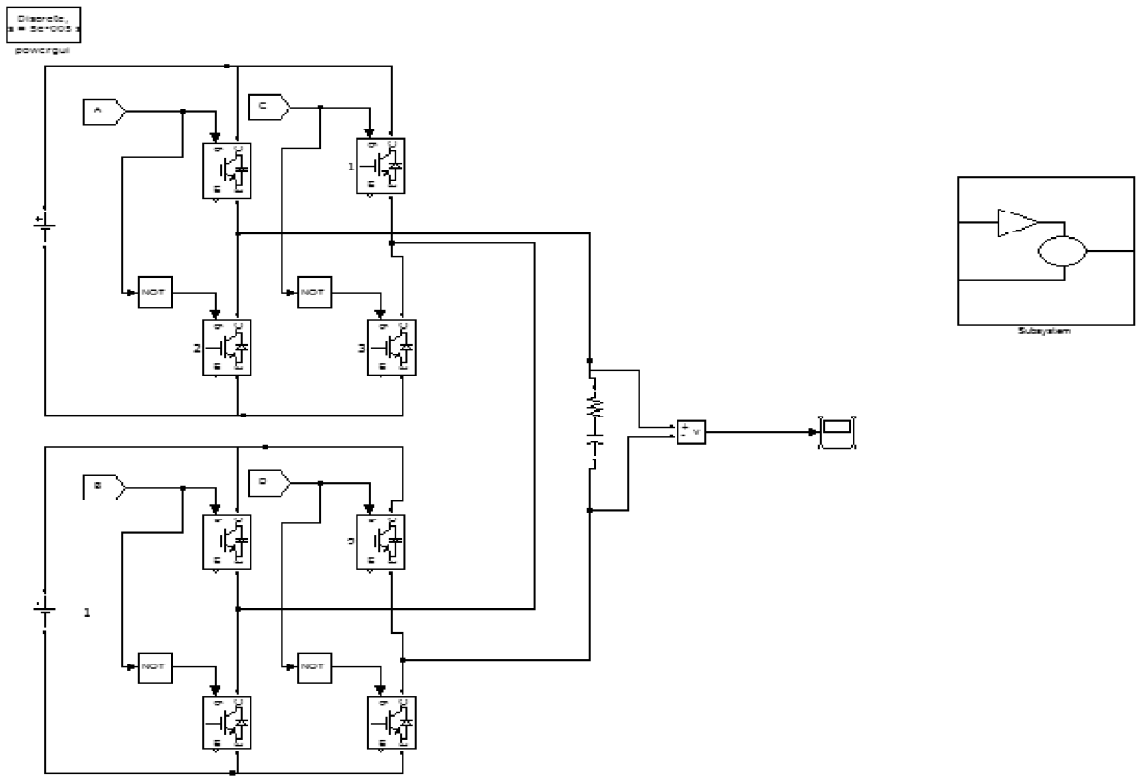

Figure 8 : 5 level CHB MLI with phase shifted PWM Simulink model

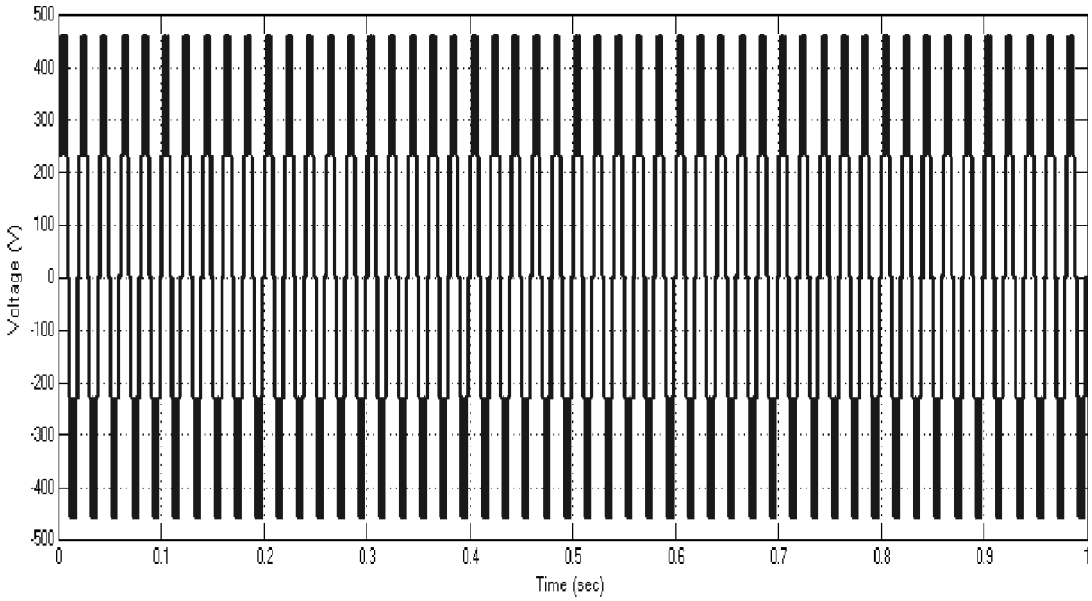

Figure 9 : 5 level CHB MLI output voltage waveform

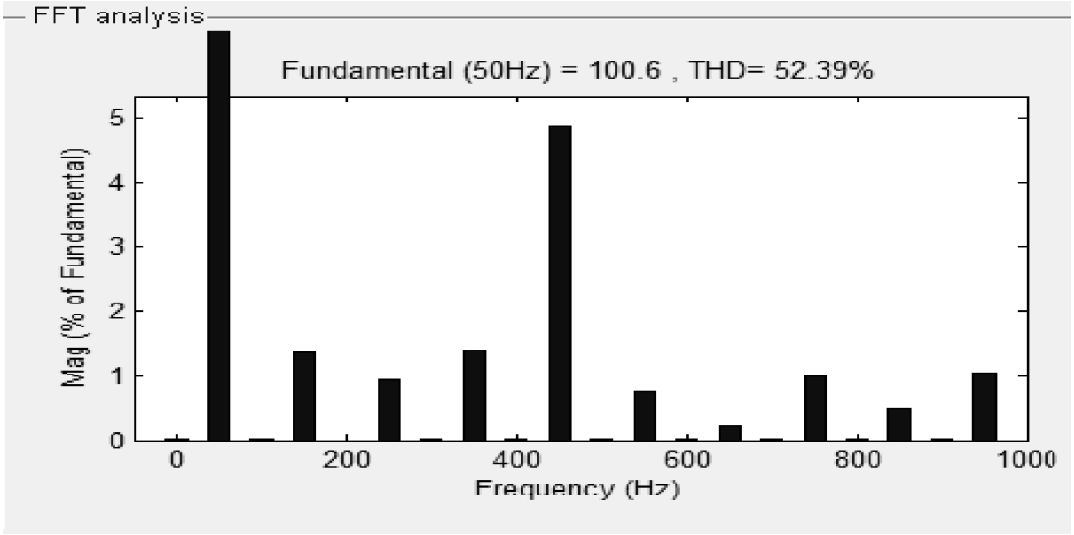

Figure 10: 5 level MLI CHB FFT analysis

From this we can observe that for 5 level cascaded H bridge the dv/dt value is 50V. Fig 10 represents the FFT analysis of Voutput. By observing this we can justify the frequency is 11950 to 12450 Hz and the high frequency zone is transferred to dominant frequency harmonics.

From the table 4 it is seen that when the number of levels are increased and by fixing the switching frequency the frequency of the dominant harmonic will become high.

Dominant harmonic equation is given by:

$$F_{\text{dominan}} = F_{\text{switching}} * (\text{levels} - 1) \pm (\text{levels}) * F_{\text{fundamental}} \quad (1)$$

From the above equation, it is observed that it is valid only for the level of inverters equal or greater than 3

Fdominant= 3050 * (5 – 1) ± (5) * 50

=11950 and 12450 Hz

As seen in table v we get same dominant frequency i.e, 12450 and 11950. In the below table 4 it is seen that when the fixed dominant harmonic frequency is applied, if no. of voltage levels are increased, $f_{switching}$ reduces, then it reduces the $L_{switching}$. For the given 3 level multilevel inverter switching frequency by knowing dominant frequency the 3 level inverter is replaced by MLI. Dominant frequency & the no. of levels are substituted in expression 1 the MLI $f_{switching}$ is observed. From the below table it is shown for a $f_{switching}$ of 3050 Hz that dominant frequency of 3 level is 5950 Hz.

Table 4
Dominant harmonic frequency of voltages levels and switching frequency

Number of levels	*Switching frequency in HZ*	*Dominant harmonic frequency*
CHB 3 level inverter with sinusoidal PWM	3050	5950 & 6250
CHB 5 level inverter with sinusoidal PWM	3050	11950 & 12450

4. FIVE LEVEL CHB MULTILEVEL INVERTER BLDC DRIVE

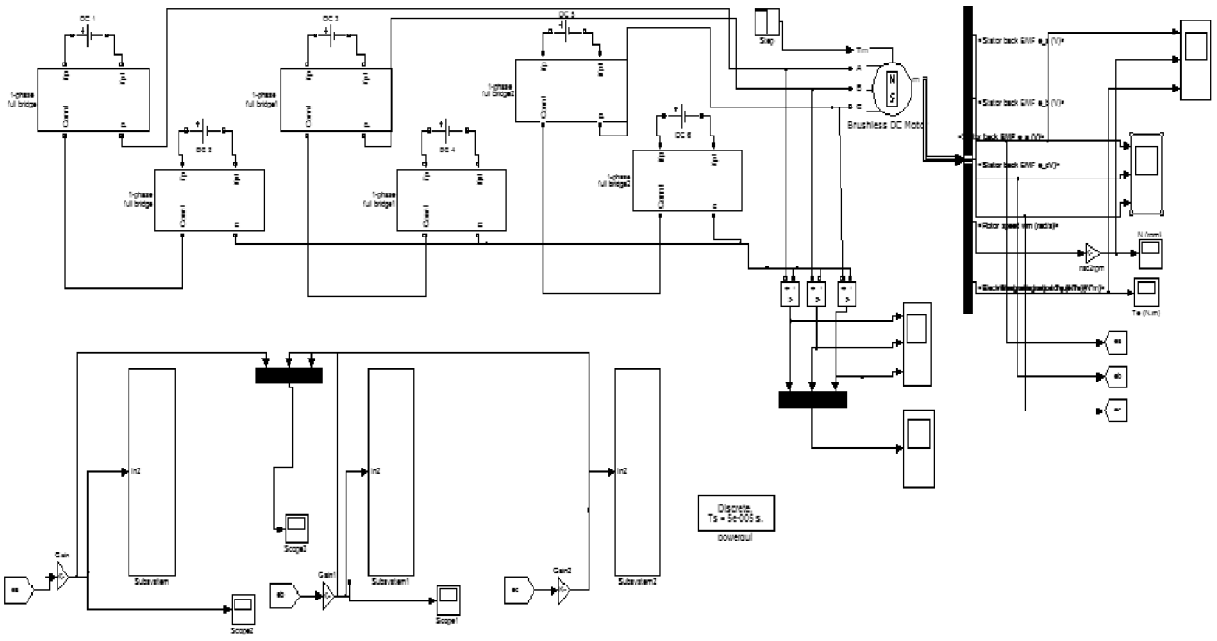

Figure 11: Simulation model for 5 level cascaded H-bridge MLI fed BLDC drive

In this, the 2 level CHB inverter fed brushless DC motor with level sifted carrier pulse width modulation block diagram is show in figure 11. The electro magnetic torque behavior which is generated placing a major role. The produced torque and the 5 level CHB inverter fed BLDC drive to the carrier level shifted pulse width modulation of output speed is shown in the Figures 12.

In figure 13 for each phase the stator-back-emf is represented and which equals to the currents in stator.

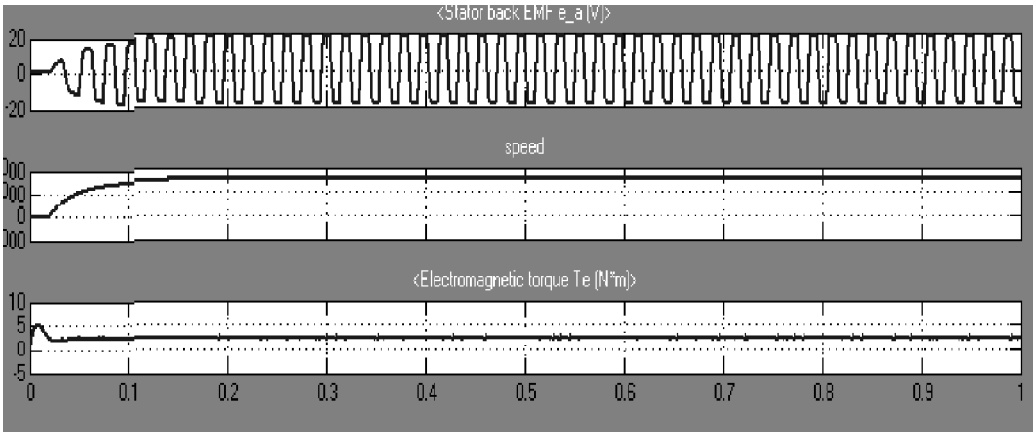

Figure 12: Electromagnetic torque and output speed of CHB inverter with five level fed BLDC motor

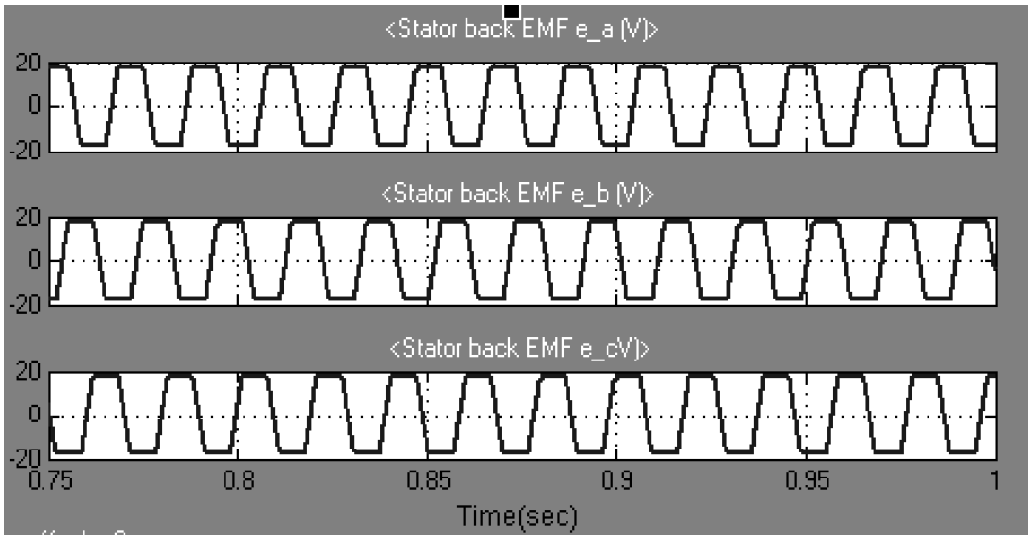

Figure 13 : Three phase stator back emfs

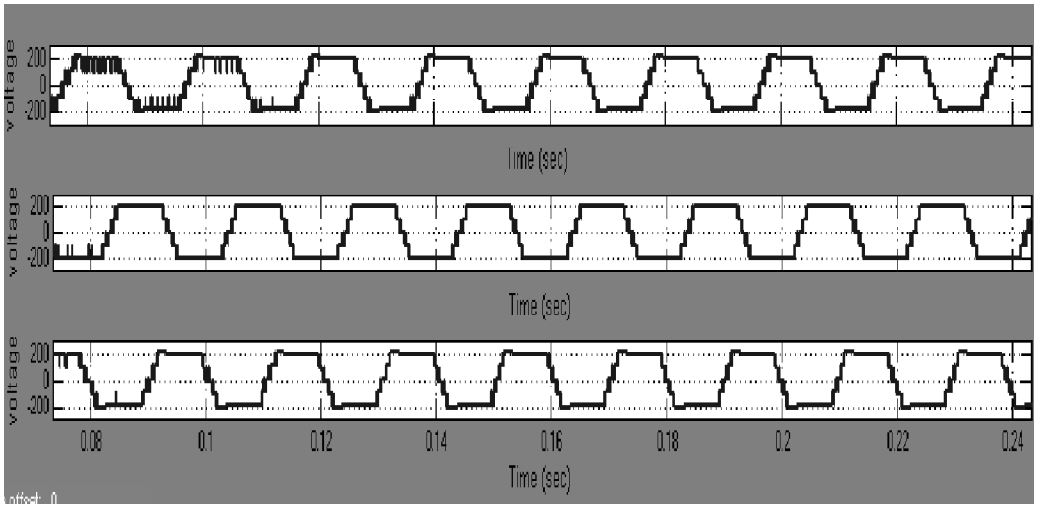

Figure 14: Three phase output voltage waveforms of CHB inverter with five level fed BLDC drive

The three phase five level CHB level shifted PWM inverter output voltages are shown in the figure 14.

5. CONCLUSION

The various types of multilevel inverters are discussed and among them the CHB inverter is chosen with the phase shifted PWM technique. The three and five level CHB multilevel inverters are simulated by using the MATLAB/SIMULINK and finally 3-Phase,5 level MLI is simulated and the output voltages and the harmonic distortion and represented and then those are fed to the BLDC drive. The harmonic expression is obtained mainly on the number of output levels and the switching frequency and also SIMULINK/MATLAB waveforms are obtained.

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