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FPGA Implememtation of Phase Shifted Carrier Pwmfor Switched Z Source Cascaded Multilevel Inverter in Speed Control of Induction Motor

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ABSTRACT

In this work, a FPGA implementation of phase shifted carrier PWM for switched Z source cascaded Multilevel Inverter in Speed control of induction motor is proposed. A novel VLSI architecture was developed in Virtex 5 FPGA for Phase shifted carrier PWM. The Developed VLSI architecture for the proposed carried PWM is fed to a switched cascaded Z source cascaded multilevel inverter and the speed of the induction motor is controlled. The implemented system is closed loop in nature and the developed VLSI architecture will act as PI controller. The realized FPGA with the power circuit has a less voltage and current total harmonic distortion, voltage stress across the switches and fast settling time. The speed control characteristics of the induction motor were studied with this developed FPGA controlled power circuit. The phase shifted carrier PWM was found to exhibit less stator current THD and a higher torque when compared to other PWM techniques used to control the power circuit. The simulations were done using Matlab/ Simulink and the results were validated using values obtained in real time using the hardware.

Keywords: VLSI architecture for Phase shifted Carrier PWM, FPGA, Cascaded Multilevel Inverter, Total Harmonic Distortion.

1. INTRODUCTION

The output voltage is derived from different levels of the input DC voltage source in a multilevel inverter. The inverter level increases with increase in the number of DC source. Multilevel inverters are generally used in power hungry applications such as motor drive, flexible AC transmission systems and UPS system [1]-[2]. The main disadvantage of the multilevel inverters is that the voltage amplitude at the output is restricted to the summation of DC voltage sources. So an interlevel power circuit is required to increase or decrease the multilevel inverter voltage at the output. In order to avoid the former problem, a multilevel inverter with Z source was produced [3]-[4]. If the voltage levels of the inverter increases then the number of switches would also increases. This causes the stress across the switches to increase thereby the loss across the switches to increase [5]. Over the years cascaded multilevel inverter has different topologies which include mixed multilevel inverters [6], soft switched multilevel inverters [7] and hybrid multilevel inverters [8]-[9]. These different multilevel inverters increases the voltage levels number so that a wide range of voltage and power in an inverter is obtained. This results in non increase in switching frequency and hence the output voltage has less ripple content. Many scholars have introduced different levels of multilevel inverter with various Pulse width modulation techniques. These PWM techniques were implemented using microcontrollers or Microprocessors or DSP controllers. Implementation of PWM

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technique in FPGA was not attempted by many researchers. The paper mainly focuses on the development of Phase shifted carrier Pulse width modulation on a Field Programmable Gate Array using (FPGA) VHDL language. Latter the FPGA would be used for controlling the speed. Section 2-5 illustrates the operation of Cascaded Multilevel inverter. Section 6 gives the different PWM techniques used for comparison. Section 7 deals with simulations and comparisons of different PWM technique on the proposed power circuit interfaced with the induction motor. Section 8 deals with the proposed VLSI architecture on FPGA for phase shift carrier PWM technique. Hardware used in making of the system is illustrated in Section 9. Section 10 gives the conclusion of the paper.

2. CASCADED MULTILEVEL INVERTER

The Cascaded multilevel inverter does not require any voltage clamping diodes or voltage balancing capacitors like DCMLI. The seven level multi level inverter is obtained by cascading three full bridge inverter circuits. The three full bridge inverters are connected in series and a single phase output is considered as shown in Figure 1. Each full bridge is fed from separate DC source along with Z-source. The number of output levels m in each phase is related to number of full bridge inverter unit's n by, m = 2n+1. Here number of levels is seven, hence number of inverter circuits connected in in series is there. The single phase seven level topology of cascaded H bridge multilevel inverter is shown in Figure 1.

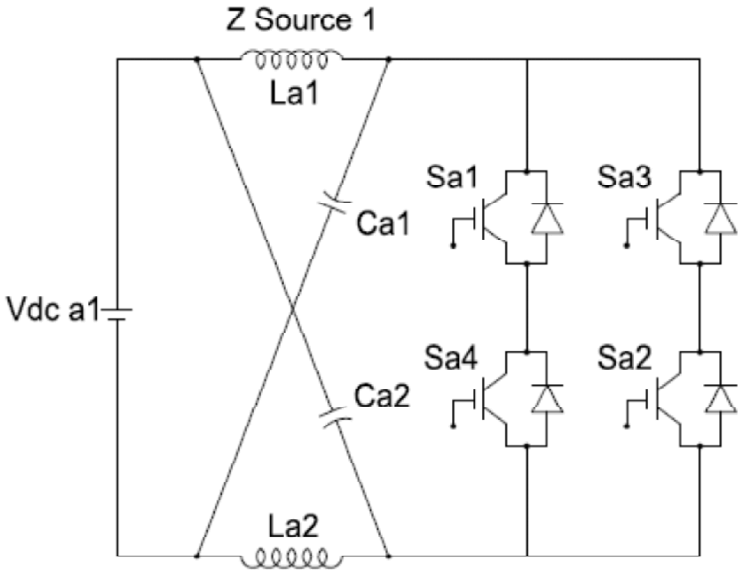


Figure 1: Single Phase Seven Level Z –Source Cascaded H-Bridge Multilevel Inverter

Each H Bridge is fed with same value of DC Voltage hence it can be called as symmetrical cascaded multilevel inverter. Each full bridge inverter can generate three different voltage outputs + Vdc, 0, -Vdc. The output voltage is synthesized by sum of three inverter outputs are at three angles. These three angles are used for giving pulses to twelve switches. The switching pattern for single phase seven level topology of cascaded H-bridge multilevel inverter is shown in Table 1. The output waveforms are shown in the Figure 2.

3. SWITCHED INDUCTOR Z-SOURCE CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

This topology has wide difference from view of existing structures. It has got the initial solution for the conflicts caused by Modulation Index and D, for the high power quality and high boost invention ability. The Seven level Inverter consists of three Z-source modules connected to Three H Bridge and are cascaded

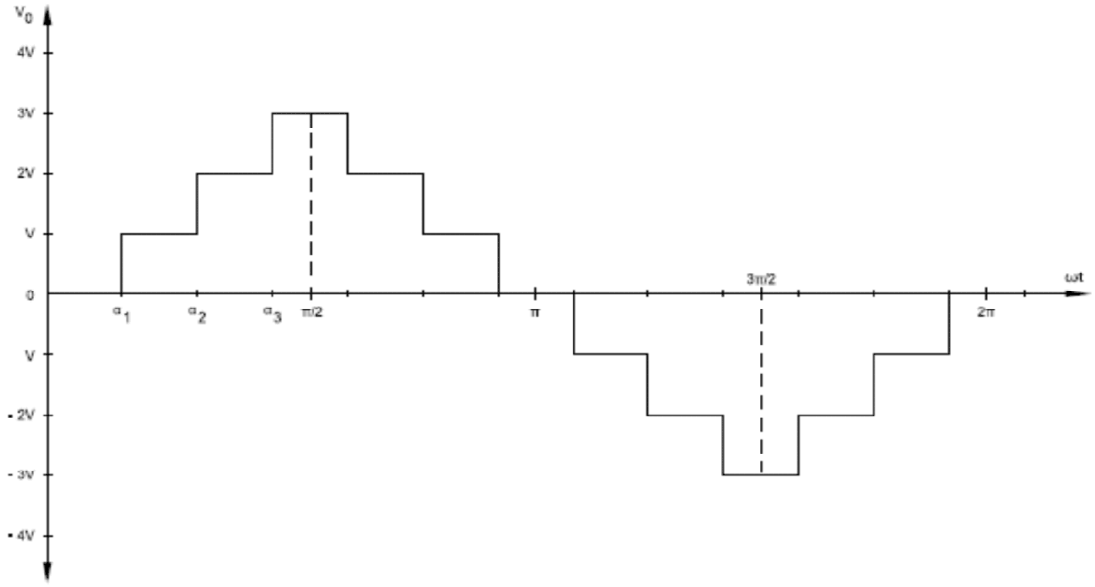


Figure 2: Voltage Wave form of Seven Level Cascaded Multilevel Inverter

among each other as shown in Fig 3. For the purpose of explanation the power circuit was explained with one basic Z –source unit connected with one H Bridge is considered. Each basic Z –source unit consists of one voltage source and two capacitor (C1& C2) and inductor (L1& L2) connected as X shape and two switched inductor cells (top cell & Bottom cell), one at the top of the z –source and the other at the bottom of Z-Source module. The DC voltage can be acquired from the rectifier along with Z source network. The seven level yield waveform is acquired by various switching combinations. The switching pattern for three phase seven level topology of the cascaded H-Bridge multilevel inverter is shown in Table 1.

4. MODE 1- NON SHOOT THROUGH MODE

The equivalent circuit during non-shoot through mode is shown in Figure 4.The inverter is in a non-shoot through state that is one of the six active states and two traditional open zero states and inductor current meets the following inequality:

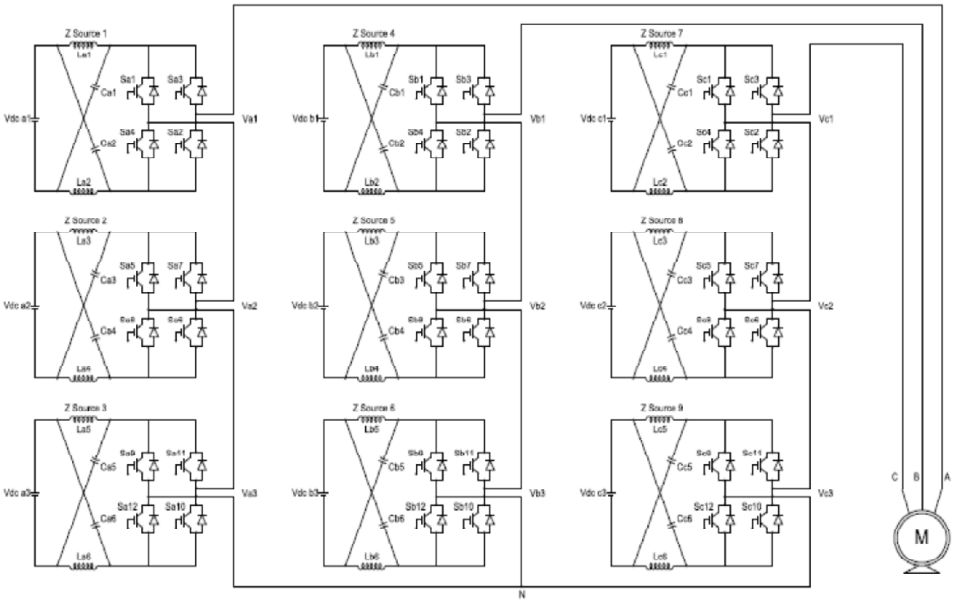


Figure 3: Seven level Cascaded H-Bridge Multilevel Inverter

Table 1
Switch States for three phase seven level Cascaded Inverter

SWITCH STATE												*Output Volt (Van)*
S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*S9*	*S10*	*S11*	*S12*	
1	1	0	0	0	1	0	1	0	1	0	1	+ V
1	1	0	0	1	1	0	0	0	1	0	1	+2V
1	1	0	0	1	1	0	0	1	1	0	0	+3V
0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	-V
0	0	1	1	0	0	1	1	0	1	0	0	-2V
0	0	1	1	0	0	1	1	0	0	1	1	-3V

The equivalent circuit during non-shoot through mode is shown in Figure 5. The inverter is in a non-shoot through state that is one of the six active states and two traditional open zero states and inductor current meets the following inequality:

$$\mathbf{i_L > 0.5\ I_i} \tag{1}$$

In this mode, the input DC current is

$$\mathbf{I_{in} = I_{L1} + I_{C1} = I_{L1} + (I_{L1} - i_1) = 2i_L - i_1 > 0} \tag{2}$$

Voltage across the inductor is

$$\mathbf{V_L = V_0 - V_C} \tag{3}$$

Where $\mathbf{V_0}$ is the source voltage and Inductor current linearly decreases.

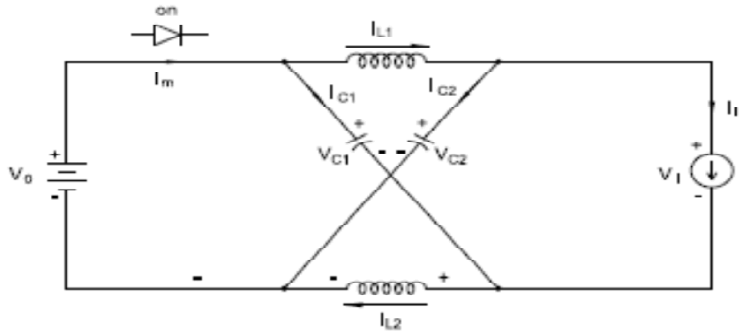


Figure 4: Non Shoot through Mode equivalent circuit

5. MODE 2- SHOOT THROUGH MODE

The equivalent circuit in shoot through mode is shown in Figure 5. A switch shoot-through zero state occurs when the switches in any of the three phase legs are gated simultaneously.

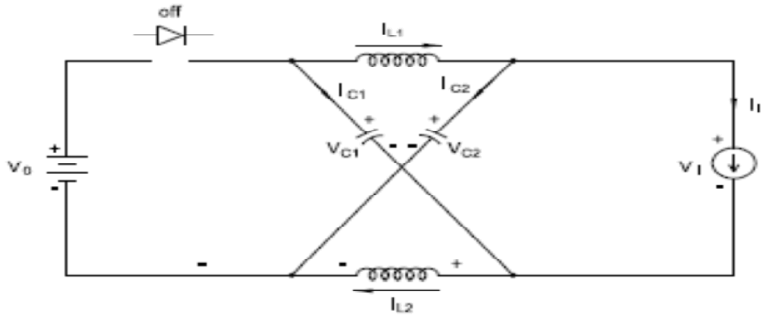


Figure 5: Shoot through mode equivalent circuit

This mode produces a zero voltage vector at the inverter output like open mode and contributes to the total active length of zero voltage state.

In this mode VC1 + VC2> V0 (4)

The diode is reverse biased, and the capacitors charge the inductors.

The Voltages across the inductors are:

VL1 = VC1 and VL2 =VC2 (5)

The inductor current linearly increases.

6. PWM TECHNIQUES

The PWM techniques used for switching multilevel inverters are carrier based PWM technique and space vector PWM technique. The former is easy to implement and more flexible. A triangular carrier waveform is used as a carrier and a sinusoidal signal is used as reference signal in a SPWM technique. Further the carrier signals are classified into Phase disposition (PD), Phase Opposition Disposition (POD), Phase shifted (PS) control technique, super imposed carrier, alternate POD and Hybrid technique. In this paper cascaded Multilevel inverter is simulated using PD, POD, PS technique.

6.1. Phase shifted carrier control technique: (PS)

In this PWM technique there exists a 90 degrees phase shift to each other in the carrier wave. Triangular waves used will have same frequency and amplitude from peak to peak. For a m voltage level required, m-1 carrier signals are required and they are shifted in phase by an angle è=(360°/m-1). Figure 6 illustrates the Phase shifted carrier control technique [13].

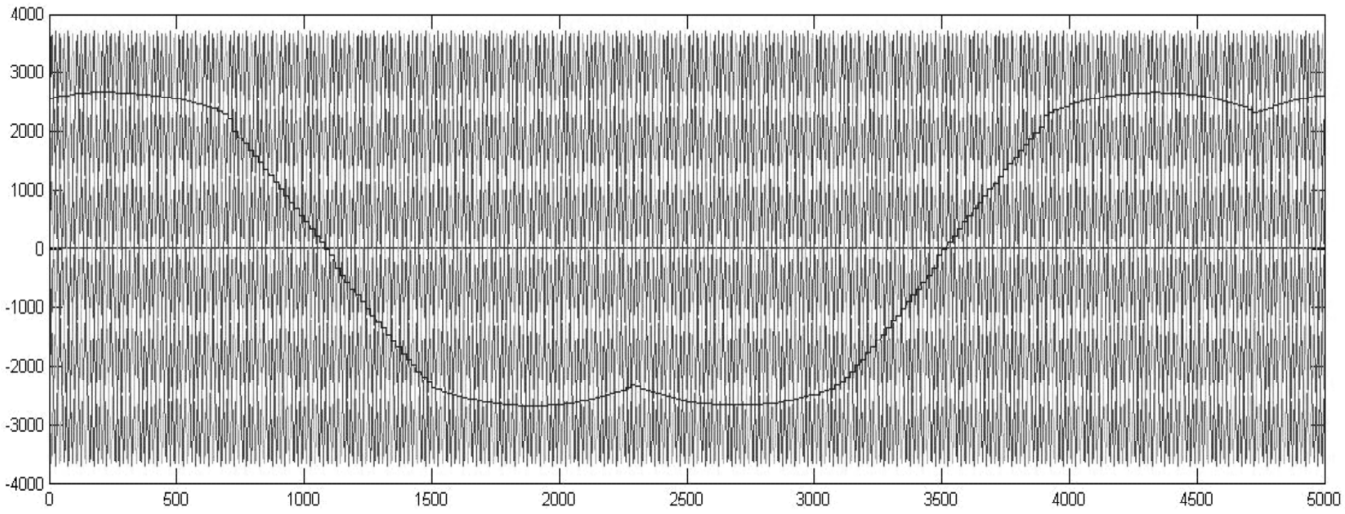


Figure 6: Phase shifted carrier control technique

7. SIMULATION RESULTS AND DISCUSSIONS

The cascaded multilevel inverter is fed to an Ac drive was simulations were carried out for three different PWM techniques such as PD, POD and PS. The quantitative parameters such as phase voltage THD, line voltage THD, Stator current THD, settling time and Stress across switches were compared based on the PWM technique applied to the power circuit. The entire simulation was done in MATLAB and the results are shown below. Matlab 2014b version was used for all the simulation.

Table 2
Comparison of different measures on various PWM techniques on seven level cascaded multilevel inverter

PWM Technique	*Phase Voltage THD*	*Line Voltage THD*	*Stator Current THD*	*Voltage Stress*	*Speed settling time*
PD	25.33%	9.29%	1.4%	50V	0.2sec
POD	25.32%	13.35%	1.27%	50V	0.2sec
PS	26.78%	15.48%	0.69%	50V	0.21sec

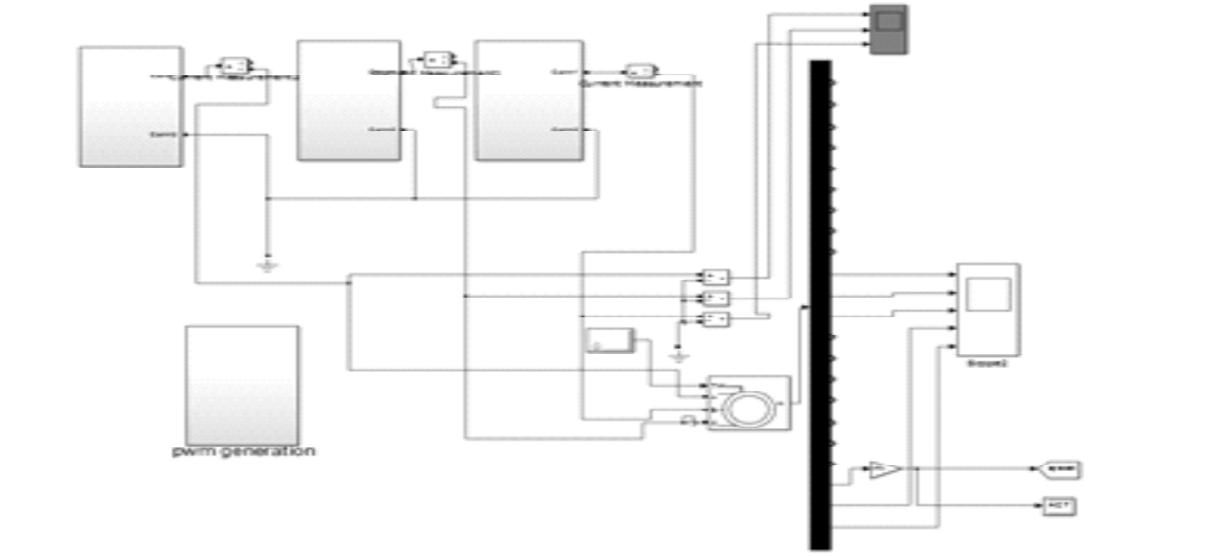


Figure 7: Simulation of seven level diode clamped multilevel inverter

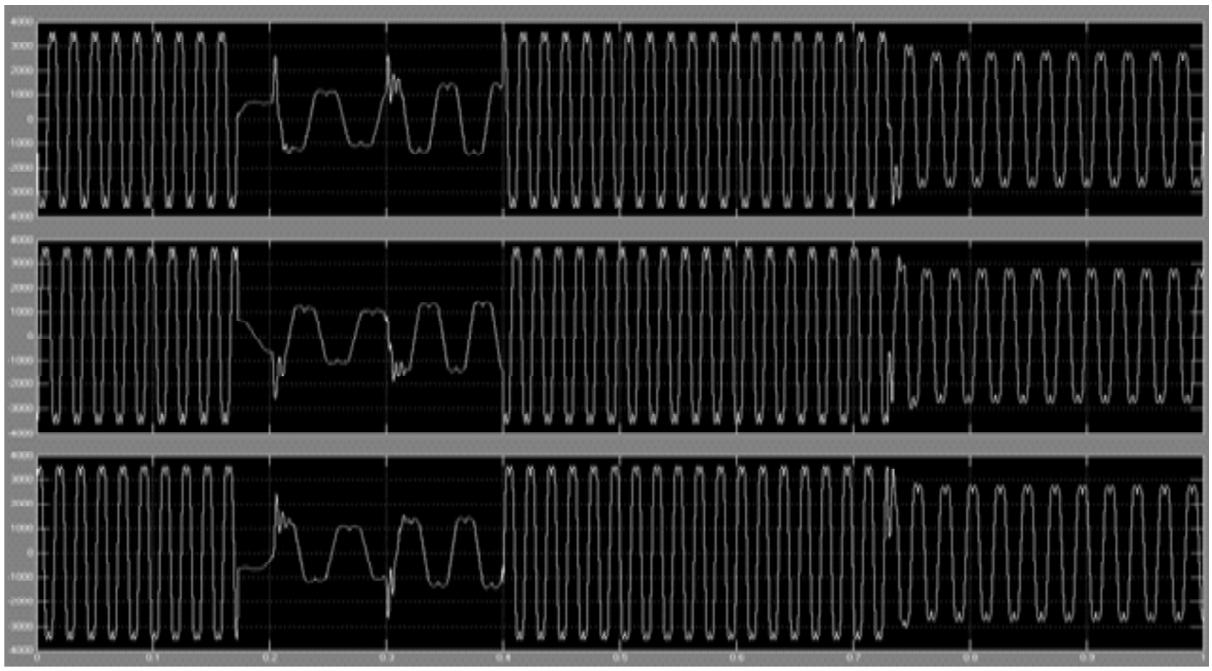
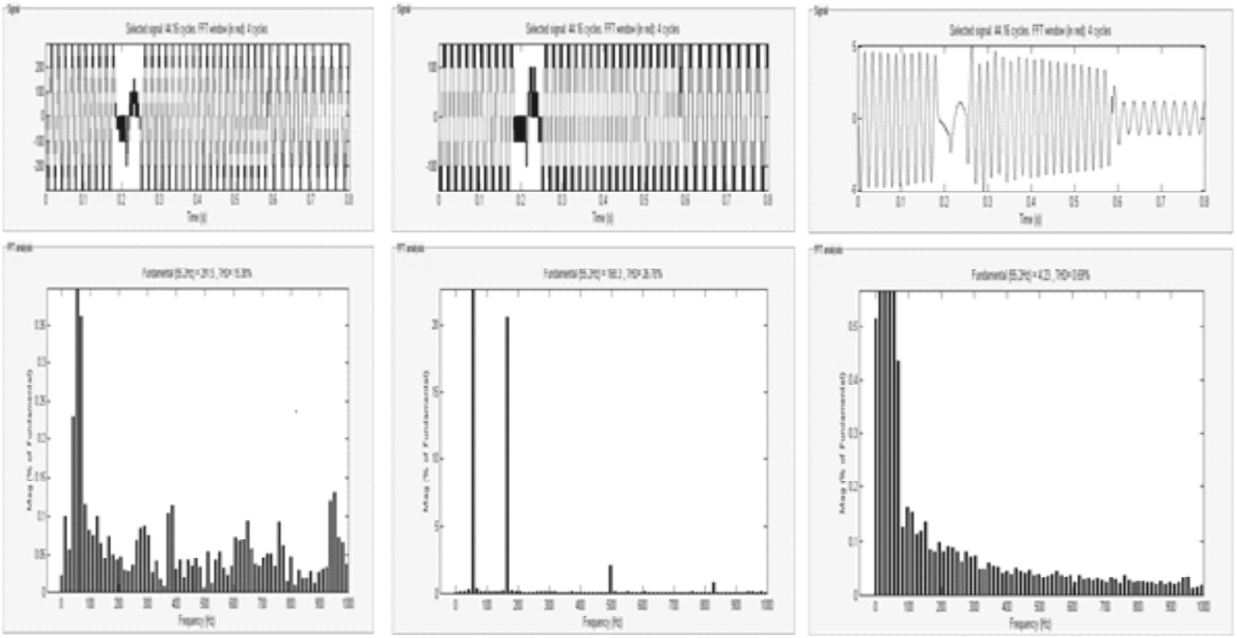


Figure 8: Third harmonic injected reference waveform

Table 1 gives the quantitative performance measures of different PWM techniques on Cascaded Multilevel inverter. Figure 7 illustrates the simulation diagram of cascaded multilevel inverter fed to a AC drive. Figure 8 gives the third harmonic injected reference waveform. Table 2 gives the comparison of

different PWM Techniques of cascaded multilevel inverter during the simulation. Figure 9 gives the line to line voltage, phase voltage and stator current THD measured during simulation for PS PWM technique. Table 3 gives the design parameters used for simulation. Figure 10 gives reference and actual speed of induction motor. The closed loop constants were obtained from Zeiger Nichols method. Figure 10 gives the result of the speed test conducted on the induction motor.



(a) **(b)** **(c)**

Figure 9: Various THD measured during simulation for PS PWM technique. (a) Line to line voltage THD (b) Phase voltage THD (c) Stator current THD

Table 3
Parameters used of power circuit used for simulation

DC Link Voltage	300 V DC
Inverter Power Rating	200 Watts
Inverter Output Voltage	0-200 V AS Rms (Line to Line)
Switching Frequency	2000 Hz
No. of Carrier used	6 Nos.

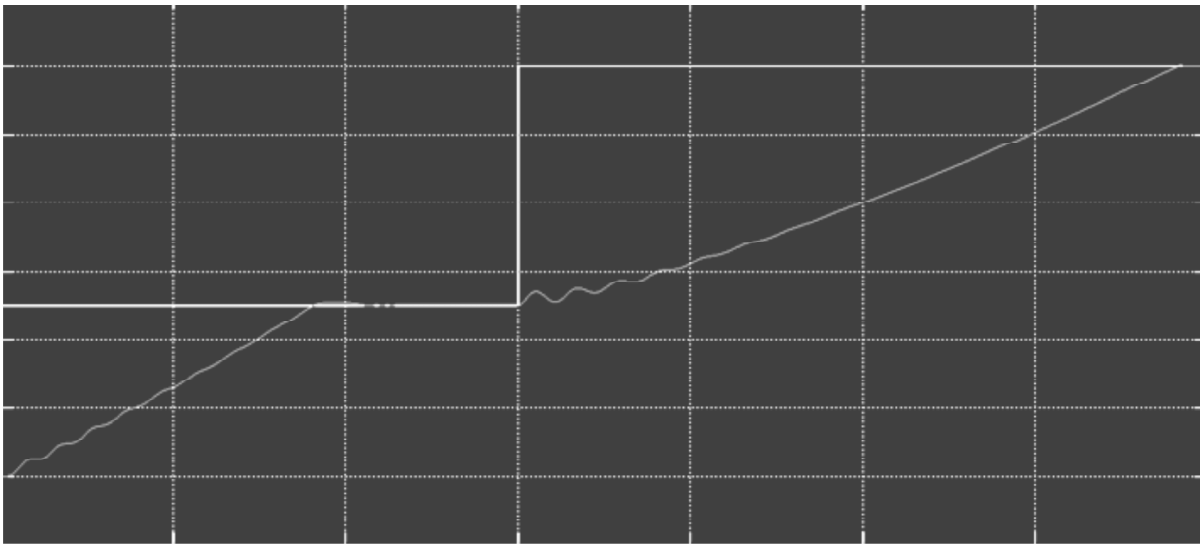


Figure 10: Reference and actual speed

8. FPGA IMPLEMENTATION OF PHASE SHIFT CARRIER DISPOSITION PWM

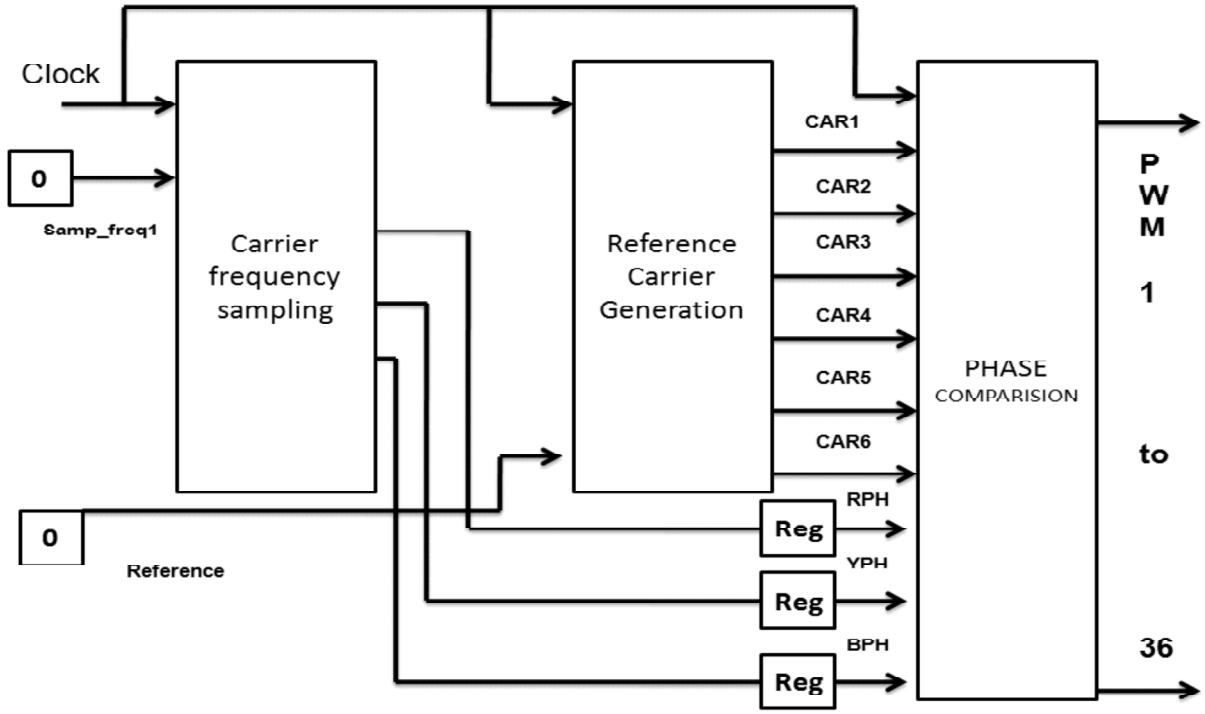


Figure 11: SPWM Architecture for Cascaded MLI

The Proposed Architecture for PS PWM technique is sequential in nature as shown in Figure 11. It consists of three main modules. The three modules are Carrier frequency sampling module, Reference carrier generation module and phase comparison module. The FPGA board used in the work operates at 20 MHz and we consider the carrier frequency to be 10 KHz. The carrier frequencies are build using up counters.

8.1. Carrier frequency sampling Module

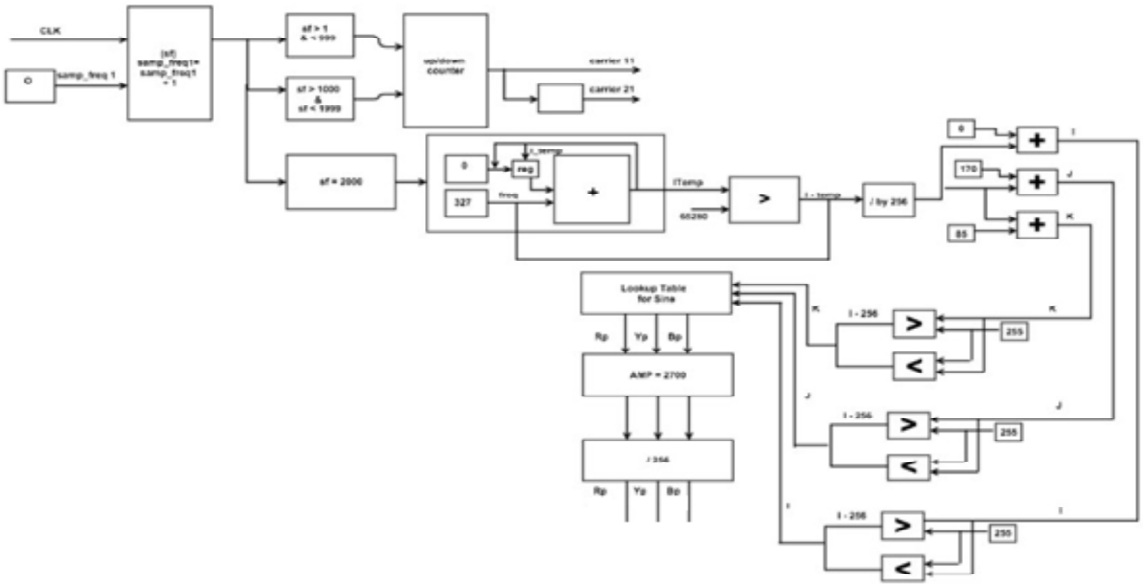


Figure 12: FPGA architecture for Carrier frequency sampling module

In the carrier frequency sampling module, the sine signal is initially sampled. As the carrier frequency is assumed to be 10Khz a Up counter is designed to count the carrier samples till 10 KHz i.e., (1000). When it counts to the maximum value a down counter is implemented to count the values till the next 10 KHz i.e., (2000). Every 10 KHz the frequency value is updated. The maximum value of the frequency update register is 65280. The maximum value is divided to get values 0 to 255. 65280/256 = 255. Now the signal looks like a Ramp signal. Next the index value for the sampled carrier signal will take a sine value. The sine wave is generated using a look up table. A RAM is implemented for sine wave generation. All the operation were considered to be 8 bit in nature and hence the maximum value will be 255. Hence 255 is equated to 360 degrees. Hence 1 degree is equal to 0.71.Multiplying with 0, 120,240 with 0.71 will give the index for RED phase, BLUE phase and YELLOW Phase. These values yield 0,170 and 85 indicating the RED phase, Yellow phase and Blue phase start with 120 degrees difference between each other. These index are stored in variables called i, j ,k respectively. If any of the value of the indices are greater than 255 then the value is made as zero else left with values as such. All the signals are considered as unipolar hence the signal s are multiplied with the formulae

RPHSE SINE = (SINE(RPHINDEX)*AMPLITUDE/256)

BPHSE SINE = (SINE(BPHINDEX)*AMPLITUDE/256)

YPHSE SINE = (SINE(YPHINDEX)*AMPLITUDE/256)

The above equation results in a waveform that is bipolar in nature (i.e., -AMP to +AMP). A value of 1000 is added to the expression in order to make the signal unipolar (the values will be from 0 to +Amp). Figure 12 illustrates the FPGA architecture for Carrier frequency sampling module .

8.2. Reference Carrier Generation Module

In order to generate reference signal for all the three phases the signals start to count at different points. A Reference signal is generated for 10 KHz. There are three reference signal generators. The first reference signal generator initially counts upwards and then downwards. An up counter that counts value till 1000 (for 10 KHz) is generated. When the up counter value reaches 1000 a down counter is initiated. This counter counts downward for the next 1000 values. The output is named as CAR. The Second reference signal generator counts down till 333. After reaching 333, an up counter starts to up counts from 333 to 1333 and down counts again from 1333 to 2000. This illustrates that the second phase also counts 1000 (for 10 KHz). This output is named as CAR1. The third reference signal down counts the value till 666 and starts counting upward from 666 to 1666. After reaching 1666 the counter starts down counting from 1666 to 2000. This output is termed as CAR2.

In order to bring the shift in generated frequency the generated reference signals CAR, CAR1, CAR2 is subtracted with 2000 to obtain CAR3, CAR4, and CAR5 respectively. These CAR, CAR1, CAR2, CAR3, CAR4, CAR5 are the output of reference signal generation module. For the generation of 36 PWM we require 5 reference signals which are illustrated above in Figure 13.

8.3. Phase Comparison Module

The output of the Carrier sampling module and the output of the reference generation module are compared. Signals CAR, CAR1, CAR2, CAR3, CAR4, and CAR5 are compared with the sinusoidal signal of RED phase. If the reference generation module is less than carrier sampling module then the output is made as one else it is zero. In similar terms all the signals CAR, CAR1, CAR2, CAR3, CAR4, and CAR5 are subtracted from 100 to repeat the above operation. This operation results in 12 PWM outputs. The reason to subtract CAR, CAR1, CAR2, CAR3, CAR4, and CAR5 with 100 is to create a dead band to avoid two switches closing at a time. Similarly the same operation is repeated in YELLOW and BLUE phase resulting in 36 PWM pulses as shown in Figure 14.

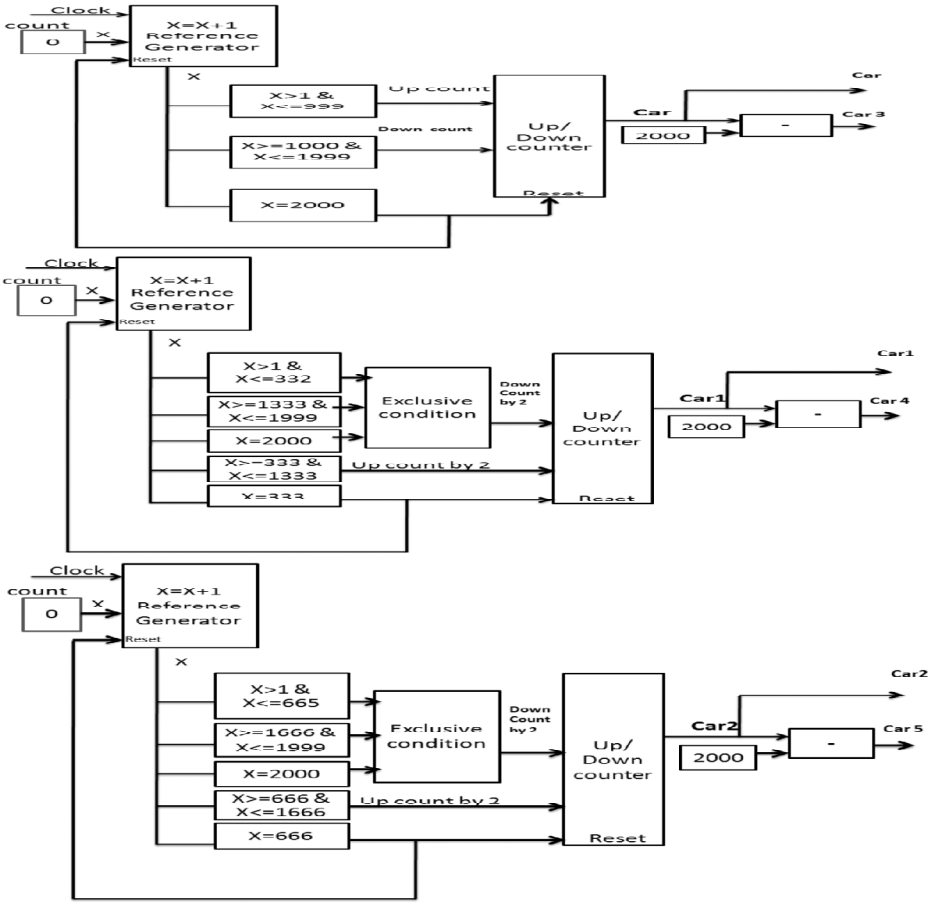


Figure 13: Carrier Generation Module

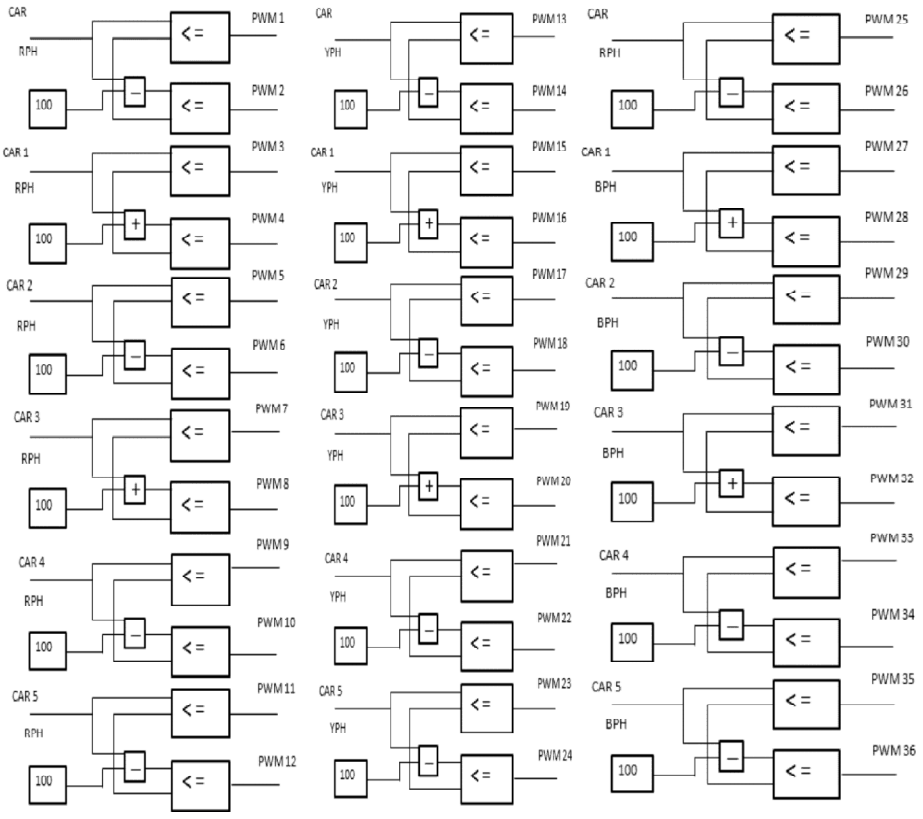


Figure 14: Phase Comparison

8.4. Discussions on FPGA development

Figure 11 gives the Proposed Sequential Architecture for PSPWM. Figure 12 gives VLSI architecture for the carrier frequency sampling module. Figure 13 gives the VLSI architecture for the reference carrier generation module and Figure 14 illustrate the VLSI architecture developed for phase comparison module. The developed codes were using VHDL. Codes were simulated using the third party simulation tool modelsim and the codes were synthesized using Xilinx XST. Figure 15,16 gives the simulation result of the different carrier generated in phase shifted carrier PWM using modelsim. Figure 17 gives the simulated output of the reference signals generated for Phase shifted carrier PWM. Figure 18,19 gives the PWM output generated for phase shifted carrier PWM. After the simulation the codes were synthesized using Xilinx XST. The codes were targeted for 6slx25ftg256-3 FPGA. Section 4.5 briefs with the device utilization summary of the developed VHDL code for phase disposition PWM. It was found that the developed architecture operates at 43.717Mhz, consumes 1105 slices.

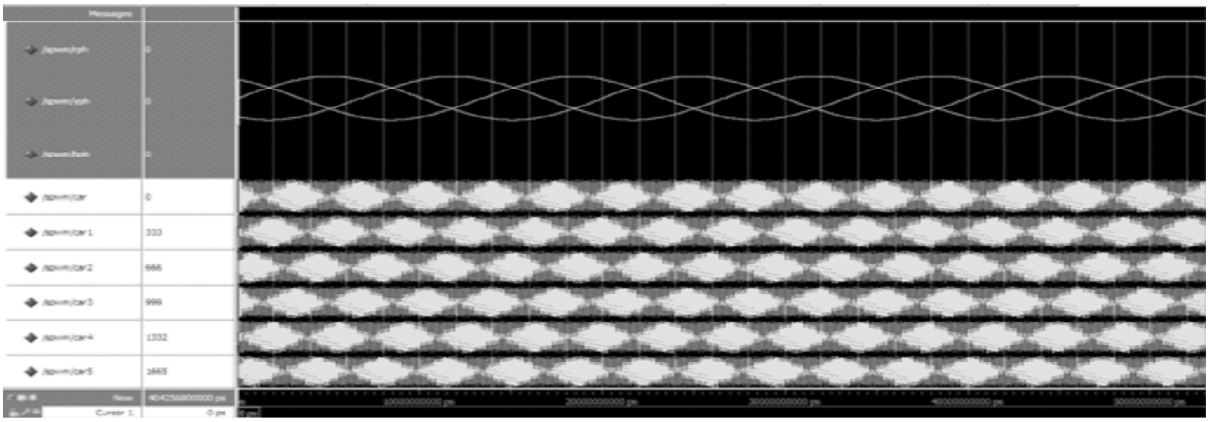


Figure 15: Carrier Reference -1

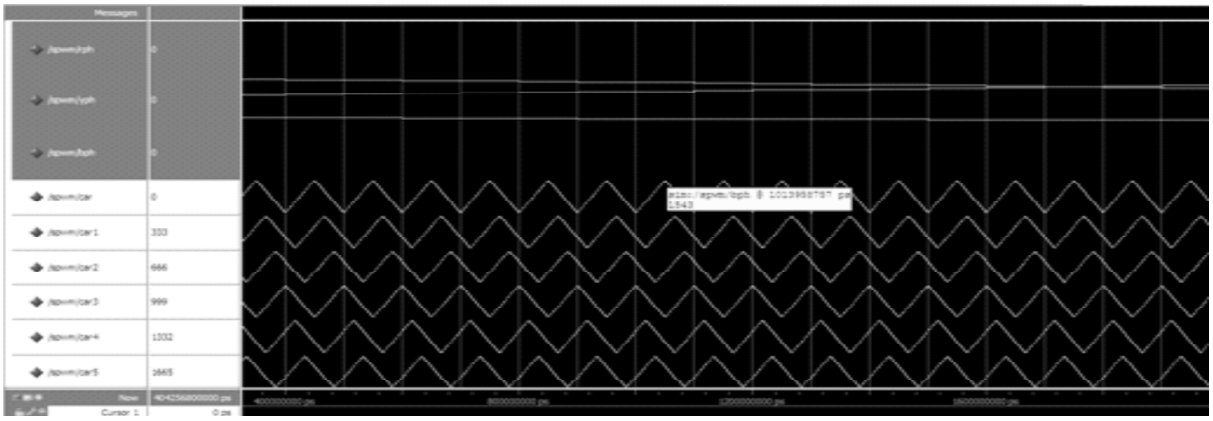


Figure 16: Carrier Reference -2

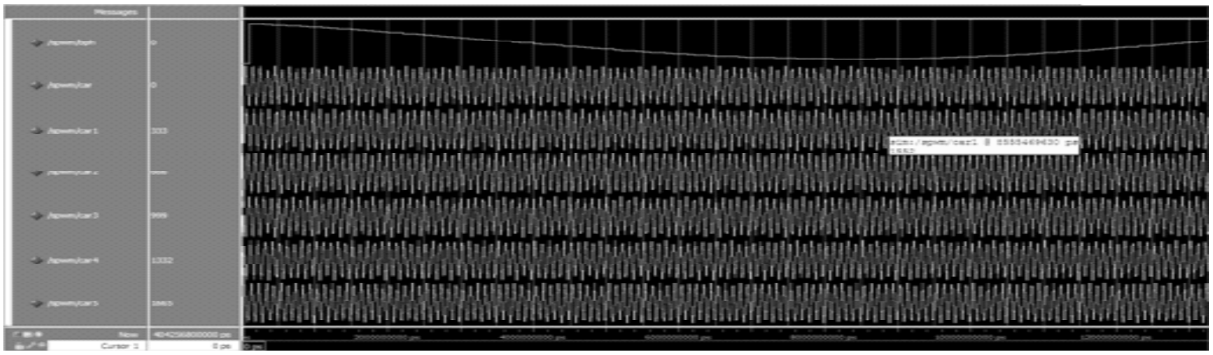


Figure 17: Reference Signal

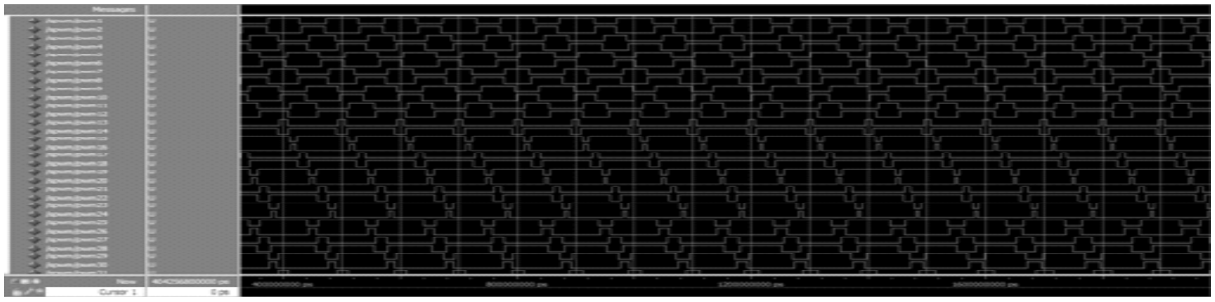


Figure 18: PWM Pulses -1

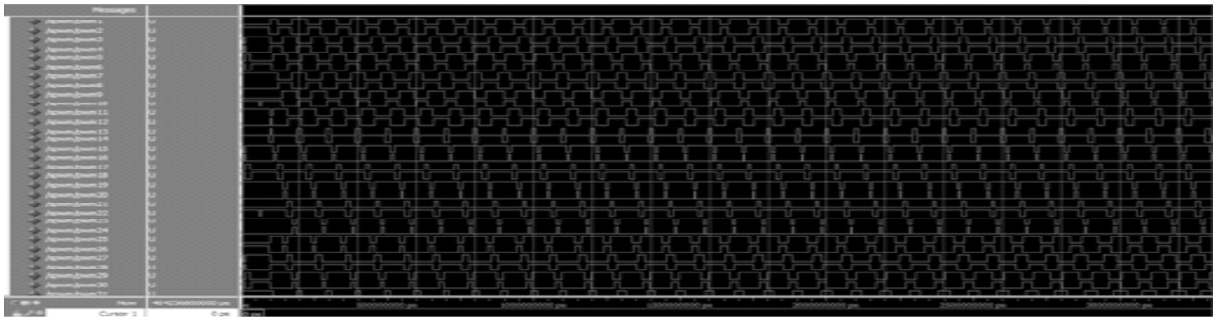


Figure 19: PWM Pulses -2

8.5. Synthesis/ Place and route Report

Device utilization summary: Selected Device : 6slx25ftg256-3

Slice Logic Utilization

Number of Slice Registers:	1105 out of 30064 3%
Number of Slice LUTs:	3479 out of 15032 23%
Number used as Logic:	3479 out of 15032 23%

Slice Logic Distribution

Number of LUT Flip Flop pairs used:	3766
Number with an unused Flip Flop:	2661 out of 3766 70%
Number with an unused LUT:	287 out of 3766 7%
Number of fully used LUT-FF pairs:	818 out of 3766 21%
Number of unique control sets:	34

IO Utilization

Number of IOs:	71
Number of bonded IOBs:	71 out of 186 38%
IOB Flip Flops/Latches:	1

Specific Feature Utilization

Number of BUFG/BUFGCTRLs:	1 out of 16 6%
Number of DSP48A1s:	18 out of 38 47%

Timing Summary: Speed Grade: -3

Minimum period: 22.874ns (Maximum Frequency: 43.717MHz)

Minimum input arrival time before clock: 10.180ns

Maximum output required time after clock: 3.597ns

9. HARDWARE DEVELOPED

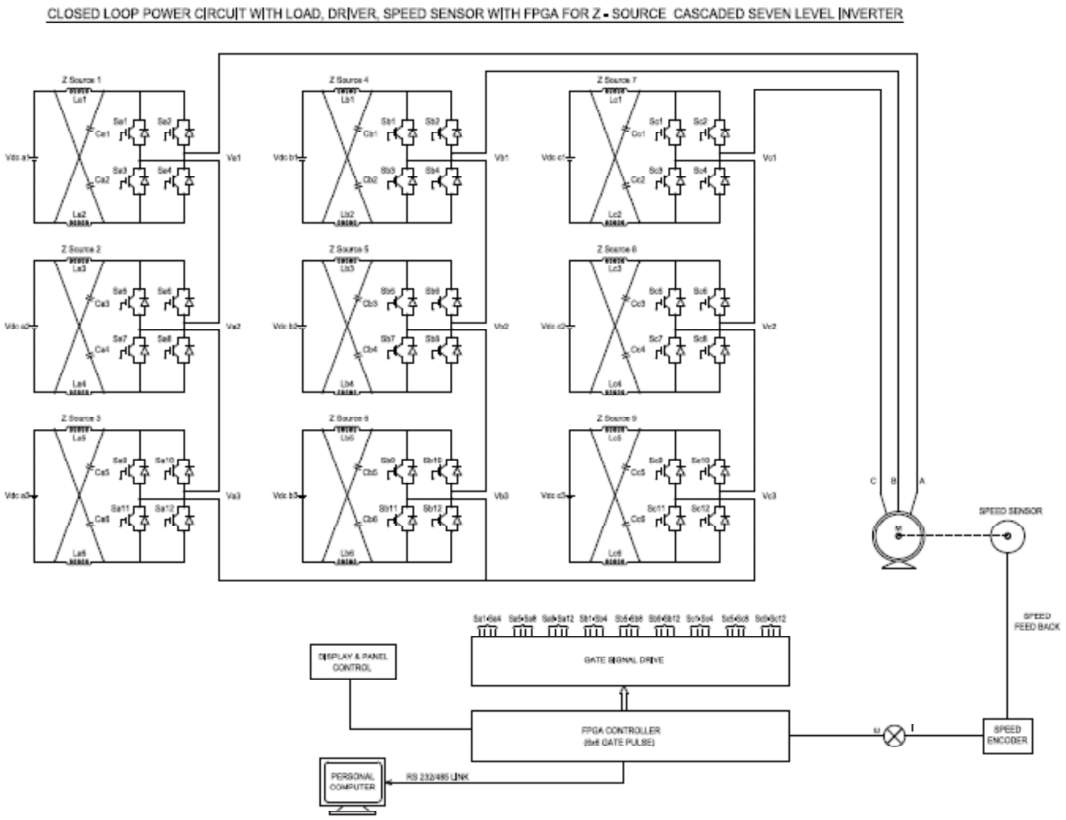


Figure 20: Proposed hardware for Speed control of induction motor using PSPWM implemented on FPGA

The proposed Cascaded H-Bridge multilevel inverter is connected to induction motor and speed control of the motor is performed. A speed sensor is connected to the shaft of the motor, latter encoded and given as input to the FPGA which acts as digital controller. HEDS5645 QEP Speed Sensor is used to Sense the Speed of Induction Motor. The Phase shifted carrier disposition (PSPWM) is implemented in FPGA. This digital controller (FPGA) will generate PWM based on the proportional integral control received from the sensor. These generated PWM is fed into the MOSFET of the proposed hardware circuits. It switches the MOSFET thereby the speed of the induction motor is controlled.

The following are the parameters considered for both simulation and hardware implementation of speed control of induction motor. Torque speed characteristics were performed

- dc link voltage—— 300 V DC
- Inverter power rating ———— 200 W
- Inverter o/p voltage———————— 0-200 V ACrms(line to line)
- Switching frequency———————— 2000Hz
- NO OF CARRIER USED———— 6 Nos
- RATED POWER———— 0.25HP
- VOLTAGE———————— 200VRMS (Ph-Ph)DELTA CONNECTION
- CURRENT———————— 0.6A rms
- FREQUENCY———————— 50Hz
- POLES———————— 4 Pole
- SYNCHRONOUS SPEED————————- 1500RPM

- Rs———————————————— 20.2OHM
- LS———————————————— 0.032H
- Rr———————————————— 8.02 OHM
- Lr———————————————— 0.032H
- LM(mutual inductance)—— 0.601H
- Inertia(j)———————————— 0.0051

Figure 21 and 22 illustrates the hardware wiring diagram of the cascaded multilevel inverter and the driver circuit used in the system respectively. Figure 20 gives the hardware set up used for conducting the speed characteristics of induction motor. Figure 23 gives the Pulse width modulated signal generated in FPGA. Figure 24, 25, 26, 27 gives the current THD, voltage THD, Phase voltage, phase current measured using THD meter respectively. Table 4 illustrates the simulated and achieved comparison for different quantitative measures. During test on induction motor, THD meters were used to acquire the required results and later used for comparison. It was found that the proposed hardware and the VLSI architecture offers reduced Harmonics. Figure 28 gives the snapshot of the proposed hardware circuit implemented and the tests were conducted. It was found that Phase shifted carrier gives better stator current THD. Table 5 gives the Torque produced on the Induction motor after applying various PWM techniques. This indicated that the proposed PWM technique based on the VLSI architecture has a high Torque due to stator current THD. This improves the efficiency of the system. Hence making this technique suitable for speed control application.

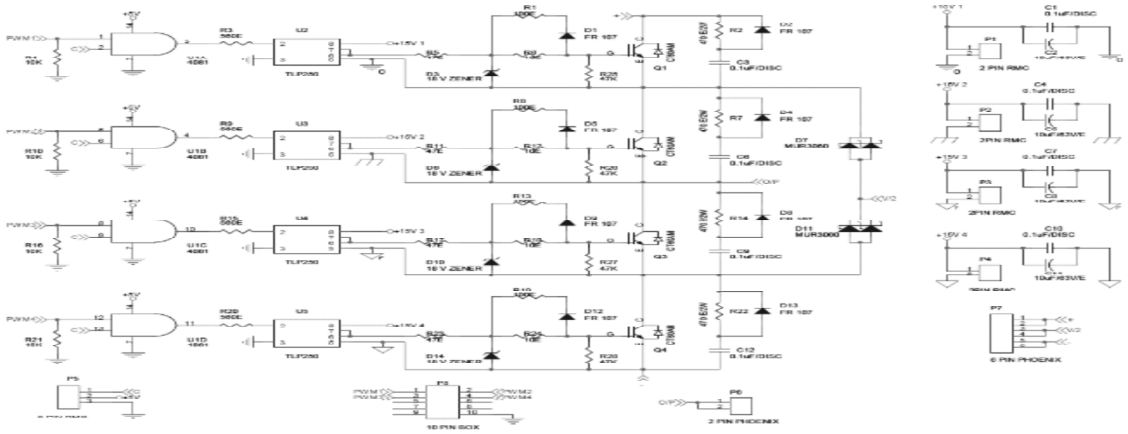


Figure 21: Power Circuit for Cascaded seven level Inverter

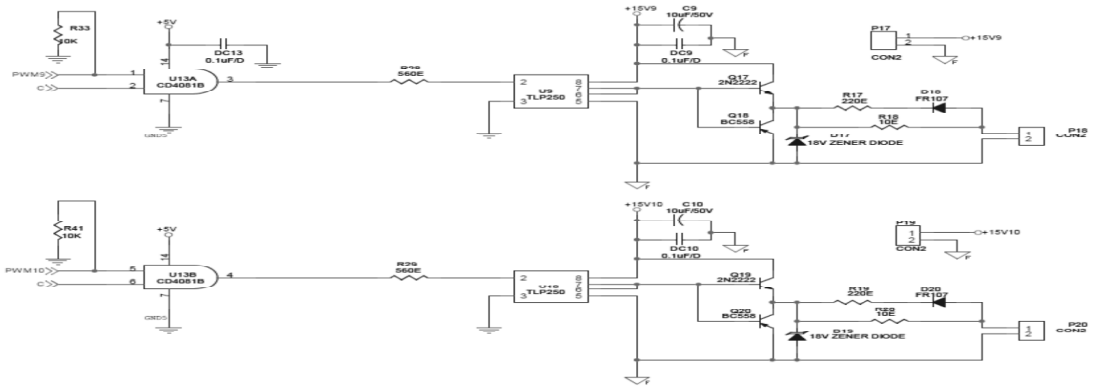


Figure 22: Driver Circuit for Cascaded seven level Inverter

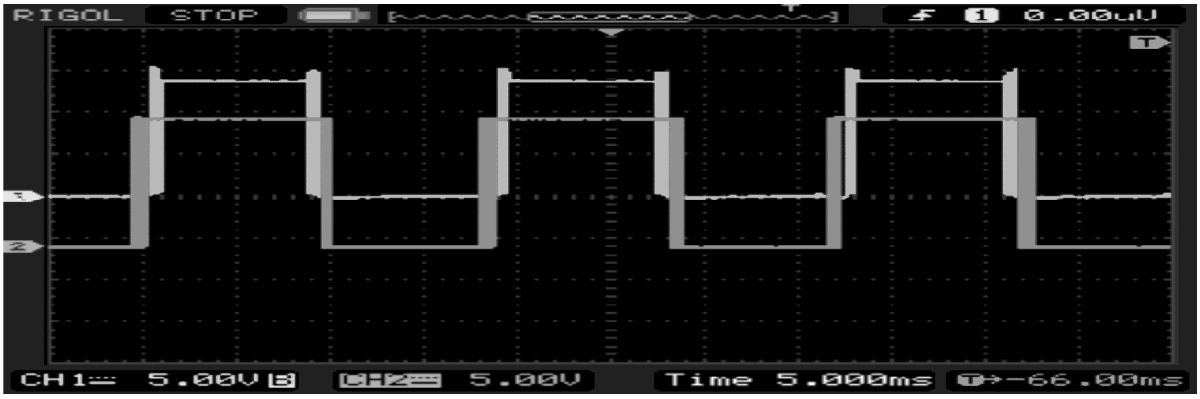


Figure 23: PWM pulse generated from FPGA displayed in DSO

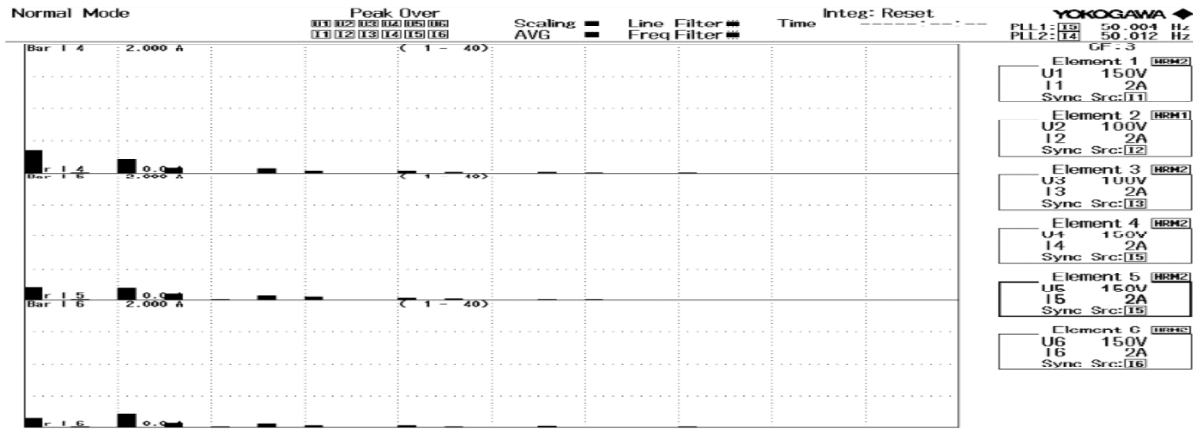


Figure 24: Current THD measured using THD meter

Figure 25: Voltage THD measured using THD meter

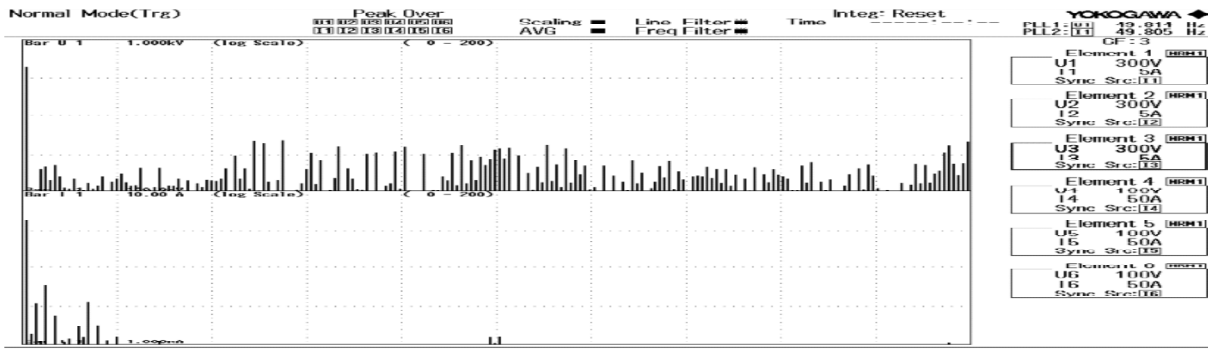


Figure 26: Phase voltage THD measured using THD meter

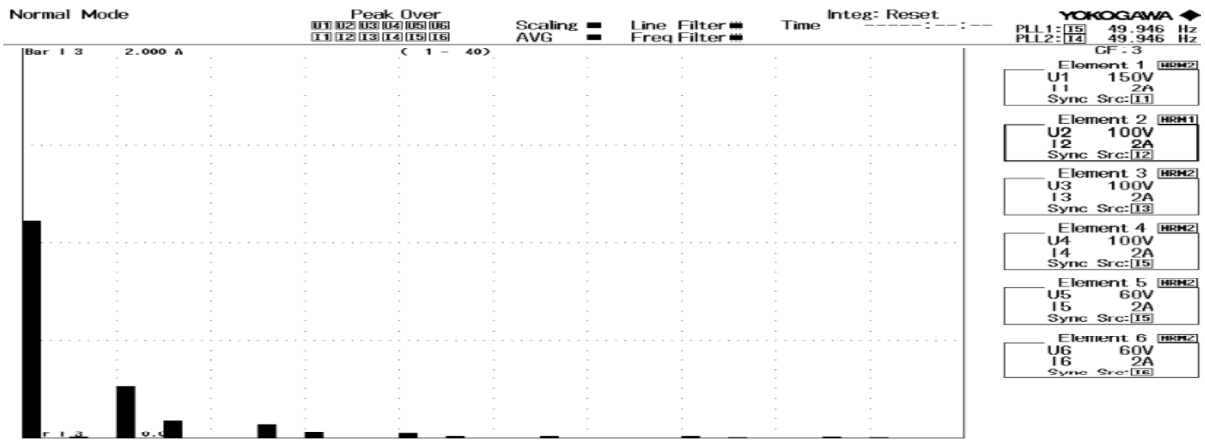


Figure 27: Phase current THD measured using THD meter

Table 4
Comparison of simulated and actual quantitative parameters for the proposed hardware circuit.

PWM Technique	*Type*	*Phase Voltage THD*	*Line Voltage THD*	*Stator Current THD*	*Voltage Stress (v)*	*Speed settling time (sec)*
PD	Simulated	25.33%	9.29%	1.4%	50	0.2
	Actual	25.9%	9.5%	1.49%	50	0.21
POD	Simulated	25.32%	13.35%	1.27%	50	0.2
	Actual	26.1%	13.7%	1.32%	50	0.21
PS	Simulated	26.78%	15.48%	0.69%	50	0.21
	Actual	27.3%	15.7%	0.72%	50	0.22

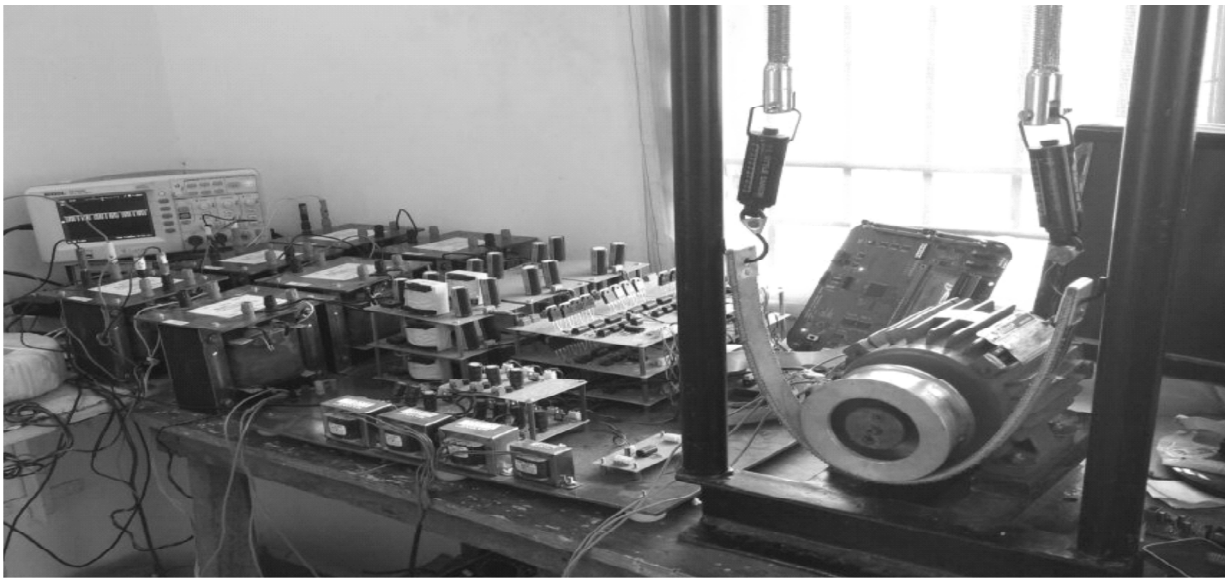


Figure 28: Cascaded Multilevel inverter circuit set up

Table 5
Torque produced on the Induction motor after applying various PWM technique

PWM Technique	*Torque*
PD	0.98-1.02NM
POD	0.94-1.06NM
PS	0.99-1.01NM

10. CONCLUSION

In this work, VLSI architecture for phase shifted carrier PWM control was developed and tested in real time by connecting the proposed hardware with FPGA and induction motor. Speed control characteristics of the induction motor were performed. The performance of the proposed circuit is validated using THD, stress caused by voltage and the time taken to settle. The performance of the proposed circuit was evaluated using THD, voltage stress and settling time. Brief Simulations were carried out and the results were validated using the hardware and THD values are obtained using THD meters. From the extensive analysis it was found that stator current THD for Phase Shifted PWM technique was found to exhibit low THD and the torque exhibited on the induction motor was found high. Hence the efficiency of the system increases.

REFERENCES

[1] K. Corzine and Y. Familiant, "A New Cascaded Multilevel H-Bridge Drive", IEEE Transactions Power Electron., Vol. 17, No.1, (2002), pp. 125-131.

[2] M. Reza Banaei and A.R. Dehghanzadeh, ¯A Z-Source novel based multilevel inverter for renewable sources fed DVR , IEEE International Conference, Power Quality Conference pp.1-6, (2011).

[3] M.R. Mohamad Reza Banaei and A.R. Ali Reza Dehghanzadeh, "DVR based cascaded multilevel Z-source inverter", IEEE International Conference, Power and Energy pp.51-56, (2010).

[4] X. Yuan and I. Barbi, "Fundamentals of a New Diode Clamping multilevel Inverter", IEEE Transactions Power Electron., Vol. 15, No.4, (2000), pp. 711-718.

[5] Jason R. Wells, XinGengPatrick L. Chapman Philip T. Kreinand Brett M. Nee, "Modulation-Based Harmonic Elimination", IEEE Transactions on power electronics, vol. 22, no. 1, pp336-340, (2007).

[6] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multi-level inverters," Conf. Rec. IEEE-IAS Annu. Meeting, (1999), pp. 1186-92.

[7] B.-M. Song, J. Kim, J.-S. Lai, K.-C. Seong, H.-J. Kim, and S.-S. Park, "A multilevel soft switching inverter with inductor coupling," IEEE Trans. Ind. Applications., vol. 37, pp. 628-36, (2001).

[8] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," IEEE Trans. Ind. Applicat., vol. 36, pp. 834- 841, (2000).

[9] Y.-S. Lai and F.-S. Shyu, "Topology for hybrid multilevel inverter," IEE Proc. Electr. Power Applicat., vol. 149, pp. 449-458, (2002).

[10] Ki-Seon Kim, Young-Gook Jung, and Young-Cheol Lim, Member, IEEE"A New Hybrid Random PWM Scheme" IEEE Transactions on Power Electronics, Vol. 24, No. 1, January (2009).