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A New Single-Phase Multilevel Inverter with Reduced Number of Switches for Solar Applications

M. Arun Noyal Doss*, K. Harsha, K. Mohanraj* and R. Shyambabu****

ABSTRACT

This paper presents a new asymmetric multilevel (MLI) inverter topology, which is capable of generating large number of levels with minimum number of power electronic switches, gate drive circuits, power diodes, and dc voltage sources. Less number of switches leads to reduction of size, simple control strategy and reduced cost. The DC sources of the proposed asymmetrical multilevel is replaced with Photovoltaic (PV) system. The PV cell is connected to multi-level inverter through Buck-Boost converter. MLI have come out as an attractive high power medium voltage converter to reduce harmonic component in the output waveform. A sinusoidal pulse width modulation (SPWM) technique is used to generate the PWM signal for inverter switches. The proposed asymmetrical fifteen level MLI is compared with the conventional cascaded fifteen level MLI. As compared with conventional cascaded MLI the proposed MLI is having reduced number of switches and conduction losses. The proposed asymmetrical fifteen level MLI is simulated using MATLAB/Simulink and the corresponding results are presented in this paper.

Keywords: PV system, Asymmetric, H-bridge multilevel inverter, Total Harmonic Distortion.

1. INTRODUCTION

Multilevel Inverter (MLI) technology is a very important alternative in the area of high power, medium-voltage applications. The concept of multilevel inverters has been introduced since 1975. The term multilevel began with the three-level converter. Later, several multilevel converter topologies have been developed [1]. Multilevel inverter is used to generate an AC output voltage from a DC voltage source. In the place of multiple dc voltage sources capacitors, batteries, and renewable energy voltage sources can be used. MLI topologies have been also considered in PV applications. The lower harmonic contents, lower switching losses, and also reduction of (dv / dt) stresses on the load is obtained by increasing the number of dc voltage input (levels) [2], [3].

In general, there are three types of multilevel converters such as Neutral Point Clamped converter (NPC), Flying Capacitor converter (FC) and Cascaded H-bridge converter (CHB) [4] and [5]. The neutral point converter proposed by Nabae, Takahashi, and Akagi was basically a three-level diode-clamped inverter. A diode clamped multilevel (m-level) inverter typically consists of (m-1) capacitors on the dc bus and produces m levels on the phase voltage. It is the simplest control method and because of all devices are switched at the fundamental frequency the inverter efficiency is high. The major drawback of NPC converter is difficult to control the real power flow of the individual converter in multi-converter systems [6].

To overcome these problems Flying Capacitor converter is introduced. Meynard and Foch introduced a flying-capacitor based inverter. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors. It can control both real and

* Assistant Professor, Department of Electrical and Electronics Engineering, SRM University.

** PG Scholar, Department of Electrical and Electronics Engineering, SRM University.

reactive power flow. The major drawback of FC converter is the inverter control can be very complicated, and the switching frequency and switching losses are high for real power transmission [7].

As compared to Diode-clamped and Flying capacitor converters, Cascaded H-bridge converter requires the less number of components to achieve the same number of voltage levels. But, it needs a separate dc sources for real power conversions, thereby limiting its applications [8] and [9].

The proposed asymmetrical multilevel inverter has more advantages in comparison with the conventional cascaded and other similar topologies. This newly proposed multilevel inverter have a less number of switches, more levels can be obtained with simple control circuit. As the number of conducting devices reduces, switching losses are reduces, hence the efficiency of the inverter is also high. The switches of this proposed asymmetrical multilevel inverter is controlled by sinusoidal pulse width modulation technique, as it is one of the best and simple techniques to reduce THD [10].

2. CONVENTIONAL CASCADED FIFTEEN LEVEL MULTILEVEL INVERTER

This conventional cascaded 15 level multilevel inverter is made of 12 switches and 3 dc sources and is shown in Fig. 1. A cascaded multilevel converter consists of the number of H-bridge converter units with separate dc sources for each unit, which is connected in cascade or series. In symmetric cascaded multilevel converter, dc voltage sources values of similar cells are equal. For the same number of power devices, asymmetric cascade multilevel topology significantly increases the number of output voltage levels. In these topologies, the values of dc voltage sources of different cells are non-equal. However, the symmetric and asymmetric CHB converter requires a large number of switches and dc voltage sources [11].

3. PROPOSED ASYMMETRICAL MULTILEVEL INVERTER

The proposed Asymmetrical multilevel inverter topology is shown in Fig. 2. In this structure, the values of the dc voltages are unequal. Therefore, this topology is called asymmetrical multilevel inverter.

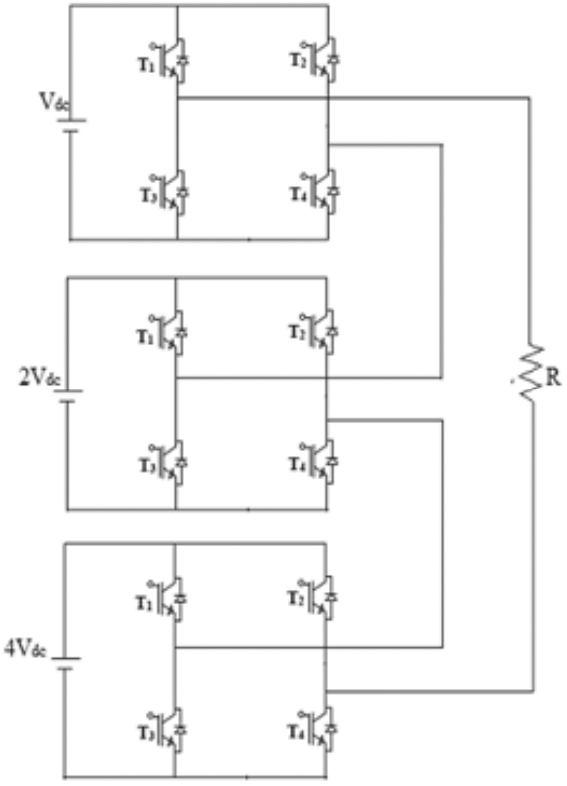


Figure 1: Conventional cascaded multilevel inverter

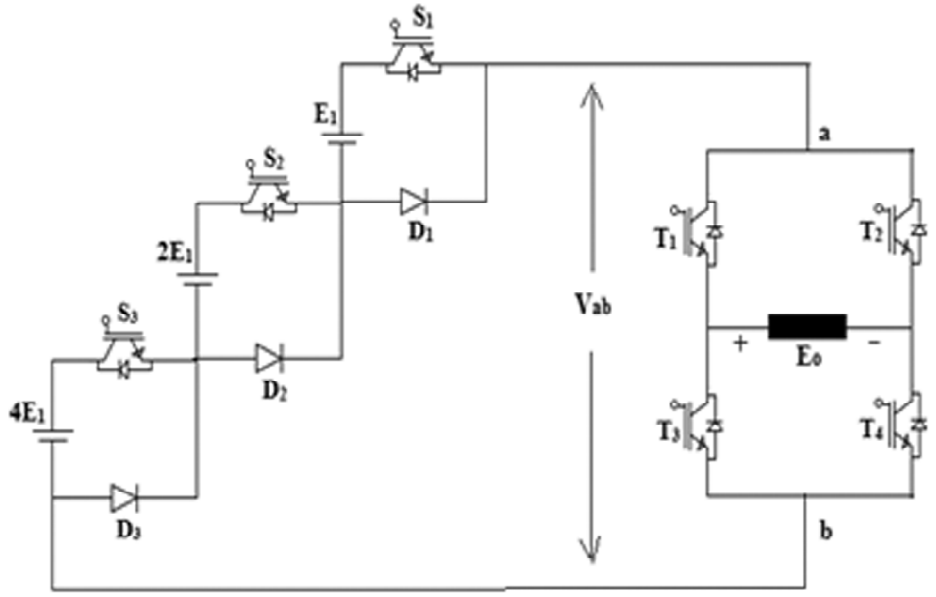


Figure 2: Proposed asymmetric multilevel inverter.

For this method, the number of levels and maximum output voltage are given by (1) and (2), respectively

$$N_{level} = 2\hat{}(Z+1)-1 \quad (1)$$

$$E_{0,max} = (2Z-1)E \quad (2)$$

Where Z represents the number of dc sources. In the proposed asymmetric topology, the number of IGBTs is obtained by

$$N_{IGBT} = Z+4 \quad (3)$$

The proposed asymmetric multilevel inverter topology can be used in renewable energy sources and medium-voltage applications. The switching states of proposed multilevel inverter are shown in the TABLE

Table I
Switching States Of Proposed Asymmetrical Multilevel Inverter

State	Switches States							Output
	S1	*S2*	*S3*	*T1*	*T2*	*T3*	*T4*	Voltage (V)
1	0	0	0	1	0	1	0	0
2	1	0	0	1	0	0	1	E_1
3	0	1	0	1	0	0	1	$2E_1$
4	1	1	0	1	0	0	1	$3E_1$
5	0	0	1	1	0	0	1	$4E_1$
6	1	0	1	1	0	0	1	$5E_1$
7	0	1	1	1	0	0	1	$6E_1$
8	1	1	1	1	0	0	1	$7E_1$
9	1	1	1	0	1	1	0	$-7E_1$
10	0	1	1	0	1	1	0	$-6E_1$
11	1	0	1	0	1	1	0	$-5E_1$
12	0	0	1	0	1	1	0	$-4E_1$
13	1	1	0	0	1	1	0	$-3E_1$
14	0	1	0	0	1	1	0	$-2E_1$
15	1	0	0	0	1	1	0	$-E_1$

I. The DC source of the proposed multilevel inverter is replaced with the PV. In this application capacitor voltage balancing is important. The comparison of the proposed MLI with the conventional multilevel inverter on the basis of circuit component requirement is shown in TABLE II. The proposed asymmetrical multilevel topology use only one full-bridge converter, which is a restriction for high- voltage applications, in addition, this topology need more number of devices.

4. MODELLING OF THE SOLAR CELL

A solar cell is the building block of a solar panel. A photovoltaic module is formed by connecting many solar cells in series and parallel. Considering only single solar cell, it can be modeled by utilizing a current source, a diode and two resistors [12], [13]**.** This model is known as a single diode model of solar cell and is shown in the Fig. 3.

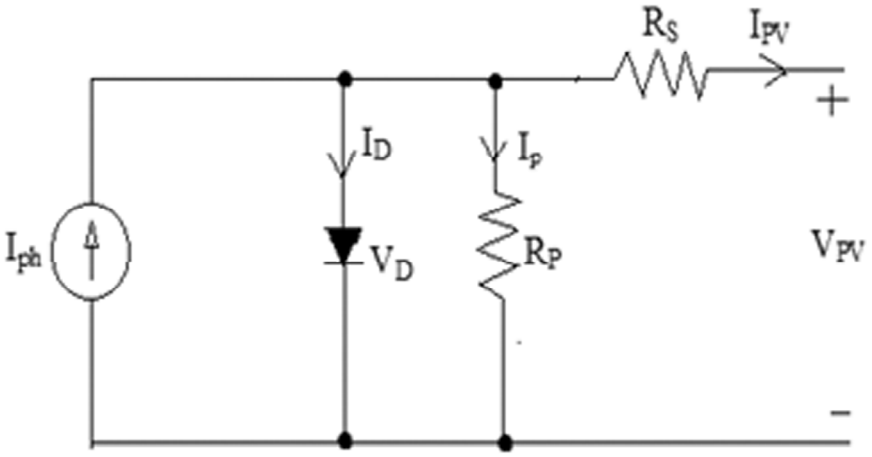


Figure 3: Equivalent circuit of PV module

The current source I_{ph} represents the cell photocurrent. R_{sh} and R_s are the intrinsic shunt and series resistances of the cell, respectively.

The photovoltaic panel can be modeled mathematically as given in equations.

$$I_{PV} = I_{Ph} - I_D - \frac{V_D}{R_P} \tag{4}$$

$$I_{Ph} = \left(I_{SCref} + K_I(T_K - T_{ref})\right) * \frac{\lambda}{10000} \tag{5}$$

$$I_D = I_0\left(e^{\left(\frac{(R_S I_{PV} - V_{PV})q}{AKT}\right)} - 1\right) \tag{6}$$

$$I_0 = I_{rs}\left[\left(\frac{T_K}{T_{ref}}\right)^3 * \left(e^{\frac{qE_{gO}}{AK} * [\frac{1}{T_{ref}} - \frac{1}{T_K}]}\right)\right] \tag{7}$$

The total output current of the PV cell is obtained as

$$I_{PV} = I_{Ph} - \left\{I_{rs}\left[\left(\frac{T_K}{T_{ref}}\right)^3 * \left(e^{\frac{qE_{GO}}{AK} * \left[\frac{1}{T_{REF}} - \frac{1}{T_K}\right]}\right)\right] * \left(e^{\left(\frac{(R_S I_{PV} - V_{PV})q}{AKT}\right)} - 1\right)\right\} - \left[\frac{V_{PV} + I_{PV} R_S}{R_P}\right] \tag{8}$$

If number of cells connected in series N_S and in parallel is N_P, then I_{PV} is given as

$$I_{PV} = N_P I_{Ph} - N_P \left\{ I_{rs} \left[\left(\frac{T_K}{T_{ref}} \right)^3 * \left(e^{\frac{qE_{GO}}{AK} * \left[\frac{1}{T_{REF}} - \frac{1}{T_K} \right]} \right) \right] * \left(e^{\left(\frac{(N_S R_S I_{PV} - N_P V_{PV}) q}{A N_S N_P K T} \right)} - 1 \right) \right\} - \left[\frac{V_{PV} + I_{PV} R_S \left(N_S / N_P \right)}{R_P} \right] \quad (9)$$

5. PULSE WIDTH MODULATION

Pulse width modulation refers to a method of carrying information on a train of pulses, the information being encoded in the width of the pulses. The pulses have constant amplitude but their duration varies in direct proportion to the amplitude of analog signal. Sinusoidal PWM is the most effective method for producing a controlled output for inverter

In Multiple Pulse Width Modulation, by varying the width of each pulse in proportion to the amplitude of the reference wave the distortion factor and lower order harmonics can be reduced significantly and the width of all the pulses are maintained same. This type of modulation is known as Sinusoidal Pulse Width Modulation.

By comparing sinusoidal reference signal with a triangular carrier wave of frequency (f_c), the gating signal is generated. The inverter output frequency (f_0), and its peak amplitude (A_r), determines the frequency of reference signal f_r and controls the modulation index M, and then in turns the rms output voltage V_0. The number of pulses per half cycle depends upon the carrier frequency. By varying the modulation index M, the rms output voltage can be varied. Each pulse corresponds approximately to the area under sine wave

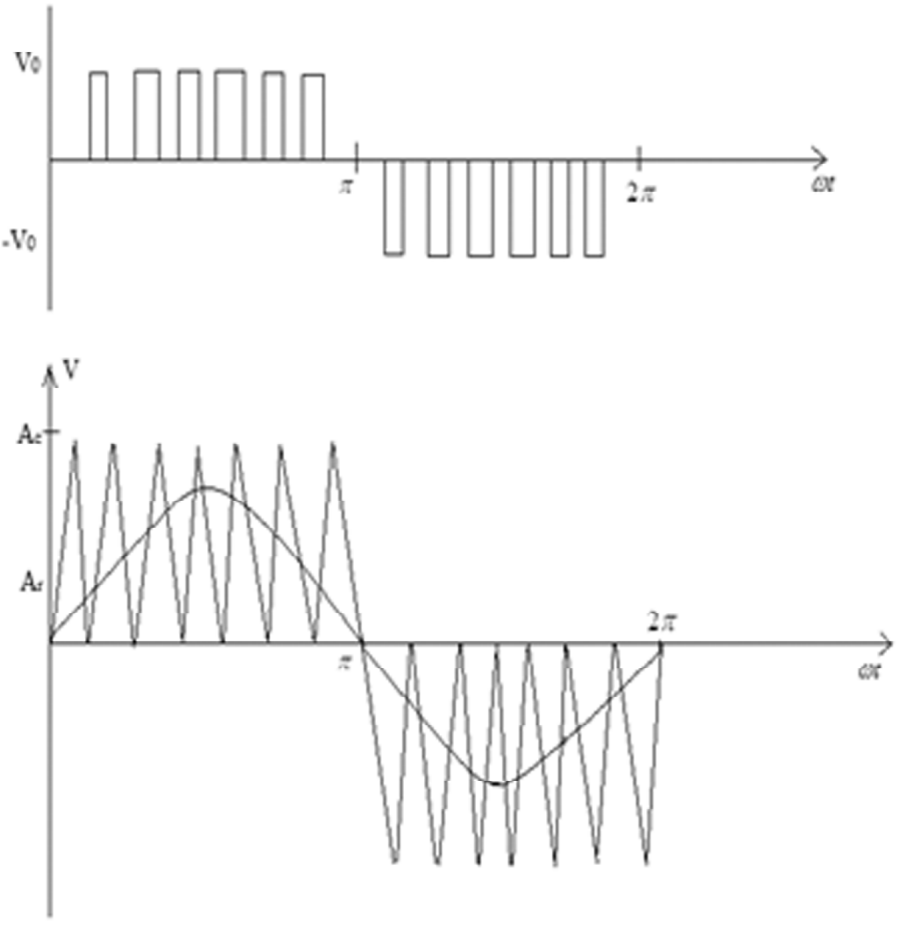


Figure 4: Sinusoidal pulse width modulation

between the adjacent midpoints of off periods on the gating signals. The sinusoidal pulse width modulation wave form is shown in Fig. 4.

6. MODES OF OPERATION OF ASYMMETRICAL MULTILEVEL INVERTER

The proposed topology consists of two sections namely level generator which is responsible for the generation of stepped voltage waveform and secondly the polarity generator stage which is responsible for generating the polarity of the output voltage. Proper switching of the inverter can produce 15 output voltage levels: 0, 1, 2, 3, 4, 5, 6, 7, -1, -2, - 3, -4, -5, -6, -7 E_1. In order to generate 15 levels of output voltage, the voltages of different DC sources must be added, as the output voltage is the sum of the DC voltage sources. Switches S_1 S_2 S_3 are involved in generation of positive levels only and the inversion of polarity is performed by the Switches T_1 – T_4. The proposed Inverter's operation can be divided into eight switching states as shown in Fig. 5. The required output positive voltage levels produced by the level generator are generated as follows:

MODE 1: To generate the zero voltage across load, the load terminals will be short circuited by switching ON the switches T_1, T_3 and is shown in Fig 5 (a).

MODE 2: When the Switch S_1 is ON, the diode D_1 is reverse biased and the current flows through E_1-S_1-T_1-T_4-D_3-D_2-E_1 and the resulting terminal voltage $V_{ab} = E_1$ and is shown in Fig 5 (b).

MODE 3: When the Switch S_2 is ON, the diode D_2 is reverse biased and the current flows through $2E_1$-S_2-D_1-T_1-T_4-D_3-$2E_1$ and the resulting terminal voltage $V_{ab} = 2E_1$ and is shown in Fig 5 (c).

MODE 4: When the Switch S_1 and S_2 is ON, the diodes D_1 and D_2 are reverse biased and the current flows through $2E_1$-

S_2-E_1-S_1-T_1-T_4-D_3-$2E_1$ and the resulting terminal voltage $V_{ab} = 3E_1$ and is shown in Fig 5 (d).

MODE 5: when the Switch S_3 is ON, the diode D_3 is reverse biased and the current flows through $4E_1$-S_3-D_2-D_1-T_1-T_4-$4E_1$ and the resulting terminal voltage $V_{ab} = 4E_1$ and is shown in Fig 5 (e).

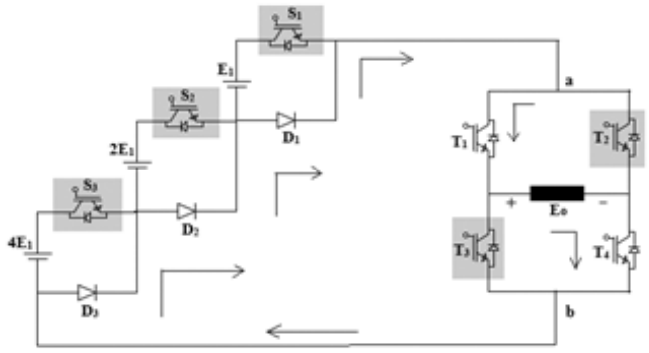
MODE 6: When Switch S_3 and S_1 is ON, the diodes D_3 and D_1 are reverse biased and the current flows through $4E_1$-S_3-D_2-E_1-T_1-T_4-$4E_1$ and the resulting terminal voltage $V_{ab} = 5E_1$ and is shown in Fig 5 (f).

MODE 7: When Switch S_3 and S_2 is ON, the diodes D_3 and D_2 are reverse biased and the current flows through 4E1-S3-$2E_1$-S_2-D_1-T_1-T_4-$4E_1$ and the resulting terminal voltage $V_{ab} = 6E_1$ and is shown in Fig 5 (g).

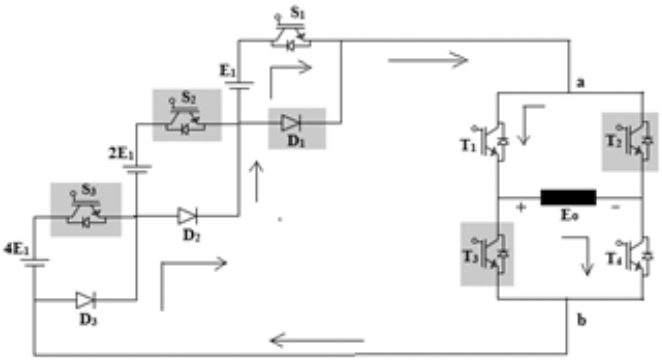
MODE 8: When the Switch S_1, S_2 and S_3 is ON, the diodes D_1, D_2 and D_3 are reverse biased and the current flows through $4E_1$-S_3-$2E_1$-S_2-E_1-S_1-T_1-T_4-$4E_1$ and the resulting terminal voltage $V_{ab} = 7E_1$ and is shown in Fig 5 (h).

Table 2
Comparison of The Proposed 15-level Inverter with the Conventional 15-level Inverters on the Basis of Circuit Component Requirements.

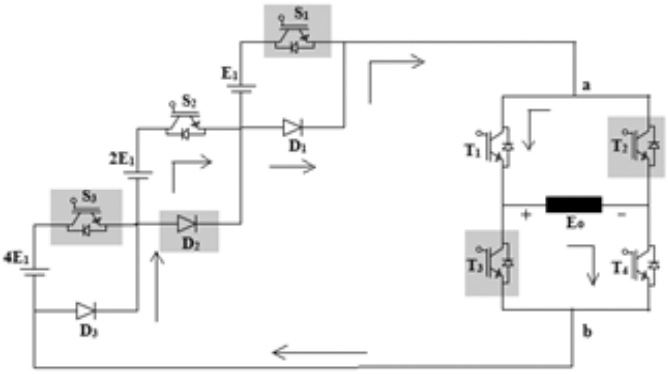
Inverter Type	*Main Switches*	*Diodes*	*Dc Sources*	*Balancing Capacitors*
Diode Clamped Inverter	12	12	1	0
Flying Capacitor Inverter	12	0	1	12
Cascaded Inverter	12	0	3	0
Proposed Inverter	7	3	3	0



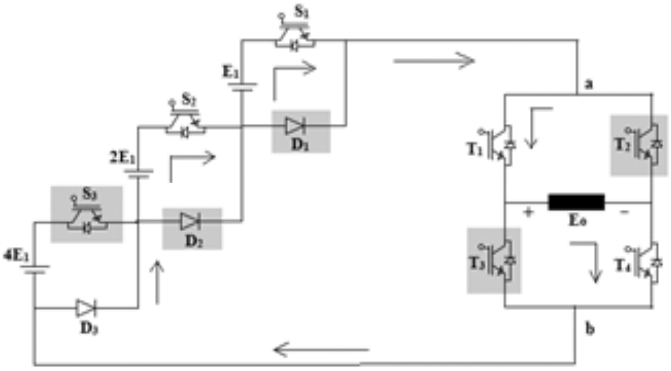
(a) Mode 1



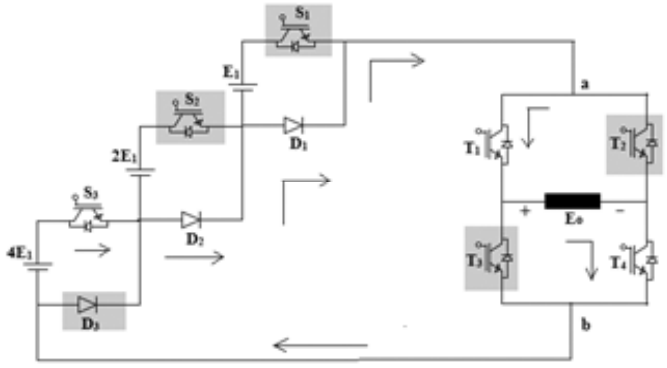
(b) Mode 2



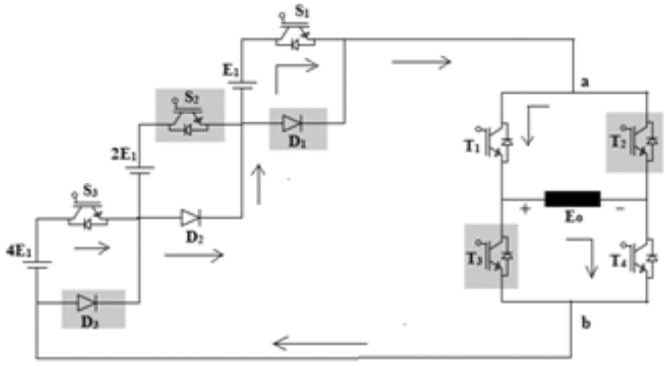
(c) Mode 3



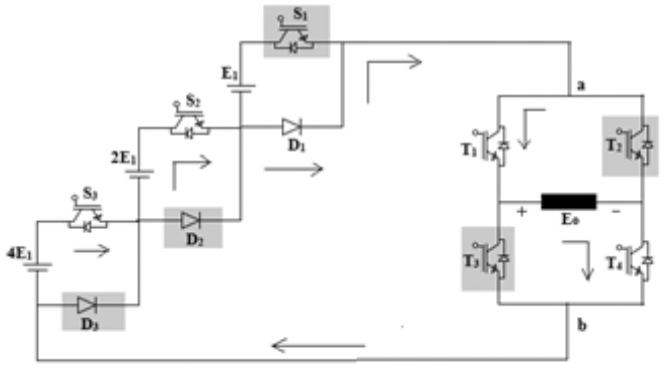
(d) Mode 4



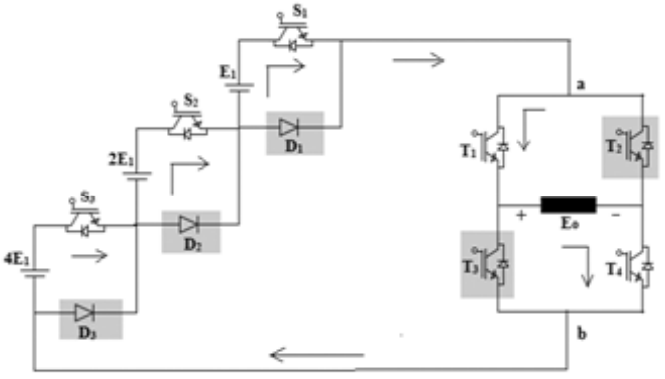
(e) Mode 5



(f) Mode 6



(g) Mode 7



(h) Mode 8

Figure 5: Different operating modes of proposed fifteen level multilevel inverter

7. SIMULATION RESULTS

The simulation of the proposed inverter is carried out in MATLAB/SIMULINK to show the effectiveness of the proposed inverter topology. The inverter dc voltage sources are assigned with magnitude of 15V, 30V, 60V satisfying the ration 1:2:4 in a binary fashion. The output voltage waveform and harmonic spectrum of the conventional MLI is shown in Fig. 6 and Fig. 7. The output voltage waveform of the proposed inverter feeding R-load of 100 Ω is shown in Fig. 8. Since the load is resistive the THD is found to be 6.68% in both voltage and current waveforms.

The output voltage and harmonic spectrum of the proposed MLI is compared with the conventional MLI and is having less number of switches with improved THD. As conventional cascaded MLI is having

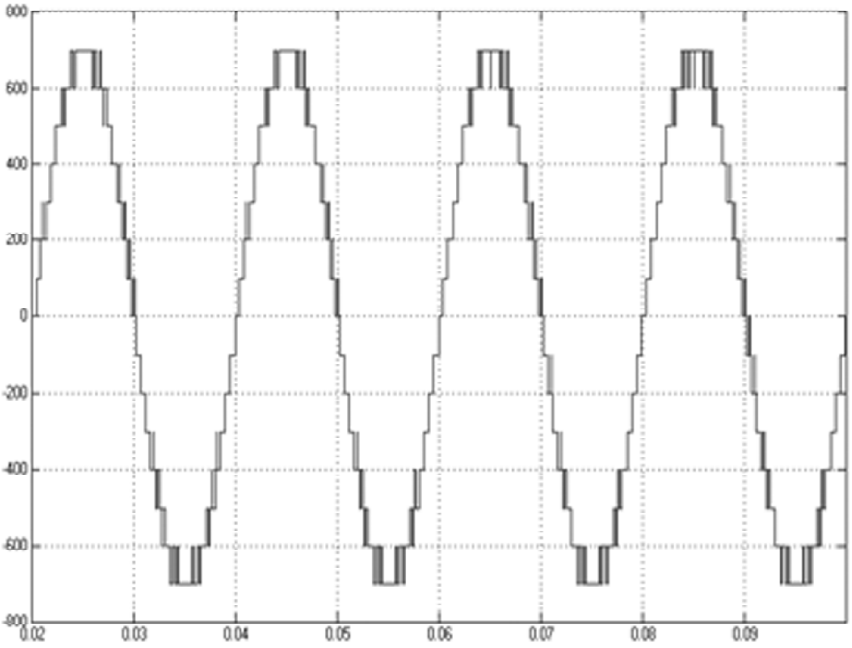


Figure 6: Output voltage waveform of conventional cascaded multilevel inverter

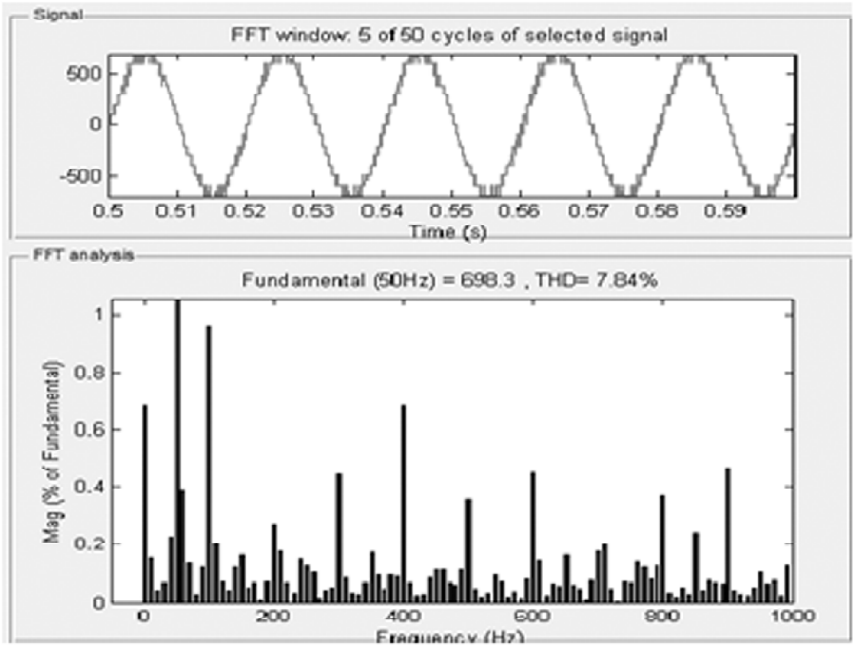


Figure 7: Output voltage and harmonic spectrum of the conventional cascaded 15 level MLI (THD=7.84%)

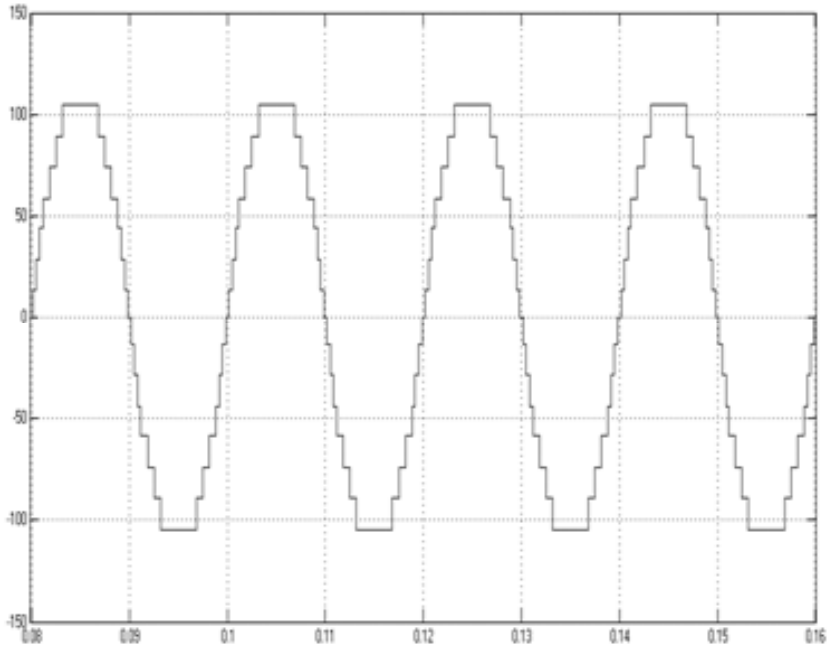


Figure 8: Output voltage waveform of proposed multilevel inverter

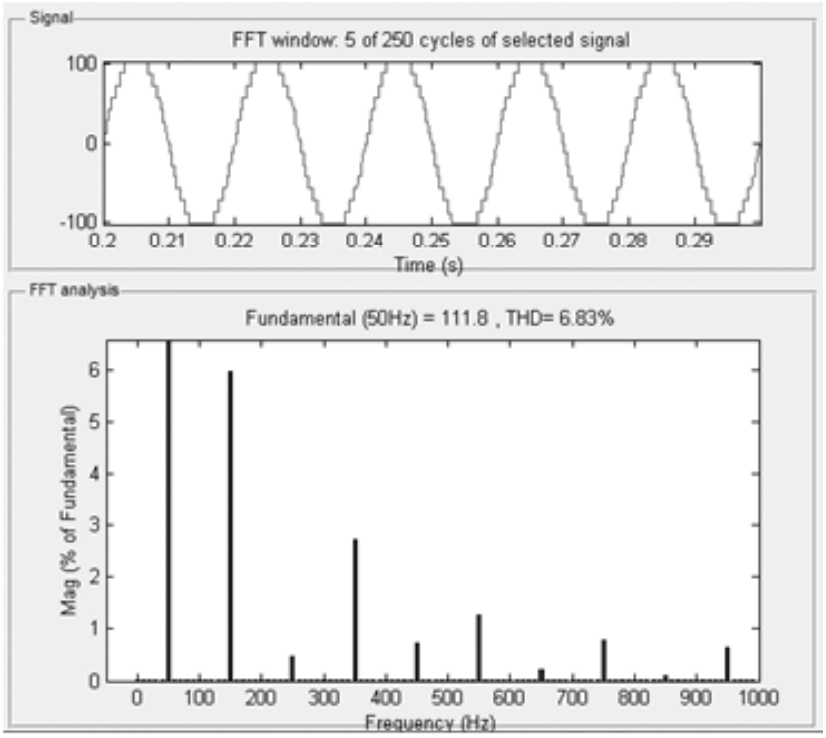


Figure 9: Output voltage and harmonic spectrum of the proposed PV fed 15 level MLI (THD=6.68%)

7.84% THD and the proposed MLI is having 6.68% THD. The output voltage and harmonic spectrum of the proposed PV fed multilevel inverter is shown in the Fig. 9.

9. CONCLUSION

The increased number of voltage levels is obtained with the reduced number of switches and distortions in a multilevel inverter. Different topologies of multilevel inverter are compared for the efficient operation with the variable renewable inputs and optimal design of inverter, asymmetrical multilevel inverter is

considered. The proposed multilevel inverter design has less number of switches which represent simple structure and higher efficiency operation. The total harmonic distortion is reduced with the implementation of sine pulse width modulation technique. For the control of the PV system input, a DC-DC buck-boost converter is implemented. The inverter is fed with a PV system which has a variable output voltage, for this purpose asymmetrical multilevel inverter topology working and operation is observed and optimum results are obtained.

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